GANIL / GIP
CLRC / NPSG

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Clock **E**vent **N**umber **T**ransmitter **R**eceiver **U**niversal **M**odule

VXI-C Standard

Specification

Please note that this module is under development and so is potentially subject to modifications before the final version.

CONTENTS

Overview

The reason for developing this type of module, for the GANIL data acquisition, is to support multiple detectors with their own electronics working in parallel. This is the case, for example, with the new experiments of how to attach ancillary detectors to EXOGAM, how to attach ancillary detectors to VAMOS and how to attach VAMOS to EXOGAM.

Central to both discussions is a synchronisation method allowing both systems to read some common information which can be used in the event builder to merge data from the two apparatuses.

In essence the proposal is for a VXI-C sized module which can either generate or receive 2 pieces of synchronising data:

- an event number
- a real time clock or timestamp (100MHz).

The whole system could be considered as a master CENTRUM (controlled by a master trigger) and seven slave CENTRUM modules connected to it. The master CENTRUM has seven serial transmission channels (TX1..7) to give the information ($time_{txn}$ and event number) to each reception channel (RX) of the slave CENTRUM's. A counter, inside the master, correlated to the trigger controls the event number value while each time value depends of the tagging signal received on its respective channel. As it is the same board (hardware and software) for both ends, local time subtagging could also be used in a slave module that is part of a coupled detector acquisition system.

In the particular case of coupling with EXOGAM, the EXOGAM event number will be used because EXOGAM will be running about 10 times faster than VAMOS. There is a facility to check that the event number in the module is correct by comparing the bottom 4 bits with the broadcast bottom 4 bits of the EXOGAM event number.

The real time clock will be used for Recoil Decay Tagging (RDT) experiments.

This proposed C-sized VXI module which is registered based can be fitted (with a mechanical adapter) in a D-sized VXI crate.

Chapter 1 : Specifications

1.1 Characteristics and functions

A timing diagram and the CENTRUM front panel are given in appendixes 1 and 2.

1.1.1 Standard

This instrumentation module is designed in conformance to C size VXI standards. It will be the same module for both ends Transmit (TX) and Receive(RX).

1.1.2 Absolute Clock

The system consists of one loadable time counter and 7 time registers (1by TX channel). It works with a 48 bits data width and is driven by a 100 MHz TCXO (stability : 1ppm).

Each tagging (time counter -> time register$_n$) will be local LTAG<7..1> (NIM input-LEMO ØØ) or remote RTAG<7..1> (one twisted pair in each serial link cable). These inputs will receive signals with good timing (FT for example) and will be equipped with programmable delay lines to compensate for wire and electronic delays (9bits / 1ns step => 500ns).

3 time counter start sources are available (logical OR): software (CMD register: "uclk" bit), VXI TTLTRG STOP/GO* line or front panel NIM input (SCLK).

Some channels of subtagging could be necessary inside a coupled detector acquisition subsystem. It is possible in that case to use the local tagging inputs of the slave CENTRUM from that acquisition, and to get the different time values by VME readout. It must be noted that the time counter is incremented by the slave board 100 MHz TCXO. This must be correlated with the time value received from the master CENTRUM through the slave RX channel. In any case, there will be no data output through the TX$_n$ output connectors on a slave module.

1.1.3 Timer

One timer with a preload register (48 bits) is also included in the module. This one works in parallel with the universal clock counter and is started at the same moment as discribed above. At the time-out, a bit is set for polling (STATUS register) or a VME interrupt (IRQ1..7) is generated if enabled.

1.1.3 Event Counter

A 32 bit counter is clocked by a TTLTRG backplane signal (VAL3 for example) or via a front panel NIM input (CKEVT).

The counter is incremented with the back edge of this signal and a comparison will be made on the front edge to check the synchronisation with EXOGAM event number (4 lsb's available on the VXI P2 connector) in the case of coupling with this equipment. When the module is slave ("rx" bit set), any event number readout perfomed in that module depends on the value received through the RX channel from the master CENTRUM (internal event counter disabled).

1.2 Front panel serial links

5 transmission channels (TX1..5) are controlled directly by the "link ports" of the DSP (ADSP-21062 / Analog Devices). 2 other channels (TX6..7) are controlled by the "serial ports" of the DSP and programmable logic.

The first channels (TX1..5) will be used for high speed (f_{dsp}) short distance (20-30 m) transfer and the last channels (TX6..7) will have programmable transfer frequency to provide valid data for link up to 100 meters.

The channel Ø is the receiver input (RX) when the module is configured for that purpose.This input channel use also a DSP "link port" on the receiver board but the transfer frequency depends of the master CENTRUM TX channel used (TX1..5 or TX6..7).

The PCB connectors used are stacked 2x15 points MDSM connectors from ITT-Cannon (MDSM-30PE-Z10-VR22). They have good EMI shielding and are especially designed to save space on VME/VXI front panels. The cable used (shielded twisted pair) and the cable connectors are also supplied by ITT-Cannon.

Each TX serial link carrying differential ECL signals has 7 twisted pairs used as follows:

- LCLK (out)

- LDATA<3..0> (out)
- RTAGn (in)
- LACK (in)

The information transmitted on channel n will be 96 bits:
- 1 x 48 bits data word (channel n clock value)
- 1 x 32 bits data word (current event number)
- 1 x 16 bits control word

A 16 pin auxiliary output connector (diff. ECL) using the same signals as serial links (except RTAG) could be used with standard ribbon cable to interface one other module (VXI module, VME board with SHARC PMC ...). This connector and its pinout is the same as the one used to send the EXOGAM single events information.

1.3 Data readout

1.3.1 VME readout

All the informations will be readable in 2 modes by the VME backplane:
- single cycle
- DT32 or GANIL block tranfer.

In single cycle mode, the full time stamp information for one channel will be obtained by 2 VME long word read (32 bits).

For the block transfer, every time stamp data (48 bits) and event number value (32 bits) will be split in 16 bit data words, each associated with a 14 bit label, an error bit (EXOGAM coupling) and an "end of block" bit. All this forms a maximum format of 26 x 32 bits data word block.

1.3.2 Serial links readout

Data will only be included in event by event readout when there is an event in the system where the clock module is located. However, data can be generated (by the transmitter clock module) every time the event number is incremented and then stored locally in the VME readout register of the receiver module used for that channel. The selection of this "send always" mode is controlled by software in the clock transmitter

module. The alternative is "send only when hit" mode which relies on receiving a Tag input before putting data in the receiver buffer.

The "send always" mode makes data merging in the event builder considerably simpler because all input data streams have a complete sequence of event numbers with no gaps. "send only when hit" mode produce less data but requires a more complex search through input data buffers due to the gaps in the event number sequence. It is inherently less secure in that there is no way to distinguish between an event missing because of an error and an event that never existed for physics reasons.

1.4 Visualization

The last NIM output signals "TEST1" and "TEST2" (LEMOØØ) will be used to control the exact timing of the tagging inputs, to view other internal signals on a scope or to trigger other module's inputs.

1.5 Indicators

Four LED's are implemented at the top of the front panel to indicate that data transfers are in progress between modules (RX - TX1-7) and also to give DSP status plus Test (calibration) status.

1.6 Calibration

For the moment, calibration, especially for remote tagging (serial cable), will be made manually by connecting the RX channel input to one of the TX output using the RTAG, LTAG inputs, TEST outputs and an oscilloscope. In a second step an automatic calibration, made by the DSP will be designed.

Chapter 2 : I/O Signals

2.1 Front panel inputs

LEMO 00: NIM level (-800 mV on 50 ?)

RTAG Remote TAGging

Description:

Input signal that could be used in a receiver module to tag an input of the remote transmitter via a differential twisted pair of the serial cable.

LTAG 1..7 Local TAGging

Description:

Input signals that are used to transfer the clock counter value to the corresponding channel time register (master or slave CENTRUM).

CKEVT CKEVenT

Description:

Signal used to increment the internal event counter when the module is configured only as a transmitter (master CENTRUM) if the backplane signal (VALIDATION*) is not used.

SCLK Start CLocK

Description:

Signal used to start the clock counter when the module is configured as a transmitter if the backplane signal (STOP/GO*) is not used.

15 pins connectors :

RX Receive data

Description:

This serial input is used to get data from the CENTRUM transmitter.

Logic levels

Differential ECL.

2.2 Front panel outputs

15 pins connectors :

TX 1..7 Transmit data 1..7

Description:

These serial outputs are used to connect one transmitter module to seven receivers modules.

Logic levels

Differential ECL.

16 pins connector :

AUX. AUXiliary connector

Description:

This connector is a general purpose output. When the module is configured as a transmitter, it supplies the TX1 information (serial link). In the other case (receiver module), this output repeats the "RX" information. This link could be useful to distribute the CENTRUM information to local electronics through this standard connector.

Logic levels

Differential ECL.

LEMO 00 connector: NIM level (-800 mV on 50 ?)

TEST1 and 2

Description:

TEST1 and TEST2 are used for timing control (calibration) or to output some CENTRUM internal signals for other instrumentation modules.

2.3 VXI bus signals

2.3.1 TTLTRG lines

Logic levels

TTL, 0 V when asserted.

CODing*

Description:

This line is asserted when VALIDATION* is received to indicate that the module is working on data and that these are not available for the moment.

CODing* could be assigned to any VXI TTLTRG bus line.

READout*

Description:

This line is asserted when CODING* is deasserted if valid data are ready for a VME backplane readout.

READout* could be assigned to any VXI TTLTRG bus line.

INIT* INITialisation

Description:

This line when asserted initializes and clears the module.

INIT* could be assigned to any VXI TTLTRG bus line.

STOP/GO*

Description:

If this line is used (i.e. assigned to any VXI TTLTRG bus line), the clock counter is incremented by the 100 MHz internal TCXO when this line is in the GO* state (asserted).

MRST* Master ReSeT

Description:

When asserted, this line clears the module.

MRST* could be assigned to any VXI TTLTRG bus line.

VAL* VALidation

Description:

This line is used mainly for the event counter as explained § 1.1.3.

VALIDATION* could be assigned to any VXI TTLTRG bus line.

2.3.2 Local Bus Lines (LBUSA/C)

The "local bus signals" (P2/LBUSA-LBUSC) could be transmitted out of the module (right or/and left) or terminated by a resistor network (VXI VXSTATUS register).

LI Logical Inspection LBUS09 (P2-AC18)

Description:

This line is used to carry logical signals between the new VXI-C GANIL modules (trigger: GMT-U2M and converters). This line will be not available when coupling with EXOGAM electronics is used.

Logic levels

ECL.

EVT 1..4 EVenT number bits 1..4 LBUS08..11 (P2-AC17,AC18,AC20,AC21)

Description:

The CENTRUM module reads these four lsb's broadcast by the EXOGAM trigger to check the synchronisation with its own event counter.

Logic levels

ECL.

REN*in/out Readout ENable input/output LBUS04 (P2-AC11)

Description:

This line controls the daisy-chain for the DT32 and GANIL readout protocol .

Logic levels

TTL, 0 V when asserted.

Chapter 3 : The CENTRUM registers

3.1 VXI Registers A16/D16

A16 addressing format :

Address

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	Logical Address (1 per module)								Add16					

Add16 : A16 address space (64 Bytes)

3.1.1 Addressing and identification

VXID *R* *SYSRESET = 0xCF5A* *Add16 = 0x00*

ID Register (VXI specification).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Dev Class		Add Space		MANUFACTURER ID: IN2P3 = 0xF5A											

Add Space = 00 : A16 et A24 addressing mode
= 01 : A16 et A32 addressing mode

Dev Class = 11 : "REGISTER BASED" module

VXLOGADD *W* *Add16 = 0x00*

LOGICAL ADDRESS Register (VXI specification).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	Dynamic configuration logical address							

VXDEVTYP *R* *SYSRESET = 0x7750* *Add16 = 0x02*

DEVICE TYPE Register (VXI specification).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
REQUIRED MEMORY				MODEL CODE = 0x750											

REQUIRED MEMORY = 0x0010 A24 mode => 2Mbytes (VXI spec.)
= 0x1010 A32 mode => 2Mbytes (VXI spec.)

VXSTATUS *R* *SYSRESET = 0x63EF* *Add16 = 0x04*

STATUS Register (VXI specification).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
AA	M*	A24	ETB	X	X	WM*	ZM*	LBG	LBD	WP	X	1	1	1	1

WP = 0 : no write protection of setup registers when the module is running

= 1: WP is on, no change of setup registers when the module is running.

LBG:LBD = 00 : local bus transmitted on the right and left (not terminated)

LBG:LBD = 01 : local bus terminated on the right

LBG:LBD = 10 : local bus terminated on the left

LBG:LBD = 11 : isolated (no connection)

ZM* : individual initialization* of the module

WM* : individual work* bit for the module

ETB = 0 : VXI TTLTRG lines connected to the VXI backplane

= 1 : VXI TTLTRG lines disconnected

A24 = 1 : A24 addressing mode selected (=0 if A32 mode)

M* : VXI MODID line status

AA = 0 : A24 or A32 access disabled

= 1 : A24 or A32 access enabled

VXCONTRL *W* *Add16 = 0x04*

CONTROL Register (VXI specification).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
AA	X	A24	ETB	X	X	WM*	ZM*	LBG	LBD	WP	X	X	X	X	X

WP, LBD, LBG, ZM*, WM*, ETB, A24, AA are control bits verified in the VXSTATUS register.

VXOFFSET *R / W* *SYSRESET = 0x0* *Add16 = 0x06*

OFFSET Register (VXI specification).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A24 & A32 offset			A32 offset								X	X	X	X	X

A24 Offset (bits 13 to 15) is used for VME address (A21 to A23) decoding

A32 Offset (bits 05 to 15) is used for VME address (A21 to A31) decoding

VXSERNUM *R* *Add16 = 0x08*

SERIAL NUMBER Register (IN2P3 specification).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	Module serial number							

VXMODLVL *R* *Add6 = 0x0A*

MODIFICATION LEVEL Register (IN2P3 specification).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	Module modification level							

3.1.2 Control signals allocation

TTLTRG0-7 lines allocation:

For these six registers, the data is defined as follow:

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ON	X	X	X	X	X	X	X	X	X	X	X	X	TTL Add		

TTL Add = 0 : signal addressed to the line TTLTRG0 (P2A23)
= 1 : signal addressed to the line TTLTRG1 (P2C23)
= 2 : signal addressed to the line TTLTRG2 (P2A24)
= 3 : signal addressed to the line TTLTRG3 (P2C24)
= 4 : signal addressed to the line TTLTRG4 (P2A26)
= 5 : signal addressed to the line TTLTRG5 (P2C26)
= 6 : signal addressed to the line TTLTRG6 (P2A27)
= 7 : signal addressed to the line TTLTRG7 (P2C27)

ON = 0 : signal defined by the register but not connected to the VXI bus
= 1 : signal connected to the line TTLTRGn addressed by TTL Add

VXCODING *R / W* *SYSRESET = 0x0* *Add16 = 0x20*

Allocation register for the CODing* signal.

VXREADOUT *R / W* *SYSRESET = 0x0* *Add16 = 0x22*

Allocation register for the READout* signal.

VXINIT *R / W* *SYSRESET = 0x0* *Add16 = 0x24*

Allocation register for the INIT* signal.

VXGO *R / W* *SYSRESET = 0x0* *Add16 = 0x26*

Allocation register for the GO* signal.

VXMRST *R / W* *SYSRESET = 0x0* *Add16 = 0x28*

Allocation register for the MRST* signal.

VXVAL *R / W* *SYSRESET = 0x0* *Add16 = 0x2A*

Allocation register for the VALIDATION* signal.

3.1.3 Interrupt allocation

EXERR_IT *R / W* *SYSRESET = 0x0* *Adr16 = 0x34*

Event number error interrupt register (EXOGAM coupling).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	IRQi			vect							

vect : interrupt vector

IRQi : interrupt request level : 1 to 7 (VME IRQ1*-IRQ7* lines used)

TOUT_IT *R / W* *SYSRESET = 0x0* *Adr16 = 0x36*

Time-out interrupt register.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	IRQi			vect							

vect : interrupt vector

IRQi : interrupt request level : 1 to 7 (VME IRQ1*-IRQ7* lines used)

3.2 A24/A32 Registers

The access to these registers is made with A24 or A32 addressing modes and D16 or D32 data tranfers.

For the module initialisation, the write enable of the setup registers is internally asserted when the module is in the "STOP" state. However it is possible to enable the access to these registers regardless of the module's state by clearing the WP bit of the VXSTATUS register (by default WP=1).

Warning: the WP bit acts as a data register protection to avoid troubles when the module works (WM*=Ø), but any VME write cycle to these registers ends normally (VME DTACK*)

The general RUN/STOP state of the CENTRUM module depends only of the WM* bit setup (VXCONTRL register).

3.2.1 General configuration registers

CONFIG *R / W* *SYSRESET/Init = 0x0* *Add = 0x0000*

CENTRUM general configuration register.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	dtf	dt32	zs	cali	tie	exie	ten	exo

exo = 0 : the module works without the EXOGAM electronic

= 1 : the EXOGAM electronic is part of the acquisition system

ten = 0 : timer disabled

= 1 : timer enabled

exie = 0 : EXOGAM error interrupt disabled

= 1 : EXOGAM error interrupt enabled

tie = 0 : timer interrupt disabled

= 1 : timer interrupt enabled

cali = 0 : calibration disabled

= 1 : calibration enabled

zs = 0 : zero data suppression off (GANIL or DT32 block mode)

= 1 : zero data suppression on (GANIL or DT32 block mode)

dt32 = 0 : GANIL block mode readout selected

= 1 : DT32 block mode readout selected

dtf = 0 : slave CENTRUM connected to TX1-5 of a master CENTRUM

= 1 : slave CENTRUM connected to TX6-7 of a master CENTRUM

MASK *R / W* *SYSRESET/Init = 0x0* *Add = 0x0002*

CENTRUM mask register.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	tx7	tx6	tx5	tx4	tx3	tx2	tx1	rx

rx = 0 : receiver channel off

= 1 : receiver channel on

tx_n = 0 : transmitter $channel_n$ off

= 1 : transmitter $channel_n$ on

TXMODE *R / W* *SYSRESET/Init = 0x0* *Add = 0x0004*

CENTRUM data transmission mode register.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	sa7	sa6	sa5	sa4	sa3	sa2	sa1	X	cor7	cor6	cor5	cor4	cor3	cor2	cor1

cor_n : correlated channel bit (events controlled by the event counter)

cor = 0 : single channel (no correlation, only the time information is necessary)

= 1 : correlated channel

sa_n : send always bit (used only with the correlated channels)

= 0 : the complete bit stream is sent only if the tag pulse is received

= 1 : the complete bit stream is sent over the serial line in any case

LOADCLKL *R / W* *SYSRESET/Init = 0x0* *Add = 0x0006*

Clock counter preload register low

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

LOADCLKM *R / W* *SYSRESET/Init = 0x0* *Add = 0x0008*

Clock counter preload register middle

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
middle word <31..16>															

LOADCLKH *R / W* *SYSRESET/Init = 0x0* *Add = 0x000A*

Clock counter preload register high

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

LOADTIL *R / W* *SYSRESET/Init = 0x0* *Add = 0x000C*

Timer preload register low

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

LOADTIM *R / W* *SYSRESET/Init = 0x0* *Add = 0x000E*

Timer preload register middle

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
middle word <31..16>															

LOADTIH *R / W* *SYSRESET/Init = 0x0* *Add = 0x0010*

Timer preload register high

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

DELTAG1 *R / W* *SYSRESET/Init = 0x0* *Add = 0x0012*

Channel 1 delay register for TAG1 input pulse (remote or local).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	delay								

delay<8..0> : 0 to 511 ns (1ns step)

DELTAG2 *R / W* *SYSRESET/Init = 0x0* *Add = 0x0014*

Channel 2 delay register for TAG2 input pulse (remote or local).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	delay								

delay<8..0> : 0 to 511 ns (1ns step)

DELTAG3 *R / W* *SYSRESET/Init = 0x0* *Add = 0x0016*

Channel 3 delay register for TAG3 input pulse (remote or local).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	delay								

delay<8..0> : 0 to 511 ns (1ns step)

DELTAG4 *R / W* *SYSRESET/Init = 0x0* *Add = 0x0018*

Channel 4 delay register for TAG4 input pulse (remote or local).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	delay								

delay<8..0> : 0 to 511 ns (1ns step)

DELTAG5 *R / W* *SYSRESET/Init = 0x0* *Add = 0x001A*

Channel 5 delay register for TAG5 input pulse (remote or local).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	delay								

delay<8..0> : 0 to 511 ns (1ns step)

DELTAG6 *R / W* *SYSRESET/Init = 0x0* *Add = 0x001C*

Channel 6 delay register for TAG6 input pulse (remote or local).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	delay								

delay<8..0> : 0 to 511 ns (1ns step)

DELTAG7 *R / W* *SYSRESET/Init = 0x0* *Add = 0x001E*

Channel 7 delay register for TAG7 input pulse (remote or local).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	delay								

delay<8..0> : 0 to 511 ns (1ns step)

LABEL *R / W* *SYSRESET = 0x0* *Add = 0x0100 à 0x0132*

Data label register for compression mode.

Address

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	1	0	0	add data					0

add $data_{hex}$: 0 to 1 : low and high word event number label address

2 to 4 : low, medium and high word time value label address (RX)

5 to 7 : low, medium and high word time value label address (TX1)
8 to A : low, medium and high word time value label address (TX2)
B to D : low, medium and high word time value label address (TX3)
E to 10 : low, medium and high word time value label address (TX4)
11 to 13 : low, medium and high word time value label address (TX5)
14 to 16 : low, medium and high word time value label address (TX6)
17 to 19 : low, medium and high word time value label address (TX7)

Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A32 addressing								A32/A24 addressing			0	0	0	0	0

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
x	x	label													

3.2.2 Control/Status Register

CMD *R/W* *Add = 0x0020*

CENTRUM control register.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	uclk	pul2	pul1	rtout	rerr	ltim	lclk	rclk	evcr	reset

reset = 1 : CENTRUM software reset (CENTRUM data readout registers)
evcr = 1 : event counter software reset
rclk = 1 : universal clock counter software reset
lclk = 1 : load universal clock counter with the "LOADCLKH,.M,.L registers
ltim = 1 : load timer counter with the "LOADTIH,.M,.L registers
rerr = 1 : event number error reset (only with EXOGAM coupling)
rtout = 1 : time-out bit software reset
pul1 = 1 : pulse on TEST1 output
pul2 = 1 : pulse on TEST2 output
uclk = 0 : universal clock sofware enable off (stopped to the last value)
= 1 : universal clock software enable on (counting)

STATUS *R* *SYSRESET/Init = 0x0* *Add = 0x0022*

CENTRUM status register.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	X	X	tout	err	clks	read	ecod	scod

scod : start of internal coding (=1, CODing* asserted)

ecod : end of internal coding (=1, CODing* deasserted)

read : internal VXI READout signal : deasserted = 0, asserted = 1

clks : universal clock status : stopped = 0 ; running = 1

err : event number error (EXOGAM coupling) : = 1 if error

tout : time-out status bit : = 1 at the time-out

3.2.3 Test and Inspection Registers

TEST *R / W* *SYSRESET/Init = 0x0* *Add = 0x0024*

Register used to control the signal multiplexers of the CENTRUM front panel TEST1 and TEST2 outputs.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	test2					X	X	X	test1				

$visu_n$ = 0 : permanent NIM level 0 (0V)

= 1 : TAG1 (local or remote)

= 2 : TAG2 "

= 3 : TAG3 "

= 4 : TAG4 "

= 5 : TAG5 "

= 6 : TAG6 "

= 7 : TAG7 "

= 8 : RTAG

= 9 : RUN/STOP

= A : START CLOCK (STOP/GO* line or CMD "uclk" bit or SCLK input)

= B : VAL* or CKEVT

= C : internal CODING

= D : internal READOUT

= E : MRST*

= F : permanent NIM level 1 (-800mV)

= 10 : $PULSE_n$ (CENTRUM_CMD)

= 11 : -
= 12 : -
= 13 : -
= 14 : -
= 15 : LDTACK*
= 16 : LBERR*
= 17 : AS*
= 18 : WE*
= 19 : LWORD*
= 1A : IACK*
= 1B : DS0*
= 1C : DS1*
= 1D : DTACK*
= 1E : BERR*
= 1F : LI (reflect the VXI Logical Inspection line state)

LOGINSP *R / W* *SYSRESET/Init = 0x0* *Add = 0x0026*

Register used to control the signal multiplexer of the VXI bus LI line.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
on	X	X	X	X	X	X	X	X	X	X	X	sig			

sig = 0 : CKEVT
= 1 : TAG1 (local or remote)
= 2 : TAG2 "
= 3 : TAG3 "
= 4 : TAG4 "
= 5 : TAG5 "
= 6 : TAG6 "
= 7 : TAG7 "
= 8 : RUN/STOP
= 9 : CODING interne
= A : READOUT interne
= B : -
= C : -
= D : -
= E : -
= F : -
on = 1 : signal "sig" connected to the VXI LI line

3.2.4 Readout Registers

EVCNT *R* *SYSRESET/Init/Raz= 0x0* *Add = 0x0030*

Event counter value (current 32 bits event number).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
event number low															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
event number high															

TIMEMLØ *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0044*

Readout register for low and middle word time value of channel 0 (RX) used for addressed backplane access when that receiver channel is used (MASK register "rx" bit=1).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
middle word <31..16>															

TIMEHØ *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0040*

Readout register for the high word time value of channel 0 (RX) used for addressed backplane access when that receiver channel is used (MASK register "rx" bit=1).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ØØ															

TIMEML1 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x004C*

Readout register for low and middle word time value of channel 1 (TX1) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
middle word <31..16>															

TIMEH1 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0048*

Readout register for high word time value of channel 1 (TX1) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ØØ															

TIMEML2 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0054*

Readout register for low and middle word time value of channel 2 (TX2) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
middle word <31..16>															

TIMEH2 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0050*

Readout register for high word time value of channel 2 (TX2) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ØØ															

TIMEML3 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x005C*

Readout register for low and middle word time value of channel 3 (TX) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
middle word <31..16>															

TIMEH3 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0058*

Readout register for high word time value of channel 3 (TX3) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ØØ															

TIMEML4 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0064*

Readout register for low and middle word time value of channel 4 (TX4) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
middle word <31..16>															

TIMEH4 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0060*

Readout register for high word time value of channel 4 (TX4) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ØØ															

TIMEML5 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x006C*

Readout register for low and middle word time value of channel 5 (TX5) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
middle word <31..16>															

TIMEH5 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0068*

Readout register for high word time value of channel 5 (TX5) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ØØ															

TIMEML6 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0074*

Readout register for low and middle word time value of channel 6 (TX6) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
middle word <31..16>															

TIMEH6 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0070*

Readout register for high word time value of channel 6 (TX6) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ØØ															

TIMEML7 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x007C*

Readout register for low and middle word time value of channel 7 (TX7) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
low word <15..0>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
middle word <31..16>															

TIMEH7 *R* *SYSRESET/Init/Raz = 0x0* *Add = 0x0078*

Readout register for high word time value of channel 7 (TX7) used for addressed backplane access.

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
high word <47..32>															

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ØØ															

DATA *R* *SYSRESET/Init/Raz = 0xFFFFFFFF* *Add = 0x0080*

Data register (fifo) used to read in block mode (GANIL or DT32) the 8 channel 48 bits time values and the 32 bits current event number. All the informations are split in 16 bits data words, each identified by a 14 bit label. The end of block is indicated by the msb bit set in the last 32 bits data. An error bit (D<30>) is set in this last long word in case of event number error (EXOGAM coupling only).

Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Data															

Data

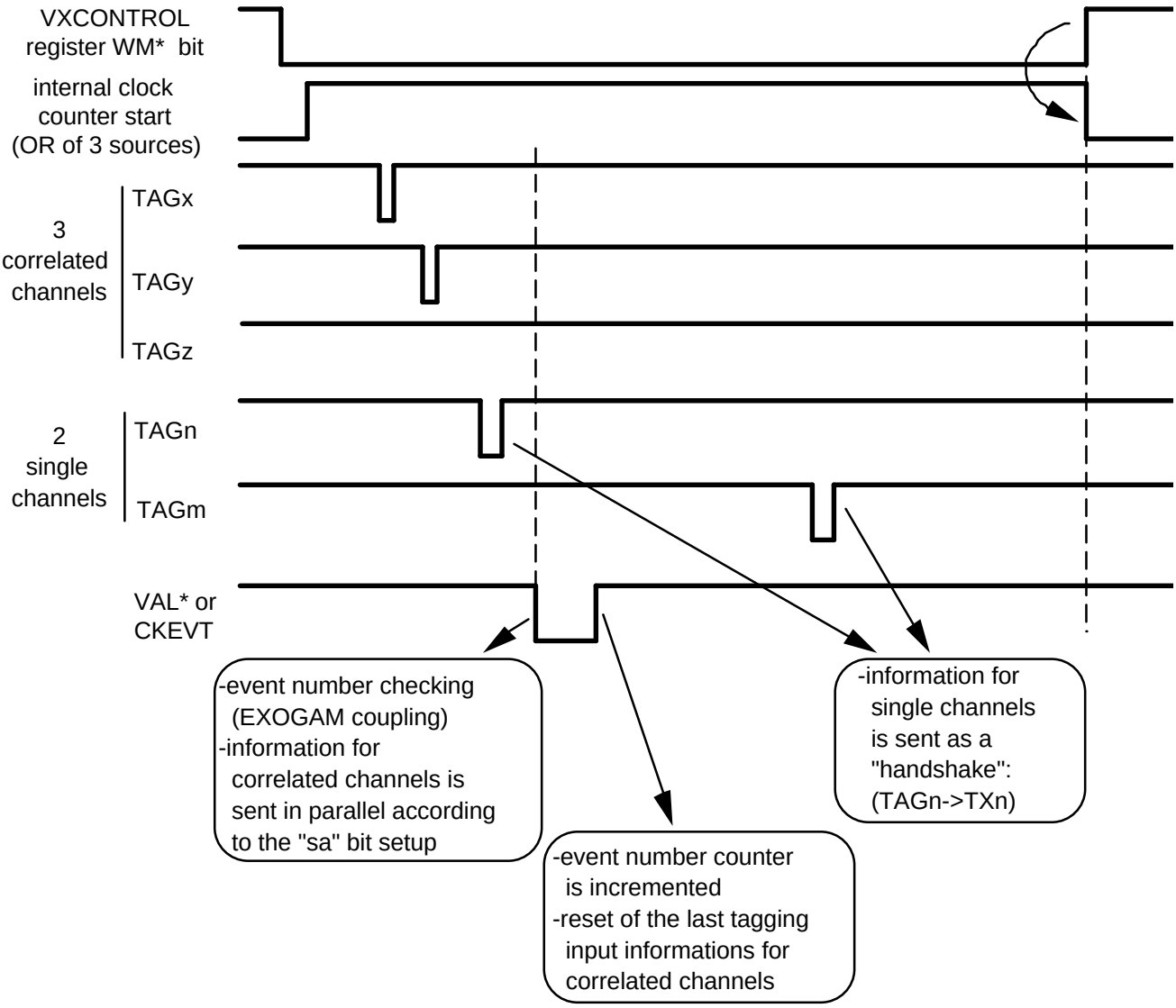
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
end	err	label													

label : defined in the LABEL registers

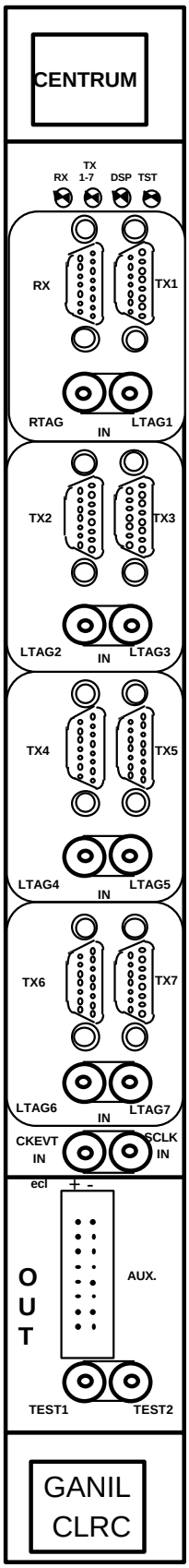
err = 1 : event number error (EXOGAM coupling only)

end = 1 : end of block

Appendix 1 : Timing diagram



Appendix 2 : CENTRUM front panel



VXI-C