

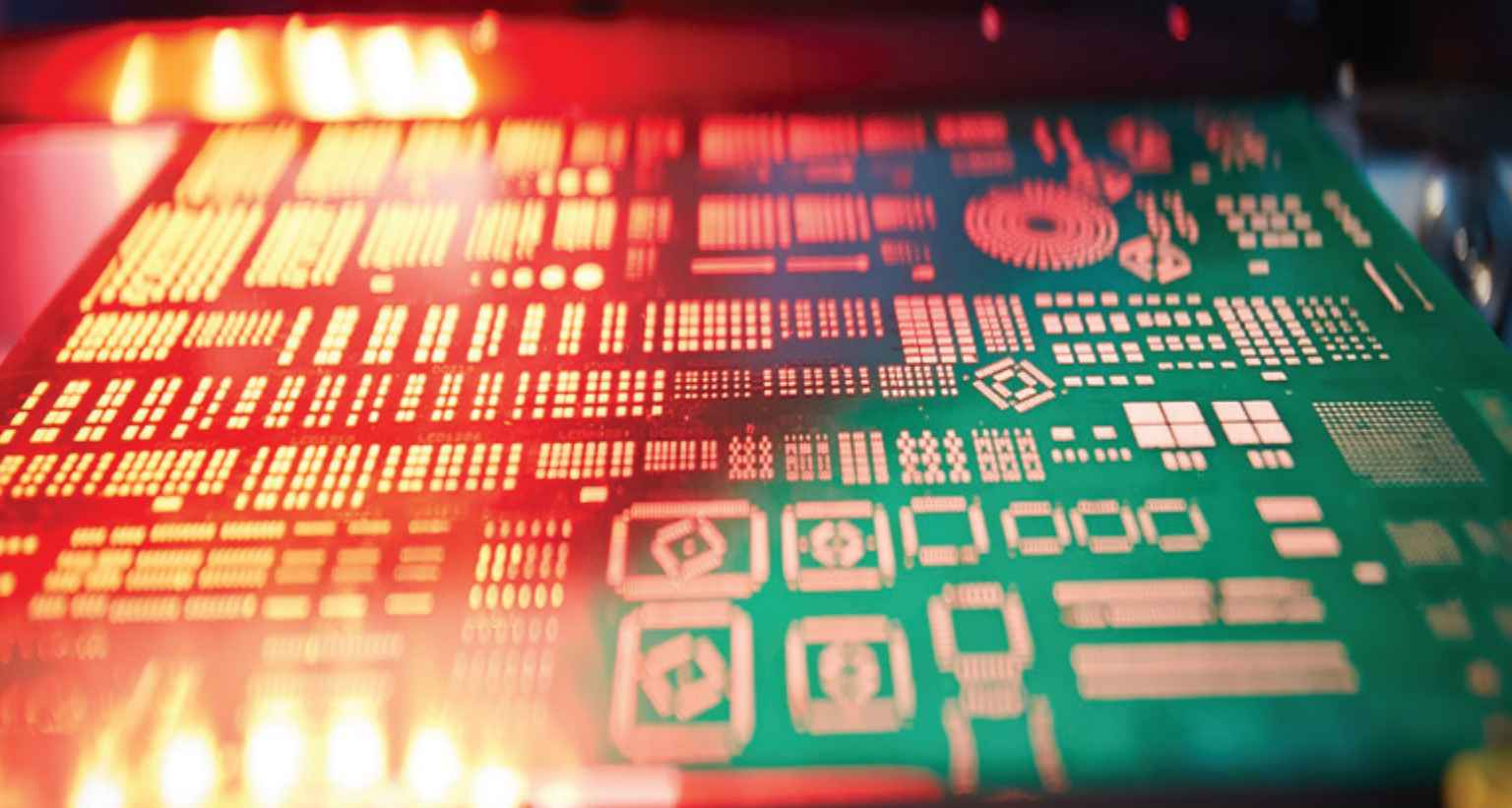
PRINTED CIRCUIT DESIGN & FAB

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November 2019

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for Tiny Parts



- Additive Manufacturing
- Through-Hole Fill Levels
- Board Support



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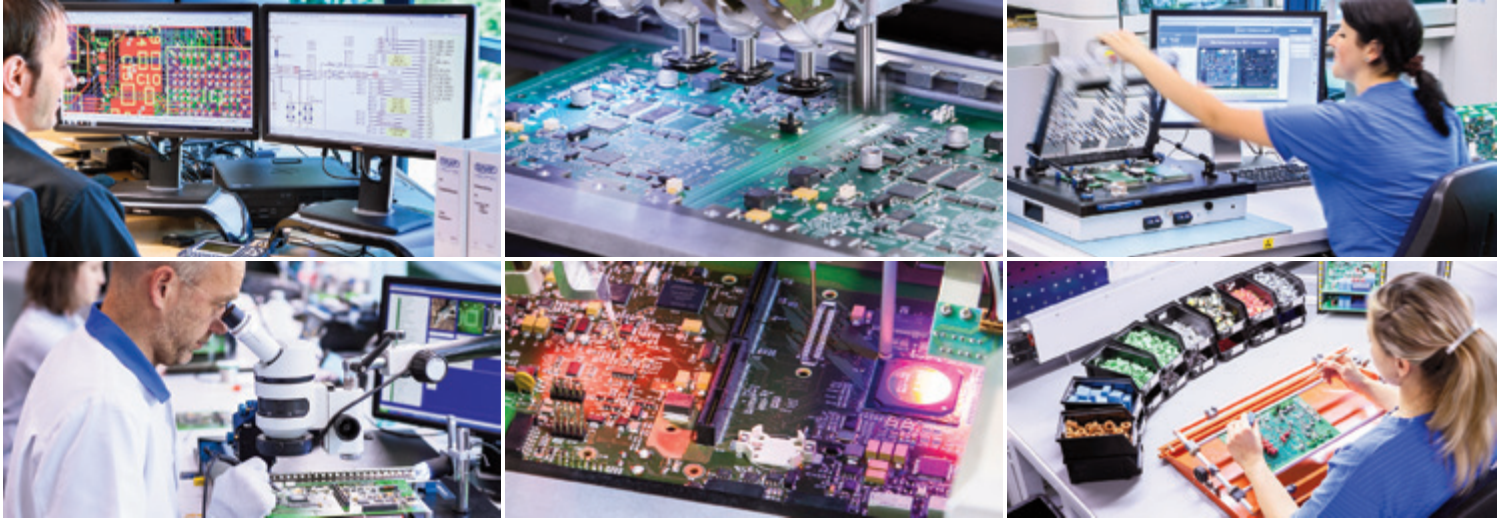
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Austrian Manufacturing Experts Rate XJTAG® as Top Boundary Scan System

“Graf Elektronik, an Electronic Manufacturing Services provider in the Lake Constance region joining Switzerland, Germany and Austria, worked with a client to identify the best boundary scan test platform to achieve mutual objectives. The evaluation rated XJTAG as number one for user friendliness, features and value for money.”

Graf Elektronik specialises in electronics development and electronics manufacturing services, and has clients across the industrial, medical, and consumer-products sectors. Its service portfolio includes project management, hardware development, software development, mechanical design, circuit-board assembly, test engineering and production-line testing, painting, potting, and box-build ready for sale.

Recently, the company’s engineers worked with a client that serves the electrical power industry with innovative products and services for testing, diagnostics and monitoring of protection circuits. The objectives were to increase test coverage and raise productivity when building the client’s power-testing equipment, augmenting Automatic Optical Inspection (AOI) and In-Circuit Testing (ICT) with JTAG boundary scan testing.

During the evaluation, engineers from Graf Elektronik and the client company carefully compared the support, software, hardware, functionality, and the cost of boundary scan systems from several well-known vendors. This rigorous comparison examined both the development and run-time environments of the leading platforms, as the two partners intended to use both environments to develop and execute tests.

“XJTAG was by far the most user-friendly of the systems we evaluated, yet its superior ease of use did not

come at the expense of features,” says Marcél Ströhle, Testing Coordinator, Graf Elektronik. “We found XJTAG to have the most intuitive workflow while offering a very competitive price. XJTAG also gives us the ability to rapidly develop and deploy new tests.”

Graf Elektronik is also supplying their client with the boundary scan tests originally developed for use in production. This way the company can use XJTAG’s XJRunner run-time

environment in-house to speed up analysis of any returned units.

Marcél Ströhle and the engineering team at Graf Elektronik are using XJTAG to check bus interfaces between various chips, DSPs, FPGAs and other complex ICs. “The ability to test DDR2 and DDR3 RAM connections without functional testing is incredibly helpful, and checking connectors through external boards significantly increases our typical test coverage of digital circuits,” he explains.

He highlights XJTAG tools like the Layout Viewer and XJAnalyser as being especially powerful. Layout Viewer helps the user find the physical location of components, nets and pins on a board, and to visualise any faults

that are found when running tests. XJAnalyser enables the user to set pin values and trace signals, and so debug boards quickly. It can also be used to program devices, thereby saving expenditure on other download tools.

Marcél Ströhle goes on to explain how XJTAG also helps engineers identify unusual defects that are invisible to AOI and cannot be pinpointed using ICT. “We successfully created custom tests that enabled us to trace some unexpected faults back to a bad batch of ICs,” he adds. “Developing new tests is very easy, since the user interface is more intuitive than the other systems we evaluated, and a lot of pre-packaged tests are available online to help us get powerful tests up and running quickly.”

opinion

Marcél Ströhle
Testing Coordinator
Graf Elektronik

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Data Bank	
Company	Graf Elektronik GmbH (Part of Graf Group, Austria)
Nature of business	One of the leading Electronics Manufacturing Services providers for OEMs in Austria
Main product	Full service from development to testing and volume production of certified electronic assemblies and devices
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Incorporated	1989
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No dice for “chiplets.”

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by MIGUEL ARROYO COLOMER

IN THE DIGITAL EDITION**The Digital Route**

The latest happenings among the IPC Designers Council chapters.

by STEPHEN CHAVEZ

ON PCB CHAT (pcbchat.com)**All-Silicon Die Connection**

with PUNEET GUPTA, PH.D.

SMT Solder Paste Printing

with KAY PARKER

New ECAD SI/PI Tools

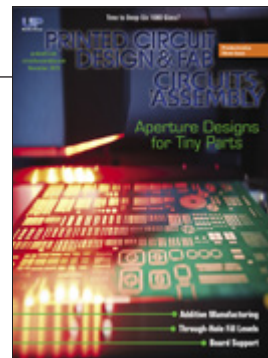
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What Happens to the Stainless-Steel Dust from Low-Cost, Short-Life Metal Squeegees?

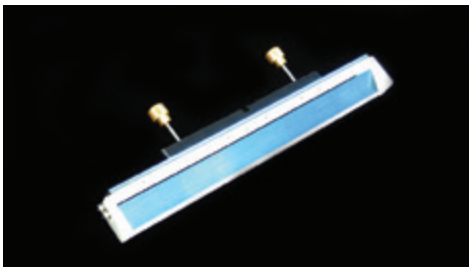


- **Contamination Issues**
- **Detrimental to SMT Assemblies**

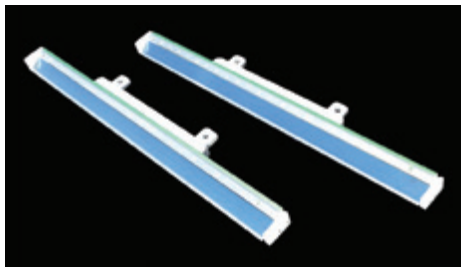
Dust piles from low-cost
stainless-steel blades

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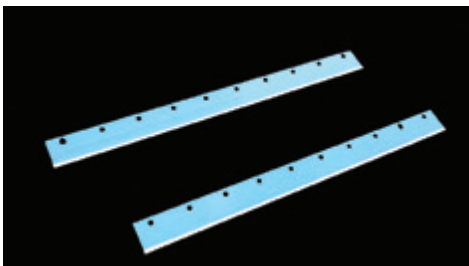
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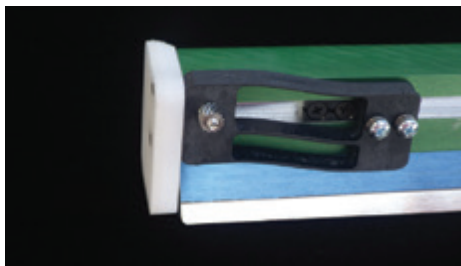
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PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by UP Media Group Inc., PO Box 470 Canton, GA 30169. ISSN 1939-5442. GST 124513185/ Agreement #1419617.

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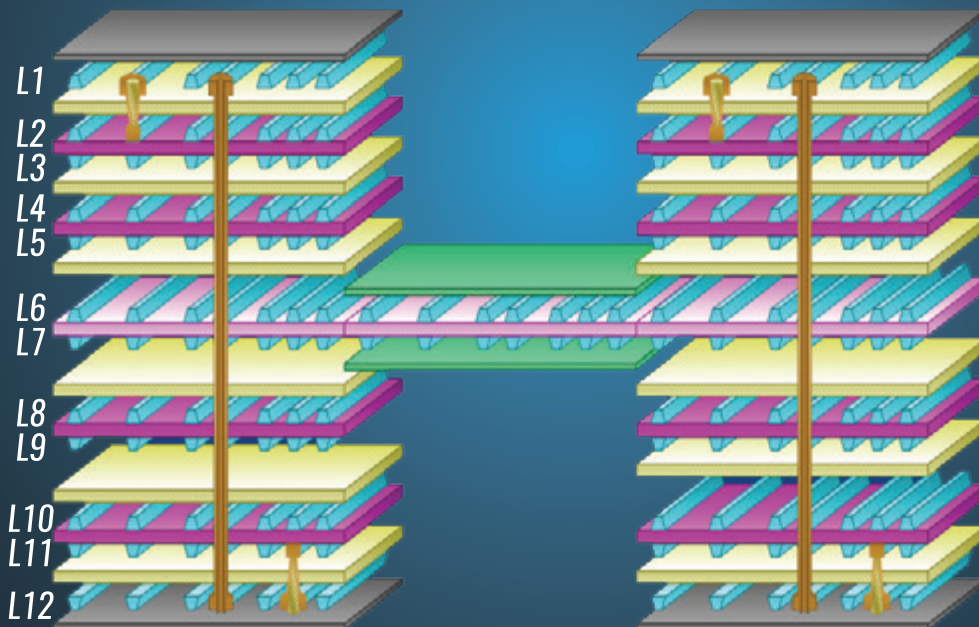


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MIKE
BUETOW
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No Dice on 'Chiplets'

WHEN I first started in electronics back in 1991, through-hole was still dominant and SMT was just taking hold. It wasn't long after, however, when we began hearing about multichip modules, or MCMs. Conferences sprung up, publishers dedicated entire issues to the subject, and trade groups started writing standards.

And then ... not much. MCMs never became the dominant packaging style some analysts predicted.

But will they?

When the Semiconductor Industry Association ceased its roadmapping activities, a host of organizations, including IEEE, SEMI, ASME and others, jumped in. Last month, they launched the second edition of the *Heterogeneous Integration Roadmap*. Heterogeneous integration refers to the integration of separately manufactured components into a higher-level assembly (SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics.

Or, as Dick Otte and Phil Marcoux wrote in this magazine in August ("Interconnects Drive Heterogeneous Assembly and Substrate Options"), "heterogeneous is the latest branding effort to promote the assembly of dissimilar electronic components. In the past these could be called *multichip modules* [it's mine], 2.5-D, 3-D and – really going back – 'hybrid' assemblies."

Multichip modules.

For the uninitiated, an MCM consists of multiple ICs or dies integrated on a common substrate. The resulting module is treated for processing purposes as a single component.

The HIR is called a roadmap to the future of electronics, identifying technology requirements and potential solutions. The sponsoring organizations wanted to spur "pre-competitive collaboration" among industry, academia and government, in the hopes of speeding up progress. Not surprisingly, IEEE has promoted the use of heterogeneous assembly at its popular ECTC conference. PCB designers have traditionally eschewed die-level issues in favor of focusing on the package-to-board interconnection. Is there reason to think that might change?

At ECTC and in the HIR, the term chiplets has emerged as a technology in waiting. And, points out Jan Vardaman, our resident components packaging editor, chiplets are MCMs. The substrate for chiplets could be a wafer or an organic package. The die might be wire-bonded, but solder ball interconnect (aka flip chip) is more common, and hybrid bonding is emerging.

Work is ongoing in many centers. Besides some of the largest foundries, academia is taking a look. Teams of researchers at UCLA, led by Dr. Puneet Gupta and Dr.

Subramanian Iyer, have developed a silicon-to-silicon concept that uses nanoscale wires to directly connect bare chips right on the wafer. They claim their idea, which they call silicon-interconnect fabric, permits a far greater number of chip-to-chip connections capable of transmitting data at faster speeds, at lower power, and without all the excess heat. (Dr. Gupta explained the process on our PCB Chat podcast in October.) The twist here is use of copper pillars for solder attachment or thermo-compression bonding.

That designers could save on power and possibly depress heat should open some eyes. Chip and hardware designers have long been grappling with how to manage the heat inside these packages. What's far hairier is the notion the work of placing and soldering parts might not just become a die-level phenomenon, but it could be moved entirely upstream, eliminating the need for component assembly.

For that I turned back to Marcoux. He points out this is actually at least the third time MCMs have popped up as the technology of the future. And he allows chiplets are "attractive" from the IC perspective because it's "not optimum to fabricate all circuit functions on the same wafer using the same processes." For example, says Marcoux, "voltage regulators require different diffusions and oxide thicknesses than RAMs, etc. Analog functions are more optimum with bipolar compatible fab processes than digital processes."

According to Marcoux, three hurdles may conspire to prevent silicon as a chiplet array substrate from taking hold: 1) The cost of silicon far exceeds that of PCB materials; 2) adding more than two layers causes adhesion problems and thus yield issues, which can mean wider traces to promote adhesion, and wafer planarization and metal deposition pumping processes that truly inflate costs; and 3) interconnecting the wafer externally is complex and, in his words, "not cheap."

In the ongoing battle of silicon vs. package, the package always seems to win. PCB designers and contract assemblers can breathe easy.


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P.S. A big thanks to Koh Young and Chrys Shea for the cover image.



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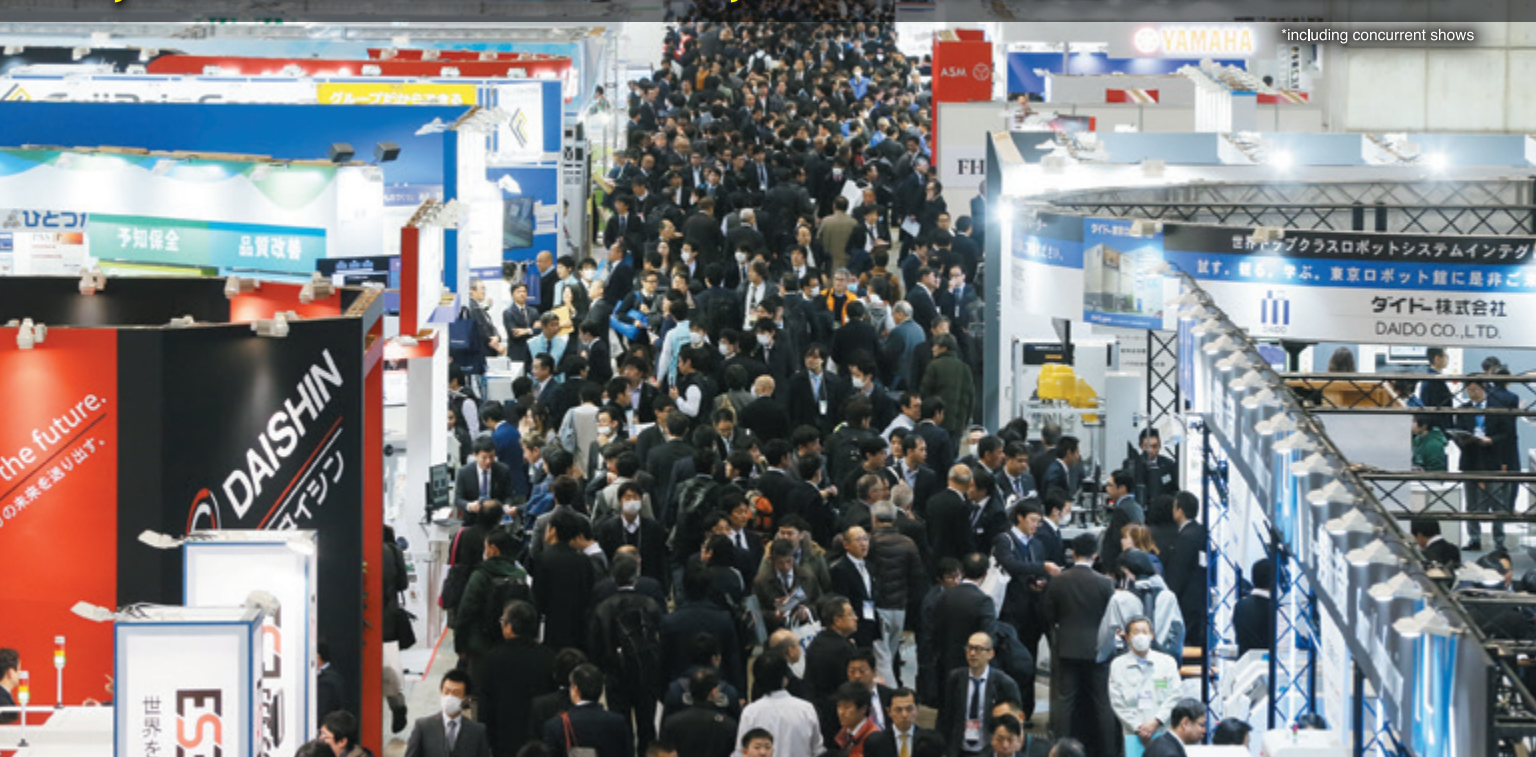
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PCD&F People



FTG named **Jamie Crichton** vice president and CFO. He has extensive experience in finance leadership roles within the aerospace and defense sector, including Nanowave Technologies, Raytheon and Spar Aerospace.

Nordcad Systems named **Allan Norgaard** senior application engineer.

PCD&F Briefs

Chunghwa Precision Test Tech will recruit 1,000 new employees for its new R&D headquarters to promote development of its ICT equipment.

Cicor installed an ENEPIG line at its fabrication site in Boudry, Switzerland.

DuPont Electronics & Imaging is undertaking a \$220 million capacity expansion of its Circleville, OH, plant, where it makes Kapton polyimide film and Pyralux flexible circuit materials. DuPont anticipates production will be operational by 2021.

DuPont Interconnect Solutions named as chemistry product distributors **East Coast Electronic Materials Supply (ECEMS)** for the Eastern US and Canada and **Tritek** for the Western US and Canada.

ECIA released *EIA-979, RF Transmission Line and Connector Selection Guide*.

Nano Dimension sold an additional DragonFly system to an undisclosed branch of the US Armed Forces.

Ohmega filed provisional patents for two new OhmegaPly designs: a macro tuning technique for embedded resistor elements and a split trace thin film fractional resistor.

CA People



Critical Manufacturing named **Dave Trail** vice president, Electronics segment. He has more than 25 years' experience in electronics manufacturing equipment, processes and MES software.



Kurtz Ersa named **Justin Rohloff** field service engineer. He has 13 years' experience at Rockwell Automation as a process engineer technician.



KIC hired **Karl Pfluke** as regional sales manager for Eastern US and Canada. He has a degree in manufacturing engineering and is SMT process engineer certified.

Altair Acquires PCB CAD Tool Developer Polliwog

TROY, MI – Altair in October acquired EDA software developer Polliwog Co. for \$11 million in cash, subject to customary working capital adjustments, and an aggregate of 473,752 shares of stock valued at about \$48,000.

Altair develops PLM, modeling and simulation tools primarily for the high-performance computing sector. Polliwog expands Altair's portfolio for system-level engineering to the PCB design and analysis market. The products include a PCB modeler, simulation solvers and design verification tools. Polliwog's customers include Samsung and LG Electronics.

"The PollEx Modeler shares Altair's open system philosophy and integrates easily into customer environments that use any of the leading PCB design tools and deliver innovative and practical solutions, a perfect fit for what we call simulation-driven design," said James Scapa, chairman, chief executive and founder, Altair. "Polliwog's powerful PCB modeler and design verification tools allow EDA engineers at small and enterprise customers to collaborate at never-before-seen levels and greatly expands our HyperWorks solution portfolio."

Altair pursued Polliwog as part of a strategy to expand from its foundation of mechanical simulation software into areas of systems simulation and electromagnetics. Polliwog's PCB solvers and verification tools extend these capabilities, the firm added. – MB

UP Media Group Announces 15% Spike in PCB West Conference Registration

ATLANTA, GA – Conference attendance for PCB West 2019 was up 15% year-over-year, UP Media Group Inc. announced. Show organizers said the surge was tied to the now four-day conference, coupled with steady demand for the longer-form training sessions.

PCB West, the largest conference and exhibition for PCB design, fabrication and assembly in the Silicon Valley, featured 59 presentations, a third of which were at least 3.5 hours in length. "It started with the record number of abstracts submitted, which gave us the opportunity to be more selective than ever," said Mike Buetow, conference chairman. "Conference speakers were quick to notice the increase in attendance in their presentations."

The free sessions, which are not included in the conference registration, were also extremely popular, he added.

Comments from attendees were glowing, including: "I chose to come to PCB West to learn best design practices and I was not disappointed," and "Such good information. I will be spending the next few weeks digesting what was taught."

The one-day trade exhibition sold out all 110 booths for the eighth consecutive year, UPMG said. Exhibitors reported high lead counts and quality attendees. "We exhibit at multiple trade shows but by far PCB West is one of the best!" said Eriko Yamato, FaradFlex marketing manager, Oak-Mitsui Technologies. Added Joe Clark, cofounder, DownStream Technologies, "Great show. Many existing customers here and new prospects too."

PCB West 2020 will be held September 8-11 in Santa Clara, CA. The event includes a four-day technical conference and one-day exhibition, to be held at the Santa Clara (CA) Convention Center. – MB

Nano Dimension Presents Production-Grade Printed Capacitors for PCBs

NESS ZIONA, ISRAEL – Nano Dimension has developed 3-D printed capacitors using its DragonFly additive manufacturing system. These capacitors are embedded in the body of the additively manufactured PCBs, saving space and eliminating the need for assembly.

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MacDermid Alpha Electronics named **Steve Williamson** senior district sales manager.

Mercury Systems named **Scott Mazur** senior principal quality systems engineer.



MicroCare promoted **Joe Ng** (pictured) to operations manager, MicroCare Asia, and named **Eric Lie Sticklers** business manager, Asia.

Mirtec Europe named **David Bennett** managing director of Bentec to concentrate on Mirtec's two main European-controlled territories: UK and India.

Naprotek named **Paramjit Singh** senior director, engineering / QMS.



Sanmina named **Hartmut Liebel** chief executive, succeeding **Michael Clarke**. He most recently served as president and CEO of iQor, and previously spent over 10 years at Jabil.

SMTA announced **Kim Porter** has been selected as the winner of the 2019 Joann Stromberg Student Leadership Scholarship.

Such capacitors are primarily used to filter electrical noise and ripple voltage for a wide range of applications, including RF transmission lines, audio processing, radio reception and power circuit conditioning.

In internal testing, repeatability results show less than 1% variance, the company said. The technology uses the same dielectric and metal traces as in the additively manufactured PCB yielding capacitors with a capacitance range from 0.1nF to 3.2nF. The results are based on over 260 tests with 30 different additively manufactured capacitor dimensions.

By integrating capacitors using additive manufacturing, the entire capacitor and PCB are printed as a single job. This cuts fabrication time and avoids many challenges imposed by traditional production techniques, Nano Dimension said. – CD

Keynote, Mentor Teams Tackle Challenges Big and Small at SMTAI

ROSEMOUNT, IL – SMTA International kicked off in the Chicago suburbs in late September with a dazzling keynote and an innovative session on leadership.

The keynote was a story of humility and doggedness. Adam Steltzner, Ph.D., the JPL engineer who led development of the Mars Curiosity rover, juxtaposed the development of that machine against his own background, which took him from high-school dropout and hippy musician to finishing first in his class in engineering at University of California, Davis. "Curiosity is our species' superpower," he told a rapt SRO audience. His team had to resolve all kinds of challenges with heat, weight and foreign matter to deposit the one-ton rover on the surface of Mars. Steltzner's 45-minute narration was both self-deprecating and highly personal.

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A day earlier, the Women's Leadership Program spent a half-day tackling the often-thorny situations newly minted engineers and aspiring managers must navigate. Women make up about 20% of the roughly 100,000 bachelor's degrees awarded in engineering in the US, but despite the title, the program was applicable to any less experienced employee.

In a speed-dating style, a novel roundtable offered a chance to get insights from mentors on a variety of soft and hard topics, from managing peer pressure to managing one's own career path. Mentors included a mix of users and suppliers. While references to literature and business axioms abounded, the advice wasn't preachy. Instead, it felt truly bidirectional. Mentors asked questions as much as they offered advice. Most valuable were the strategies for how to manage the inherent tension between one's work and personal life. The general tone was light but thoughtful.

Much of the session was aimed at developing soft skills. For instance, Jennifer Bly of Intel counseled participants on how to deal with introverts and extroverts in the workplace, and when and where to assert oneself in the mix. "It's about being conscious of your personality type and those of the people around you," she said. "Say, for example, after an all-day team meeting, the team leader wants everyone to go to a bar. [What's important is to] understand that some members might want to stay back and recharge." She suggested balancing group time by offering a low-key event prior to a long session, then an optional, time-limited event after.

Kyzen's Debbie Carboni talked about juggling two teens and a major house move. "Don't try to be perfect," she said. "And be aware that priorities can change. Be willing to dive in, if that's what makes you happy. Find the company and management that supports your goals and approach."

On a more technical level, Brian Toleno, Ph.D., of Microsoft, challenged listeners to think about how changes in technology impact their business and lives. "Consider, what's a possible future?" he recommended. "What are the goals of the future, and what



STI Electronics hired **Caroline Spencer**, Ph.D., as analytical lab manager. She has a bachelor's in forensic chemistry and a doctorate in chemistry, with a focus on forensic applications.



Tempo Automation appointed **Joy Weiss** president and CEO. She most recently was vice president at Analog Devices, responsible for the data center and IoT businesses. She was also CEO of Dust Networks, Inviso, and president and GM of Nortel Networks' Network Management division.

Universal Electronics named **Walter Holle** vice president of operations.



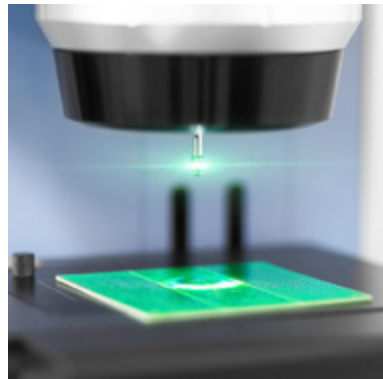
Z-Axis hired **Chuck McFee** as sales manager. He has more than 30 years of experience in technical sales, market development, marketing, and management at Sydor, QED, Zygo, Honeywell/Measurex, and GE Power.

CA Briefs

Apple is reportedly planning to invest \$1 billion to expand its local manufacturing in India.



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are steps along the way? For instance, if you change FR-4 to textile fibers, even if it seems farfetched, what'll take to get there?" He conjured up both big-picture scenarios ("In the event of a war over resources, how do you ensure supply chains if resources become restricted? Especially without warning?") and small-scale ones ("If people wear sensors all the time, what are the ambiguous questions, such as how will that impact you, and what can you do about it?")

On the show floor, an early rush gave way to modest traffic. The absence of IPC likely dampened attendance; the trade group's technical committee meetings, which were co-located with SMTAI the past several years, were moved to the summer this year. Attendance fell from 1,584 in 2018 to around 1,300 this year.

The show floor featured roughly 160 exhibitors, mostly equipment or materials suppliers, with a few contract assemblers and fabricators sprinkled in. Machines were plentiful, but most exhibitors opted for ones that best fit the local market, even if they are not their most feature-laden systems.

PRODUCT DEBUTS. Most "new" product announcements are made at Production or IPC Apex Expo. Still, there were a few debuts.

Nihon Superior, which makes its living in the high-tin-content arena, showed its flux cored solder wire for laser soldering, called Sn97C(032K). Also, the TipSaveN flux cored solder for robotic soldering is said to slow dissolution on the tip, increasing uptime and reducing changeover. Its Sn100CV solder paste now comes in a Type 5 powder.

Europlacer rolled out its Atom 3 high-speed placement machine last spring. The company reports it is now in full production on the machine.

Identco's Brian Connolly explained the ILP-30 label feeder, which is 30% narrower than other competitive feeders. Labels come on antistatic reels.

Insituware, an offshoot of Systems Innovation Engineering (SIE), showed its Vision Mark-1, a materials analysis device. The handheld device reportedly can identify residues on an assembly, predict residue corrosivity, correlate it to SIR, and verify solder paste consistency and fitness for use.

Pace has new tweezers for 0201 sized packages. The company is focusing more on micro-soldering applications. It also noted increased demand for fume extraction at the bench level.

Anda had a modular assembly cell, called the ZPCB-1. The SCARA robot-driven system can perform a variety of tasks, such as die bonding, with stations for printing, placement and UV curing, all in an enclosed environment.

After being shrouded in secrecy at IPC Apex Expo last spring, the Magnalytix OE-200 SIR test system, the brainchild of senior employees of STI and Kyzen, was on full display. The system has undergone certain software and hardware tweaks, and the first units have shipped, the company said. Steve Pollack, formerly of Essemtec, has joined the company to head up its sales effort.

Surprisingly, not much in the way of AGV (automated guided vehicles) was present. Omron had a system that was working in tangent with CTI's loading machines. Juki did not have its AGV onsite but noted its capability of bringing materials to the line by tying them into its component storage systems.

Perhaps the most innovative new product comes from Charlie Moncavage. The cofounder of Ovation Products and Quick-Tool has returned with a new company, Inspire Solutions, and a new take on handling boards at the printer level. His latest invention is Toolmaker, a laser-driven mini CNC system for developing fixtures. A laser scans an assembled PCB and makes a mirror image in a foam "blank." It handles panels up to 300mm x 300mm, and the resulting fixture supports the board, squeegee and provides a precise planar surface for boards and parts. No CAD data are needed; programming is literally as simple as pressing "Go." A fully formed fixture takes about two hours, according to Moncavage. Bjorn Dahle, the former president of KIC Thermal, has joined Moncavage as general manager.

SMTA announced several awards during the show. Chuck Bauer was presented with the Founders Award, Dudi Amir won Member of Technical Distinction, and Greg Kloiber won Excellence in Leadership. Intel won the Corporate+ Partnership Award. — MB

Aqueous Technologies appointed **Restronics** exclusive manufacturer's representative in Northern California.

Astronautics purchased a **Takaya** APT-1600FD-A flying probe tester.

Compal is relocating production of US-bound notebooks to Taiwan from China.

Electrolube held the grand opening of its 8,800 sq. m. manufacturing facility in Zhuji, Zhejiang province, China.

EPFL scientists announced the creation of the world's first robotic hand control — a new type of neuroprosthetic that unifies human control with artificial intelligence automation for greater robot dexterity.

Inventec has invested \$38 million to acquire a new plant in Taoyuan, Taiwan, to expand its local capacity.

Albuquerque approved more than \$35 million in incentives for the expansion of a **Jabil** 3-D printing facility. Jabil will also expand its R&D capabilities in China with a 5G intelligent manufacturing innovation center.

Juki Automation Systems named **Horizon Sales** "Rep of the Year."

Kitron opened an 88,000 sq. ft. EMS plant in Grudziądz, Poland.

Koh Young released its latest case study filmed on location at **Schweitzer Engineering Laboratories (SEL)**.

A new technique by researchers at the **Paul Scherer Institut** in Switzerland and **USC** would allow nondestructively scan chips to ensure they haven't been altered and are manufactured to design specifications without error.

PVA has acquired the software and intellectual property of additive manufacturing startup **Create Orthotics & Prosthetics**.

SVI Public Co.'s largest individual shareholder is making a bid to take the EMS company private.

Vicor is kicking off construction of a \$35.5 million expansion of its Massachusetts manufacturing plant this fall.

VJ Electronix appointed **Torenko and Associates** manufacturers' representative.

WKK will build a new EMS manufacturing plant in Querétaro, Mexico, to take advantage of the trade situation between the US and Mexico.

Würth Electronics will move early next year to a new location in Miamisburg, OH, where the electronics manufacturer plans to more than double its space and staff.

SEE A/V FALL

Trends in the U.S. electronics equipment market (shipments only).

	% CHANGE			
	June	July	Aug.	YTD%
Computers and electronics products	-1.2	-0.3	-0.4	4.4
Computers	-6.7	-1.2	-2.9	-20.8
Storage devices	-4.2	2.7	1.4	20.2
Other peripheral equipment	0.5	-5.5	3.4	5.2
Nondefense communications equipment	1.0	0.6	0.2	11.5
Defense communications equipment	12.1	-14.9	-2.6	2.1
A/V equipment	0.0	0.6	-12.5	35.1
Components ¹	1.6	-1.0	1.0	3.5
Nondefense search & navigation equipment	-1.6	0.4	0.3	3.4
Defense search & navigation equipment	-1.3	1.1	-0.4	2.8
Medical, measurement and control	-3.2	0.5	-1.0	0.9

¹Revised. ²Preliminary. ³Includes semiconductors. Seasonally adjusted. Source: U.S. Department of Commerce Census Bureau, Oct. 3, 2019

IPC Survey: Global Electronics Industry Still Growing – Barely

BANNOCKBURN, IL —The global electronics industry continues to thrive in a positive business environment, according to third quarter results from IPC’s Pulse of the Electronics Industry global data service.

The survey still predicts continued growth over the next year, but results are somewhat less optimistic than in earlier 2019 quarters, and there are some sharp contrasts between regions. The composite score on the current state fell to its lowest level since the Pulse survey began in mid-2017.

The companies’ average outlook for the next six months remains solidly positive on a global level but has weakened since the beginning of 2019. Europe is the only region reporting a net negative composite score on the industry’s six-month outlook. In the six-month outlook for Asia, only exports were rated as a negative driver this quarter, due to the trade war between China and the US.

The 12-month business outlook as of the third quarter remains strong globally, with 87% of responding companies indicating a positive outlook. Only Europe reported a mixed outlook, reflecting the current uncertainty about the impact of Brexit and the region’s slowing economic growth.

Hot Takes

- Global shipments of gaming desktops, notebooks, and monitors reached 10.4 million units in the second quarter, up 16.5% year-over-year. (IDC)
- Smartphone sales worldwide will decline 3.2% in 2019, the worst decline the category has seen. (Gartner)
- The worldwide market for HDI PCBs topped \$10 billion in production value in 2018, with Taiwan accounting for about 40% of the total value. (TPCA)
- India’s production of electronics goods has doubled in the past four years to \$65.5 billion in 2019. (India Ministry of Electronics and Information)
- PC monitor shipments declined 2.2% year-over-year in the



US MANUFACTURING INDICES

	MAY	JUNE	JULY	AUG.	SEPT.
PMI	52.1	51.7	51.2	49.1	47.8
New orders	52.7	50.0	50.8	47.2	47.3
Production	51.3	54.1	50.8	49.5	47.3
Inventories	50.9	49.1	49.5	49.9	46.9
Customer inventories	43.7	44.6	45.7	44.9	45.5
Backlogs	47.2	47.2	43.1	46.3	45.1

Sources: Institute for Supply Management, Oct. 1, 2019

KEY COMPONENTS

	APR.	MAY	JUNE	JULY	AUG.
Semiconductor equipment billings ¹	-28.5%	-23.6%	-18.4%	-14.6% ^r	-10.5% ^p
Semiconductors ²	-13.7%	-14.8%	-16.5%	-15.5% ^r	-15.9% ^p
PCBs ³ (North America)	1.02	0.99	1.00	1.00	1.02
Computers/electronic products ⁴	5.35	5.39	5.46	5.46 ^r	5.48 ^p

Sources: ¹SEMI, ²SIA (3-month moving average growth), ³IPC, ⁴Census Bureau, ^rpreliminary, ^prevised

- second quarter to just over 30 million units. (IDC)
- German electronics companies reported July sales rose 1.8% over the previous year to 16 billion euros. (ZVEI)
- Taiwan’s electronic components exports reached \$10.48 billion in August, up 10.3% sequentially and 7.5% from last year, with ICs making up 89% of the segment’s value. (TPCA)
- The server industry is having a weak 2019 due to high inventory levels, but global shipments are expected to grow around 5% in 2020. (DigiTimes Research)

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A Wave at the Future

From additive manufacturing to autonomous vehicles, figuring out the next big thing is no small chore.

WITH THE LAST quarter underway and all eyes beginning to contemplate what and how to do better in the year to come, one of my focuses is trying to identify which technology will be the next big thing – one that will either transform or disrupt doing business as I know it.

Over the past couple years politics seems to have been the biggest disrupter for all types of businesses. As challenging as it may be to identify the next tariff or tweet that may or may not send markets – and customers appetite to buy products – into a tailspin, the real challenge is trying to identify the next technological breakthrough that will either propel my business and the greater electronics industry forward or retard them into oblivion. Over the past dozen years many technological initiatives have been touted as game-changers; however, to date none has truly had the big bang effect on our industry.

Printed electronics, after decades of hype, has a place in the technology roadmap but not as originally anticipated. Early prognosticators believed printed electronics would displace printed circuit boards. Thinner, more exotic substrates appeared to offer promise of finer lines and features “printed” on them than could be fabricated on traditional substrates used in traditional PCB processes. In many ways printed electronics continues to show promise, but it will not cost-effectively displace inner or outerlayers as the predominate form of circuit board construction anytime soon.

Nano materials also have been hyped for some time as a game-changer, yet also had difficulty finding traction as a replacement for traditional chemistries and additive surface finishes. Some of these materials show much potential as viable options to some chemistries for some applications. They are not ready for prime time, however, and as a group still appear as illusive to board fabricators as a lake in the desert is to a thirsty traveler. Traditional chemistries still offer the most cost-effective and reliable option in our industry.

3-D printing, on the other hand, has been a game-changer, and not just for our industry. In the mechanical world 3-D printing has changed the way products are developed, from prototype to production, from simple to complex. While offering an interesting and potentially viable platform on which an electronics circuit could be applied, how 3-D printing might impact board fabrication and assembly is far from clear. 3-D printing offers intriguing geometries and angles that need to be monitored, as they may result in some breakthroughs in how circuits are applied and components are mounted, but to date has not been as disruptive in electronics as it has in the mechanical world.

Autonomous automobiles, and pursuit of same, are being hyped as the technological wave of the future. While the market may or may never come to fruition, the investment into technology to attain the goal is significant. The beneficiary industries for this technology appear to be in the world of sensors and software, which require PCBs. While the technologies being developed may not have any impact on the technologies that go into fabricating or assembling boards, there potentially will be a beneficial bump in product volume, even if built by traditional methods using existing materials.

All the above technological innovations, as well as dozens of others developed over the span of my career, have impacted our industry. But none has revolutionized or forever changed it.

The last technological development that truly transformed our industry was the development of the IC. It displaced wire harnesses as they had existed, forcing that industry to forever change, and created what is now the PCB industry – encompassing fab and assembly.

When the IC, or microchip, was developed, it was underestimated. Yes, it offered a breakthrough in the number of circuits that fit into a small area of real estate. But no one imagined the impact so many circuits in such a small space would have on such a wide spectrum of products. No one could imagine that, as incredible as the first generation of microchips were, they would provide a platform that would continue to enable greater processing capacity in ever smaller spaces, what we now call Moore’s law. Most important, no one imagined the impact on manufacturing, and certainly no one could fathom the impact on society.

When looking into the future, too often we overestimate the impact, disruptive or not, of some development hyped by the pundits, while underestimating or even ignoring a less visible but more impactful innovation. It is those quiet innovations I seek, and fear most!

Nevertheless, finding what is important and impactful is not easy. Amid the hype, promise and pronouncements, it can be close to impossible. Yet somewhere out there lies an idea or process or product that could be a real game-changer for us all and lead to a “big bang” that will transform industries and everyone in them. That’s why we need to keep looking, train our eyes and ears on what is new, and what is being quietly worked on, as well as what is being hyped. Take the hype with the proverbial grain of salt. Focus on understanding the little things that could come to fruition and become big.

I doubt that anything in 2020 will displace the PCB, but I also hope nothing will be developed that eventually displaces us all. □

PETER BIGELOW

is president and CEO of IMI Inc. (imipcb.com); pbigelow@imipcb.com. His column appears monthly.



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A Good PCB Vendor Should Ask Questions

Talk isn't cheap, but the absence of it could cost you even more.

THROUGHOUT MY PCB career as a go-between for board buyers and manufacturers, I've often heard complaints from buyers that fabricators – domestic and offshore – ask too many engineering questions (EQs) after receiving an order. “Why can't they just build the board?” buyers say.

This mystifies me. In my view, PCB vendor questions provide valuable feedback. They may indicate the vendor lacks all the required information to build the order. They also tell me the manufacturer is intent on gathering all the data necessary to do the job right.

I'd be more concerned if no EQs came from a vendor. A PCB has over 100 separate required manufacturing processes, almost all of which are unique to each customer. It would be surprising, even alarming, if everything in an order was absolutely clear, with no back-and-forth necessary.

Rather than argue with customers, if a buyer complains about too many EQs, I simply respond there is a direct correlation between the number of EQs and quality of the PCBs received. Then I add, “Let me see what I can do to limit the number of questions.”

I understand the delivery clock is ticking, and the customer wants the order as soon as possible. But who wants to populate boards with expensive components, only to have them fail at the end of the assembly line? PCB vendors want to build orders correctly. Their questions help protect their interests and those of their customers. It's worth it to take the time to answer all questions completely.

Over the years, I've worked for a number of different companies, all of which had a variety of customers building an even wider selection of PCBs. Yet, the complaint about too many EQs came up more than anything else. It still does. After a while, I began to wonder whether the problem was not so much with the fabricators as with the buyers. Maybe purchasing and engineering personnel lack the training needed to properly relay all the information required to build a PCB.

Prior to sending to fabricators, files need to be checked, not only to ensure they have all required information on orders, but also that they fall within industry (and possibly company) manufacturing standards. Not all buyers have the expertise to do that. In addition, many companies lack a documented PCB fabrication specification that manufacturers can reference when they receive information that is incomplete or needs clarifying.

Does your board get the least attention of all the items on a bill of materials (BoM)? The PCB makes up 8 to 12% of the BoM cost, and it is the founda-

tion of the manufactured product. When vendors ask engineering questions, they are acting in the buyer's best interest.

Here are questions and comments I often see from PCB vendors. By answering them ahead of time, you'll help speed your order through the manufacturing process:

- “Confirm PCB solder mask to be green in color.” Many older fab prints still in circulation do not specify solder mask color. That's because PCBs were traditionally green. Today, boards come in a variety of colors, so fab drawings need to clearly state the color to be used.
- “Print states: Build to IPC Class 2. Is that IPC-A-600 or IPC-6012?” This simple question means a world of difference when it comes to the amount of testing and paperwork required. The customer might require all that additional paperwork to confirm the assembly meets its needs. If the proper paperwork isn't with the boards at delivery, the assembled product might be useless. Be sure you answer this question. By the way, “Just build commercial” is not an acceptable answer, as both IPC-600 and IPC-6012 are commercial specifications.
- “Are X-outs allowed?” To save on PCB costs, some assembly operations can accommodate PCBs that are provided in array or panel format with X-outs – nonfunctional boards – while other assemblers cannot or will not accept X-outs. A corporate PCB fabrication specification spelling out customer preferences addresses this issue and saves time.

Surprisingly, many companies, including some well-known OEMs and plenty of EMS firms, do not have a corporate PCB fabrication specification that is unique to their operation or assembly needs. This document can be as concise as a few pages. It should outline everything from acceptable material types to desired metal finishes to final packaging and storage requirements. It should also include panelization instructions.

Corporate fabrication specs should answer most EQs. You might get specific queries about dealing with artwork tolerances, for example, or the need for a stack-up variance to permit controlled impedance. Those questions would have to be answered individually. Companies can save a great deal of time by creating fab specs and then ensuring they are fully understood within the firm and among the vendor's personnel.

continued on pg. 64

GREG

PAPANDREW

has more than 25 years' experience selling PCBs directly for various fabricators and as founder of a leading distributor. He is cofounder of Better Board Buying; greg@boardbuying.com.

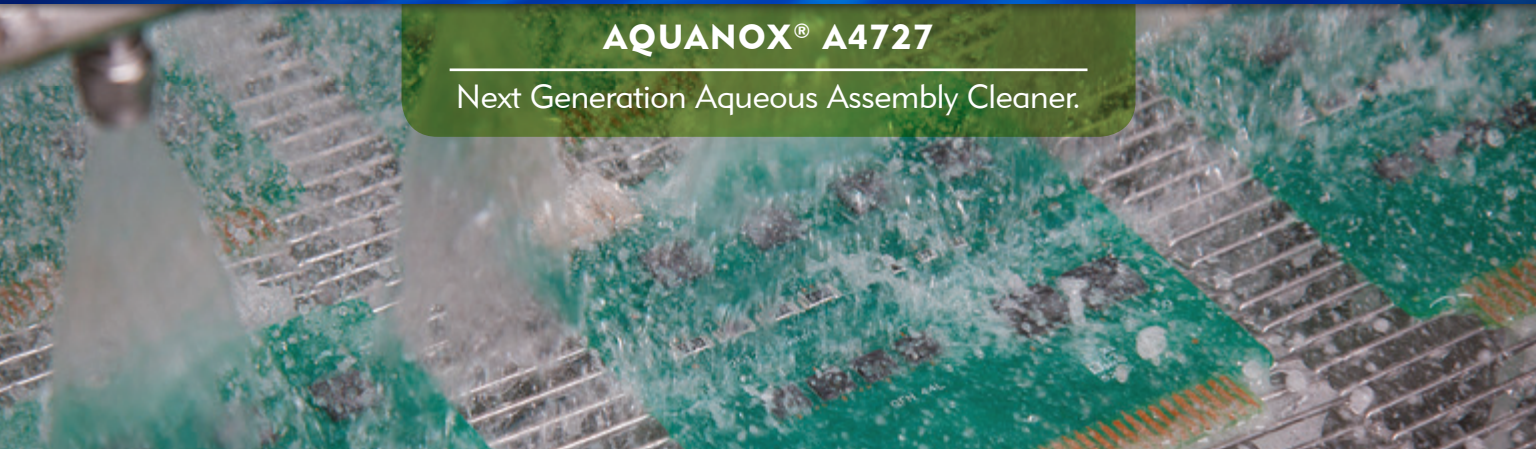




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IT IS TRUE that even today, so many years after 3-D printing started to garner attention and acclaim, rapid prototyping remains the single most common use for 3-D printers. 3-D printers offer advantages in the form of shorter turnaround times, improved development secrecy and greater design freedoms. But it is also true 3-D printing isn't going to remain primarily a tool for rapid prototyping much longer.

Those keeping abreast of events in the worlds of design, construction, manufacturing or medicine will be keenly aware of the impact of additive manufacturing in these fields. Certain products have been rapidly affected by the arrival of additive manufacturing. Prime examples are hearing aids and dental aligners. Both markets have been transformed by the adoption of 3-D printing technologies. Additive is now the default manufacturing technology for such products.

Now, the emergence of additive manufacturing to make final parts correlates well with products that require:

- Customization (where individualization is a priority, such as dental aligners and hearing aids)
- Small volumes (where scaling to mass production is not a priority)
- Difficult logistics (distributed in-situ manufacturing such as in space or other remote locations)
- Highly complex parts that cannot be made using traditional methods (such as GE's advanced jet nozzles).

The arrival and evolution of additive manufacturing in the mechanical world is something people are now familiar with. That it is beginning to have a similar impact in other domains such as medical and electrical functionality is becoming more obvious. The underlying advantages remain the same, but the systems and materials required to deliver the results are very different.

What makes additive manufacturing of electronics different? For additive manufacturing to make inroads into the world of electronics requires several ingredients the traditional additive manufacturing toolset doesn't include. Resolutions need to be better; multiple materials need to be printed simultaneously in the same machine, and materials must support high temperatures and have specific dielectric properties.

For additive manufacturing to provide a compelling offering to the electrical engineer, the approach must deliver ways to speed prototyping, bring it in-house and open doors to entirely new ways of designing and manufacturing electronics. The same recipe that has brought much success to 3-D printing is now in place to do the same to this new electrical domain.

Deposition of materials is key. An additive manufacturing approach is clearly based on precise deposition of materials. This is a layer-by-layer additive process, whereby specific materials are placed in specific locations to build up an integrated functional part in a one-system print process.

For an engineer looking to speed current R&D cycles, this means bypassing much of the waiting involved in traditional outsourced prototyping. Going from design to functional part in a matter of hours can change how innovators and R&D groups practice their craft. This can get a validated circuit board from PCB design much more quickly. Given the flexibility of additive manufacturing, the engineer can also consider electrical applications beyond traditional PCBs, including designs for antennas, printed capacitance, electromagnets and molded interconnect devices (MIDs).

Rapid progress from design to part. To be clear, additive manufacturing of electronics is not limited to PCBs. It is also used for other types of application development, including devices with new requirements and increasingly complex formats. It's an ideal fit when faced with geometrical complexity, portability and very small dimensions, such as those for semiconductor applications, medical devices, Industry 4.0, the Internet of Things, etc.

When designing a standard planar PCB, operating a 3-D printer doesn't require anything other than the traditional Gerber and Excellon output files. Traditional EDA PCB design packages are focused on meeting the needs of today's electrical engineers. This means the ability to design circuits and systems of circuits that are rigid or flexible, planar, multilayered, high-speed-compatible and so on. All these can then readily output files that can then be used by the 3-D printer.

A new way of thinking. Additive manufacturing is now leading to new ways of thinking about old challenges. Some of these require design tools that can design in the third dimension and design new capabilities.

- **Capacitors.** Additively manufacturing capacitors within the layers of a circuit can create space to meet miniaturization requirements. With extra space, designers may pack more functionality on the board and shrink component size – all without compromising reliability.
- **RF circuits.** Harris Corp. has additively manufactured 6GHz RF amplifier circuits, and found they worked as well as those created with traditional methods.
- **Side-mounting technology.** Recently, Nano

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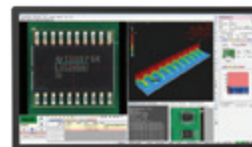
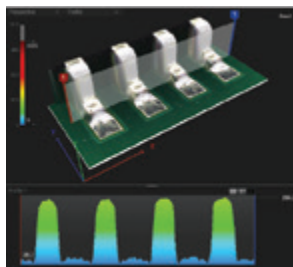
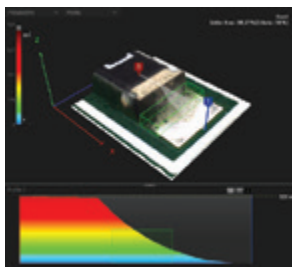
cofounded Nano Dimension and has worked as a consultant on projects covering sales, marketing and strategy across the automotive, financial, retail and telecom industries.





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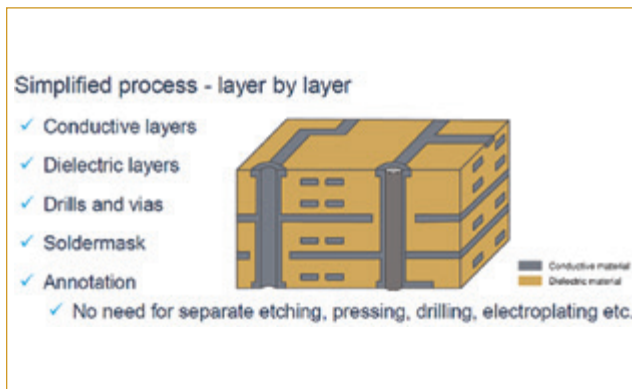


FIGURE 1. A cutaway rendering of a 3-D printed board.

Dimension announced a world's first side-mounting technology for additively manufactured PCBs. Using a 3-D printer to create a circuit board, components were placed on the top and bottom of the PCB, as is traditionally done. Components were also added to the sides, resulting in as much as a 50% increase in board space compared with traditionally manufactured PCBs. 3-D printing mounting allowed design engineers to pack more functionality on the board.

- **Ball grid arrays.** Modern printing technology can shorten and simplify the assembly process for BGAs and other SMT

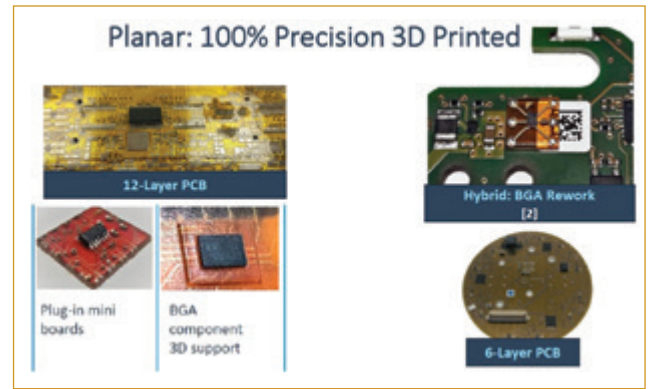


FIGURE 2. Samples of 100% precision 3-D printed products.

components. In a proof-of-concept testing, the time needed to create and populate PCBs with BGAs went from days or weeks to just one hour. Typically, the process from initial design through printing, soldering, manufacturing, assembly and reflow takes weeks to complete. With a special layout structure that can be achieved only through additively manufactured PCBs, there is no need for special tooling for assembly. This enables in-house manual assembly of BGAs and SMT components during the design and application development phase.



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"Going from design to functional part in a matter of hours can change how innovators and R&D groups practice their craft."

Where are we heading? Additive manufacturing of electronics, whether circuits, antennas or components, is very much a reality. No doubt we are in the early days of the revolution, but 3-D printing electronics is here. Developing and deploying increasingly rapid, reliable and material-agnostic printers will only further use of this technology. The addition of a broad range of advanced, 3-D printable materials and sophisticated electrical design packages capable of truly non-planar electrical design and simulation will see this grow to an everyday part of the electrical engineer's toolkit. □

The logo for PCB WEST 2020 Conference & Exhibition. It features the letters 'PCB' in white on a teal square background with three white dots below it. To the right, 'WEST 2020' is written in a large, dark, sans-serif font, with 'Conference & Exhibition' in a smaller font below it. The background of the entire page is a stylized circuit board with glowing lines and a teal-to-yellow gradient.

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Smart Manufacturing Technology Calls for Smart Investment

If Southeast Asia has the lowest labor rates, why do they also have the best automation?

COMPARED TO HIGHLY visible “mass” markets such as automotive electronics and smartphones, it’s easy to think of the market for industrial electronics as “niche.” However, in total, about 23% of PCBs produced worldwide are used in electronics equipment for manufacturing applications. If we include categories that are obviously non-consumer, such as telecom equipment, data-center computing, and solar/wind-power conversion, storage, and smart-grid control within our concept of industrial electronics, it’s clear this sector is extremely important to the world’s electronics producers.

As far as technology for manufacturing is concerned, we see organizations introducing digital transformation are profoundly changing the way they go about making, marketing, and supporting their products. Within this, smart manufacturing (aka Industry 4.0) leveraging cyber-physical systems, connected through the Industrial Internet of Things (IIoT), seamless linking of operational technology (OT) and IT infrastructures, intensive robotic process automation, and infusion of AI into edge devices and cloud services, is enabling companies to increase efficiency and agility, and improve standards of service delivery to customers.

But moves toward pervasive automation are no longer purely about the drive to compete. For many years now we have accepted the view that Western high-tech manufacturers have driven high levels of automation to combat the labor-cost advantages enjoyed by offshore producers. It’s a notion that has become entrenched. In today’s world, however, the situation is rather different. Right now, the largest and most highly automated factories are found in China. It’s a simple fact automation is critical to be able to build advanced products meeting the expected levels of quality and reliability. End-user markets everywhere, from telecom and data centers to consumer smartphones, are expecting faster speeds, greater capacity, and more functionality. Automating key manufacturing processes – including the fabrication of advanced PCBs designed with progressively smaller and smaller feature sizes and hence finer and finer tolerances – is the only viable approach if manufacturers are to satisfy these demands.

The race is on globally. I recently visited some state-of-the-art PCB factories in Europe that are predominantly founded on automated processes fed by robotic handlers that are themselves supplied using automated guided vehicles (AGVs), and include fully automated 100% inline inspection and verification.

Establishing and maintaining such fully automated factories is not cheap, but there is really no alternative. Automation cannot move forward without investment. Without automation, needed products cannot be built to the expected quality and reliability standards. And falling short on quality and reliability will lose the market.

This is understood everywhere: All manufacturers have the desire to compete and understand what it takes to do so. But it is clear the necessary capital structures are strongest and best adapted in Asia, where it is normal for organizations to work toward payback over, say, five, 10 or even 15 years. The financial structure to support heavy investment in advanced technologies is the one key ingredient I’ve heard Asian visitors in Europe remark is lacking in the West.

"We have accepted the view that Western manufacturers combat labor-cost disadvantages with high levels of automation. But right now, the largest and most highly automated factories are in China."

Perhaps this is why, despite the fact that major markets for high-tech products (all products, not only consumer electronics but also telecom infrastructure equipment, automotive electronics, and others) remain in the West, PCB production including production of advanced substrate materials and chemicals, as well as final board fabrication, is predominantly in Asia. And by some margin. Some 54% of today’s PCB fabrication takes place in China, with Taiwan and South Korea accounting for another 10% each. While production in Japan represents about 7% of the world’s output, that’s about the same as North America and Europe combined.

Things are different when it comes to final assembly of high-tech products. A significant proportion of surface-mount assembly of industrial electronics equipment destined for consumption in Europe now happens in countries on the edge of the Bloc. Former

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Eastern European countries such as Hungary, Poland, Romania, Slovakia, Czech Republic and others have become important electronics manufacturing destinations.

In addition to producing equipment for use in smart factories, manufacturers in these locations are supporting Europe's strong presence in the renewable energy sector, including high-efficiency power filters, inverters, storage-battery systems, and grid-tie electronics.

This is heavily dependent on power electronics for conversion and control, maintaining acceptable power quality, as well as advanced smart grid equipment to manage feed-in and balance energy flows using techniques such as demand-side management.

From a supplier's perspective, the globally dispersed nature of high-tech manufacturing and long-term economic shifts, as well as short-term effects such as political uncertainties, challenge us to get products in the right place at the right time and provide the support that customers need. At Ventec, for instance, although our major manufacturing centers are in Taiwan and Suzhou,

close to where the majority of the world's PCB manufacturing is focused, our distribution network is global and entirely self-owned, giving us control over quality of service delivery and the way we respond to changing situations.

In the longer term, although consumption in Asia is currently low compared to output destined for Western markets, the picture is likely to change due to rising domestic demand, as the growing Asian middle classes acquire more disposable income to spend. This will be manifested not only in increasing sales of high-end consumer products but also growing demand for high-performance telecom and data infrastructures and technology for smart transportation, smart energy and micro-generation, driving further large-scale shifting in global manufacturing capabilities. □

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Chapter Meetings Put a Fine Coating on Education

Reports from San Diego, RTP and AltiumLive.

AS THE SECOND half of the year is quickly passing by, we have seen many continued activities in our industry regarding PCB design. From the PCB West conference held in mid-September in Santa Clara, CA, which was another huge success and always exceeds expectations, to AltiumLive 2019 held in early November in San Diego; both events were hugely successful and had great turnouts. We also have had some activity within our local IPC Designers Council (DC) chapters, such as the San Diego Chapter, which held its final chapter meeting for the year in late September. Here is a brief breakdown of these recent fall activities.

San Diego Chapter

Chapter leader: Luke Hausherr, CID+

The San Diego Chapter held another successful meeting on Sept. 24 at San Diego PCB with 25 attendees. OrCAD EMA sponsored the event to help offset the cost of lunch. The highlight of the meeting was a presentation by Jeff Jenkins that covered conformal coatings. The content of the presentation was thorough and received positive feedback from all who attended. Jeff is a PCB chief technologist for L3Harris and has been involved in the workings of the PCB design, fabrication and assembly industries for over 23 years.

His presentation covered:

- The purpose of conformal coatings
- Types of conformal coatings and pros and cons of each
- Methods of application and pros and cons of each
- Items not coated
- Engineering drawings and notes.

The San Diego Chapter will reconvene in January to plan for 2020.

Silicon Valley Chapter

Chapter leader: Bob McCreight

The Silicon Valley Chapter held a chapter meeting on Oct. 24 and will report its continued success in next month's column.

Research Triangle Park (RTP) Chapter

Chapter leader: Tony Cosentino

Next month the RTP Chapter will report on PCB Carolina, which will take place Nov. 13 in Raleigh.

AltiumLive 2019

This annual event, which takes place in the US, as mentioned earlier, and in Frankfurt, Germany, creates a lot of industry buzz and has gained tons of traction over the past few years. This year's keynote speakers

included Eric Bogatin, Robert Feranec, Joe Grand, and Bob Martin, in addition to industry technical sessions led by Rick Hartley, Gary Ferrari, Mike Creeden, Susy Webb, Tara Dunn, Pete Wilson, Linda Mazzitelli, Max Seeley, Carl Schattke, Ari Mahpour, Shashank Samala, and many others. The Altium technical team also covered the University Day Courses. Feedback from this year's attendees has been overwhelmingly positive, as reported by my dear friend and colleague, Judy Warner, director of community engagement at Altium. As always, it's great to see and hear about continued activities, from professional development to knowledge sharing and networking taking place at various industry events.

IPC CID/CID+ Certification Success

We also continue to have successful IPC CID and CID+ certification classes. The feedback from attendees of these classes is extremely positive. They are an excellent source of professional development. If you are not yet CID/CID+ certified, I highly recommend these certification courses as a path for continued education in PCB design.

The remaining IPC Advanced Certified Interconnect Designer CID+ training session for 2019 is scheduled for Dec. 3 - 6 in Manchester, NH. Note: Dates and locations are subject to change, and a minimum enrollment of seven students is required for a class to be held. Contact EPTAC Corp. to check current dates and availability. □

STEPHEN CHAVEZ is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee. To read past columns or contact Chavez, click here.



FIGURE 1. Luke Hausherr (right) presents a certificate of appreciation to Jeff Jenkins.

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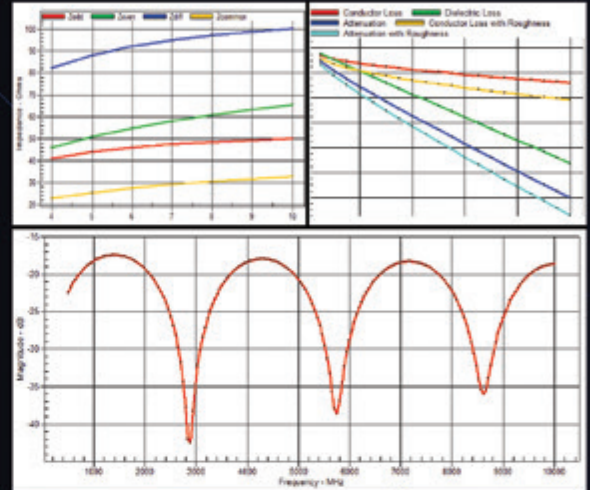
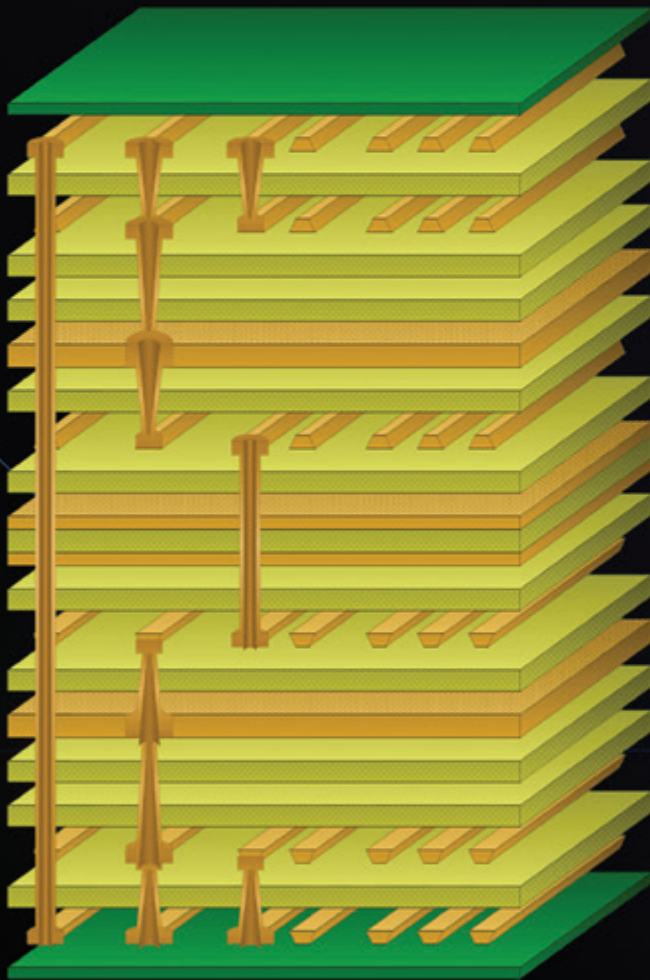
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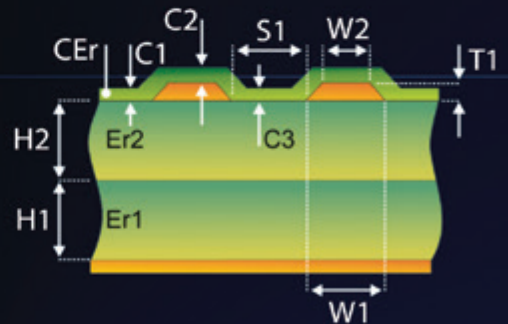
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Why You Should Quit Using 1080 Glass

The high percentage of resin coverage can cause skew issues at higher speeds.

SINCE JUNE, I'VE been writing about glass-weave skew (GWS). If you haven't read those articles, you may want to go back and bone up on the subject. We'll review a few points here.

A serial link's differential-skew budget shrinks as bit rates increase. For example, a 1Gbps (500MHz) signal would have roughly 250ps of skew tolerance. That's a wide window, and why most engineers didn't need to worry about GWS 20+ years ago. Fast forward to 10Gbps (5GHz), and the skew tolerance will decrease proportionally to around 25ps.

When working at frequencies below 1GHz, or when using whatever materials the fabricator has in stock due to schedule constraints, don't worry about glass style. If signaling at higher speeds and there is time to plan, read on.

As a mechanism for mitigating GWS, glass and laminate manufacturers adapted the mechanically spread glass already in use for improved laser drilling. IPC has not agreed on a definition for mechanically spreading glass. Like many aspects of the copper-clad laminate (CCL) world, a laminate's "degree of spread" is left to the glass manufacturers, which are currently bent on keeping everything as proprietary as possible, and little has been done to quantify the degree to which glass styles differ from one another relative to the spreading of the fabric. Nevertheless, there are things we can learn from available data.

Background on 1080 glass. The history of 1080 glass is extensive. Every PCB fabricator on the planet uses it. Your fabricator, as well as the vendors selling laminate to them, have warehouse shelves stacked with sheets or panels of 1080 glass. Tied to the high-production volumes, it's a reasonably priced alternative for the constructions it supports. Typical single-ply core thicknesses range from 2.4 to 3.5 mils. Dual-ply 1080 core constructions range from 4.0 to 7.0 mils.

Issues with 1080 glass. What is it about 1080 glass that's problematic for glass-weave skew? The primary concern is the fabric's "resin windows" (my term for it) are larger than the other alternatives. **FIGURE 1** shows how optical-measurement images are used to determine glass-coverage percentage (green) versus resin coverage (yellow). Ideally, for mitigating glass-weave skew, the glass coverage percentage (green) should be as high as possible. Higher glass coverage means there's a higher probability two halves of a differential pair will "see" the same or similar Dk environment along the signal paths, all other things being equal.

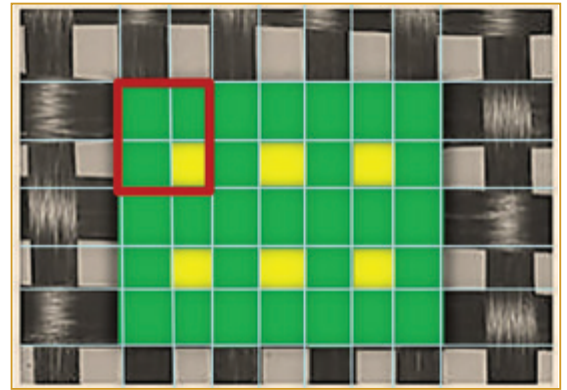


FIGURE 1. Optical measurement images are used to determine glass coverage percentage (green) vs. resin coverage (yellow).

If we consider the red rectangle in Figure 1, and we know the glass pitch (**TABLE 1**) and the warp and fill yarn widths, it would be possible to reverse engineer the relative size of the yellow resin window we are seeking to minimize, and use this as a metric for comparing glass styles, including 1080 glass and its alternatives. Unfortunately, yarn-width data for woven fabric are not widely available.

TABLE 1. IPC-4412 Parameters and Relative Availability for 1080 and 1078

STYLE	THICKNESS (MILS) (REFERENCE ONLY)	FABRIC COUNT WARP X FILL (PER IN.)	WEAVE PITCH (MILS)	FILL PITCH (MILS)	NOMINAL WEIGHT (OSY*)	AVAILABILITY
1080	2.1	60 x 47	16.7	21.3	1.38	1
1078	1.7	54 x 54	18.5	18.5	1.41	1
1086	1.97	60 x 58	16.7	17.2	1.53	2**

1 = more available. Data for 1086 glass from Nanya CCL. OSY = oz. per sq. yd. (Metric: GSM or grams per sq. m).

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has more than 20 years' experience in PCB design software and materials. He is director of everything at Z-zero (z-zero.com); billh@z-zero.com.





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One alternative to 1080 glass is 1078, which is close to a drop-in replacement, with typical single-ply core thicknesses ranging from 2.3 to 3.5 mils. Dual-ply 1078 core constructions range from 4.0 to 7.0 mils. Another alternative, 1086 glass, is thicker, with typical single-ply core thicknesses ranging from 3.0 to 3.5 mils. Dual-ply 1086 core constructions range from 5.0 to 7.0 mils.

Except for 1086 glass, IPC-4412B frames the differences between these glass styles as summarized in Table 1. Using that data, along with available widths for warp and fill yarn, we can calculate the approximate size of the yellow “resin window” in

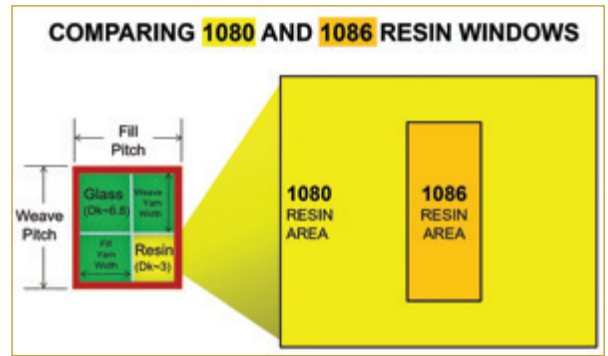


FIGURE 2. The yellow resin window we’re seeking to minimize for 1080 glass makes up 24% of the board area (76% glass), far less than alternatives.

Figure 1. Using available pitch and yarn-width data for normal, non-spread glass, **FIGURE 2** shows the resin window that we’re seeking to minimize for 1080 glass makes up 24% of the board area (76% glass), while resin windows for 1086 glass are just 5% (95% glass), using data for non-spread glass. That’s a dramatic difference! The difference between 1078 and 1080 glass is significant as well, but not quite as dramatic. (At this writing, I only have yarn widths for Nanya glass, which is spread.) Either of these offer an advantage over 1080 glass.

Glass symmetry. Another concern with 1080 glass is its asymmetrical in the warp versus fill directions. That is, it’s “asymmetrical” in the sense that yarn count in the weave and fill directions are unequal. Of the three glass styles discussed herein, 1078 is “squarest” of the three. Working from the yarn counts in Table 1, 1080 is the most asymmetrical construction, and 1086 is just a bit off. Dk and impedance are like the game of horseshoes, where getting close still helps.

The advantage here is you can align your differential signal pitch to the glass pitch, and it doesn’t matter how the board is oriented on a panel. In a later article or column, I’ll elaborate on the benefits of square weaves. □



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SOFTWARE SUCCESS Was a Leap of Faith

After three decades in ECAD sales, some things haven't changed at North America's largest VAR. BY MIKE BUETOW

Before Manny Marcano came to ECAD software sales, he jumped out of airplanes as a paratrooper in the US Air Force. Taking risks, it seems, is in his blood.

So, after selling tools for others in upstate New York in the mid-1980s – by his own account, he was a “lousy subordinate” – Marcano took the plunge. He cut a deal in 1989 to concentrate solely as a reseller of P-CAD and started EM Associates in his basement. As he recalls, “I pretty much was a one-man band. I got my family to stuff envelopes on the dining room table, and we did marketing things, but it was just old school, bootstrapping a business the hard way. There was no funding. I took a second mortgage on the house to fund the business. It's a calculated risk that worked out.”

Thirty years later, EMA Design Automation is the largest value-added reseller of ECAD tools in North America, possibly the world. Its product breadth goes well beyond selling place-and-route tools. And its founder has laid the path for continued success for decades more.

ECAD in the 1980s and early 1990s was chaos. The market was growing fast and was full of vendors and resellers. OrCAD, FutureNet, P-CAD, Scicards, Pads, Calay and many other names, most of which have been relegated to the tech dustbin, were among software startups at the time. There were 10 to 15 VARs or distributors of various sizes, with Trilogic perhaps the largest. Industry was transitioning from dedicated hardware to PCs. CAD libraries were nonexistent, Marcano recalls.

Over its first decade, EMA extended its reach from P-CAD to ViewLogic and Pads. EMA added the Cadence line in 1998. After Cadence acquired OrCAD in 1999, EMA went all in, ending its relationships with its other vendors. It was, the ex-paratrooper says, a huge risk. Then a four-person company with sales between \$1 million and \$2 million, they decided to bet its future on a single line, a highly unusual move.

Marcano remembers the time with mixed feelings. “That couple of years was probably some of the toughest I've experienced in my life. The OrCAD inside sales team was trying to find their place after joining Cadence. Because we had a rolling contract with Cadence, we were the only VAR left standing after the OrCAD acquisition. There was lots of uncertainty as Cadence absorbed OrCAD and had to figure out the product and sales direction for the business going forward. Thanks to our standing in the industry and our relationships inside Cadence, we were able to persevere.”

As EMA's product lines evolved, so did its geographical reach. In 1995, EMA extended its territory to the Mid-Atlantic US. By 2003 its sales staff was covering all of North America.

It didn't stand still from a product perspective either. What makes EMA different from its competitors, then and now, is its willingness to invest in its own IP. “We saw problems customers were having that were not being addressed by the mainstream



FIGURE 1. 1989 letter establishing EMA as a P-CAD reseller.

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Linear Technologies, Inc.	EMShop Wire Harness Design Software
Proter Solutions	CAMCAD CAM File Viewer, Editor & Database Translator
Tantrum Research, Inc.	Custom IC Design IC MEM & MCM Design Tools
Viewlogic Systems, Inc.	Workview Office A Series of Capture, Signal & Analog simulation QUAD Design Signal Integrity Software Nonlinear FPGA Express Analysis Software
Visual Software Solutions	StackCAD Tools for High-Speed Design with VHDL, Verilog & C++ code output

FIGURE 2. EMA line list, circa 1998.

PCB vendors. We decided to address these market needs ourselves. This really was a turning point in the evolution of the company,” Marcano said. As such, EMA has acquired several companies and technologies that enhance its position as an EDA player, including TimingDesigner (2007), DesignAdvance (2009) and Accelerated Designs (2016). The latter deal came after EMA lost a new customer to a competitor that had a library offering. EMA has also developed library and design data management solutions, and connected component parametric data directly to the CAD environment.

With its history of M&A and new tool development, has EMA become a full-fledged EDA company? “We are absolutely a VAR, just not in the traditional sense. We are the epitome of ‘value add,’ ” Marcano says, “We just happen to focus on building long-lasting value-added relationships with our customers.”

Yet, true to form, Marcano speaks of “global aspirations.”

“We have products that we either developed or have acquired that are seeing strong growth in North America. We are looking at ways to take this technology worldwide. The challenges for these engineering teams are the same no matter where they are.”

Demographic Shift

Still, the changing demographics of buyers and users represents the biggest shift EMA has seen in its 30 years. Designers of today are much more demanding, he says. “The 25-year-old engineers have a different set of expectations. They want things at their fingertips. They want content. They know the library should exist, and they don’t think they need to reinvent the wheel every time. And I agree with that.”

Indeed, features are in some ways taking a backseat to speed. Marcano doesn’t say it, but when you are jumping from planes, bells and whistles won’t save you. You need to know the parachute works when you need it. That experience likely colors his thinking today.

“Everything revolves around time to market,” Marcano asserts. “If the marketing department says, ‘We have to launch a product or get to a trade show’ or whatever it is, what’s the path of least resistance? We try to give the engineer the tools they need to get things done quickly, accurately and on time. Engineers are working nights and evenings to meet some deadline, and if they have to redo a BoM or research a new part because the first part they specified doesn’t meet obsolescence requirements, they are wasting time on things we can automate.”

In this last respect, he empathizes with users. “Every tool on the market right now will have its adoption challenges. Engineers get that. What they need is a vendor to help them get their job done effectively without causing delays. We do that through support as well as the IP we provide to automate as many tasks as possible with software. Engineering managers get that as well. They see when they’re buying engineering manhours back, and now they can get their engineers doing engineering work and not admin work. That’s a big part of our value proposition.

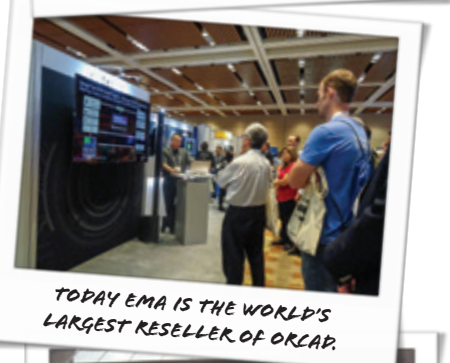
“The tools are all very capable,” he goes on. “We have found it’s the way the tools are deployed that can really differentiate and help our customers ensure success. That, and who you can get to support you. Process, methodology, and support, have been more important to our success than any of the specific tool features.”

In the past year, EMA published a tome called the *The Hitchhiker’s Guide to PCB Design*. In it, Marcano wrote the time is now for the convergence of ECAD and MCAD, a process known as mechatronics. Again, he says, it’s all about time to market. “There’s no longer time to build a printed circuit board and build an enclosure in parallel in different departments, only to find the board doesn’t fit in the box or goes up in smoke because some device is touching the chassis. This problem has to be solved way upstream and collaboratively between the two departments.”

To that end, he is bullish on the future of 3-D printing. But he doesn’t think a change in the way PCBs are prototyped will portend an entirely new wave of software. “I’m sure the current set of software will work because it’s good stuff. But the fact remains it’s still about time to market. Imagine designing something for a car like an injection molding device with traces and passives on it, and you can knock that out in a lab. People are doing this stuff now in their skunkworks or their IP group. There’s always the problem of inserting parts, but all those problems will be solved [over time]. This is absolutely where we’re going.”



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Meanwhile, he won't be losing any sleep over the future of the printed circuit board. "The PCB is the only way to get something from concept to reality. It will soldier on. There will always be a printed circuit, no matter what the technology is."

Remembering the Past

Now that Marcano is getting closer to retirement age, a succession plan is in place. "It is my firm belief that an organization cannot revolve around one person. There has to be a leader, but there has to be a succession plan." True to his vision, Marcano has put three EMA staff through full MBA programs, one of whom is his son, Manny Marcano III, known informally as M3. That triumvirate will someday take over the firm.

From a company of two, EMA is now over 100 employees. It has survived market and demographic shifts and multiple industry recessions. Still, some things haven't changed. Says Marcano: "The bottom line is people buy from people. This is my core belief,

and I try to instill this in our culture. And, it is apparent in our positive and long-term relationships with our customers."

About those long-term relationships. The longer one is in sales, the less likely their original customers are still around. Recently EMA was in the running for a deal with a major multinational corporation. Staff had traveled all over the country, visiting every site of the OEM. The day came to close the sale. As a senior manager at the customer gave the good news, he added the clincher: more than three decades earlier, Manny himself had taught him printed circuit board design.

"It goes back to the relationship," Marcano concluded. "Financially it's great, but morally and ethically I know I've done right by a lot of people. And here's a senior manager at a multibillion worldwide organization who remembered me helping him out 30 years ago when he started his career."

Maybe it wasn't so risky after all. □

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POLAR 'OPPOSITES': Software Co. Ties Tight Design-Fab Link

Resolving return loss problems, one call at a time.

BY CHELSEY DRYSDALE

Usually when presidents retire, they have a party and go home. Not Ken Taylor. He has stepped down as head of Polar Instruments' North American business unit three times and counting, but he keeps showing up to the office. Having an "enjoyable relationship with everybody makes it a great place to come to work," he told PCD&F during a visit to Polar's sales office near Portland, OR.

That elasticity has served both him and the company well. Polar's approach to customers is help them all, whether they have recently purchased one of the company's impedance or signal integrity software tools, or use older or obsolete products, or even don't use Polar products at all. Says Taylor: "Our objective is to have a satisfied customer base that speaks well of us."

In Portland, Taylor, Geoffrey Hazelett, vice president sales, and Lupita Maurer, product specialist, were eager to answer questions about the company Taylor says doesn't have "a single unhappy customer or user."

When asked about Polar Instruments' biggest technology concern, Taylor didn't hesitate: "Measuring loss. The industry can't agree on a single standard and hardware used to achieve this."

The problem, he elaborated, is no one wants to "share their knowledge with no promise of ROI. Every three to six months it changes. Each methodology hasn't lasted long enough to recoup investment."

Hazelett added, "Insertion loss testing has seen a variety of conflicting and competing methods." The tools all effectively measure loss, but vary significantly in methodology. "This is a bit of a problem for suppliers," he says, with fabricators wanting to have the tools their customers require.

"We are being asked to chase every tail in the dog park,"

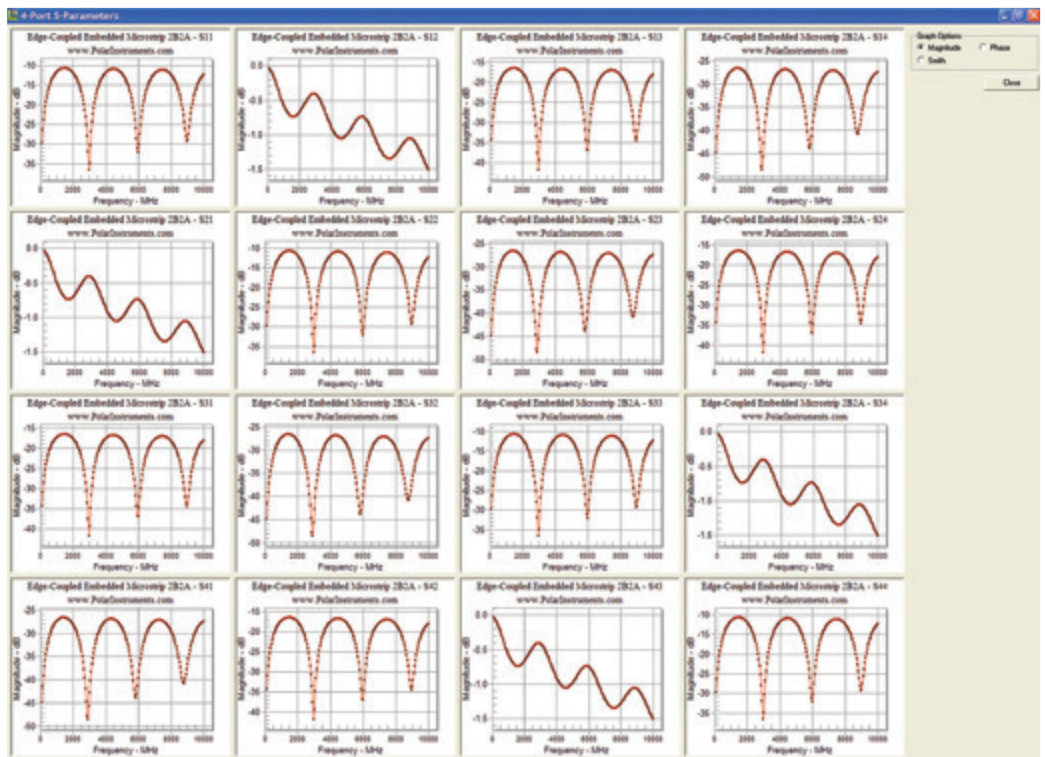


FIGURE 1. Polar's popular Si9000e PCB transmission line field solver shows the full range of two- and four-port S-parameters in a single chart window.

Hazelett said. “And we are. There isn’t one broadly accepted test method all OEMs want to use. Developing new test methods is academically interesting,” but the downside is the lack of industry consensus on a common approach. Still, the type of computer modeling Polar performs for insertion loss and impedance does expedite getting designs to work.

Another technology concern, Hazelett said, is copper roughness. “At lower frequencies, it wasn’t a problem,” he says. But with “different loss profiles, the panel was etched longer.” While Hazelett calls this the fabricator’s challenge, he added a designer’s recourse is to talk to their board shop. “Polar reports are a bridge between design and fabrication,” Maurer adds, saving headaches and time.

Polar develops tools for PCB design, fabrication and test. Hazelett said a bundle package with its Speedstack stackup design tool and the Si9000e insertion loss field solver is the firm’s most-popular product, followed by a controlled impedance test system and associated accessories, impedance modeling and documentation, and a time domain reflectometer (TDR).

Martyn Gaudion, CEO of Polar Instruments in the UK, also mentioned the company still sells its popular legacy product, the Toneohm, which performs fault finding on components on boards.

No Cold Calls

The company’s livelihood is based on reputation. The firm never makes cold calls; potential customers always contact them first, or they meet at trade shows.

Polar has existed for 20 years, focusing entirely on fabrication until 2008, Taylor explained. As the story goes, the leap to the front-end came when it began getting calls from designers who’d talked to fabricators because fabricators were telling designers, “Polar says....”

Working with designers prepared Polar for the recession, Taylor continued, by broadening its reach and lessening its dependence on a single market. Previously, “fab was interested in impedance. That was all.” Since designers also cared about insertion loss and return loss, Polar developed a field solver for those models 10 years ago. Now fabricators also want them, expanding their testing by using what was traditionally a designer’s tool.

Hazelett added, “Back in 2007 and 2008, we had Si8000 and then came out with Si9000. When we brought out insertion loss, it propelled growth years in 2008, 2009 and 2010 because we released a new tool and opened up a new market for ourselves.”

Today, they “focus a lot of attention on designers” with “adapted/enhanced tools,” Taylor said.

On the business side, Polar says it has carved out a niche that doesn’t have much competition. Hazelett is seeing growth in the North American fabrication industry. “We don’t feel any pressure [in terms of] competitors, pricing and margins. The industry is quite stable,” Taylor said. “Growth is in line with the economy. I don’t see anything negative at all.” Sales are boosted by continued demand in military/aerospace spending, Hazelett added.

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Hazelett says Polar has seen more onshoring recently, which “has resulted in more sales for [the US] and Asia offices.” (Polar Instruments is headquartered in the UK, and has offices in Austria and Singapore in addition to North America.)

Polar’s largest market in the US is the Silicon Valley, according to Taylor, where most of its customers have headquarters. The Midwest US and Canada are also big markets.

Ease-of-Use

Polar “approaches things by respecting customers’ opinions and basing product development on customer feedback,” said Hazelett. Polar is “approachable, honest, and open. We listen to our customers.”

As a result, the company plans to add a crosstalk feature to the field solver for both single-ended and differential pairs, and it has a tool in beta testing capable of performing several different S-parameter models or measurements – or both. The tool takes all the different models and actual measurements and displays them on one screen, Hazelett says.

“A lot of effort in the last few years has been moving forward insertion loss tools that are usable for designers and accessible for fabricators. A growing number of fabricators are stepping into the realm of insertion loss modeling,” Hazelett said. “That’s why we’ve kept the simple interface. Our tools

are designed to be used by nontechnical operators. They don’t require an hour of setup to get an answer.”

According to Hazelett, Polar wants to be known for its fast, accurate and easy-to-use products. “Polar is like light bulbs: [Customers] need light bulbs to see in the factory.” Taylor said this also applies to their customer service attitude. Perhaps that’s why he keeps unretiring. He can’t see a future without Polar. □

CHELSEY DRYSDALE is senior editor of PCD&F/CIRCUITS ASSEMBLY; cdrysdale@upmediagroup.com.

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Comparison of APERTURE DESIGNS, Solder Pastes, Nanocoatings and Print/Inspection Systems

Testing transfer efficiency and repeatability for microminiature devices down to 01005 discretes and 0.4mm BGAs. BY CHRYS SHEA, JENNIFER FIJALKOWSKI, RAYMOND WHITTIER, MICHAEL BUTLER, EDWARD NAUSS AND DEAN FIATO

High-reliability PCB assemblers face multiple challenges from the mainstream industry's migration to lead-free solders. One of the major challenges is in the solder paste itself. Solder paste manufacturers have been continuously developing new lead-free solder pastes for approximately 15 years. Few, if any solder suppliers, have introduced new SnPb solder pastes however, due largely to low market demand. Even if better SnPb paste formulations were available, changing them in a mission-critical application would require a great deal of due diligence and qualification testing.

The overall approach to SMT process optimization starts at the front of the assembly line and reviews each individual process moving down the line. Therefore, the method of optimizing production of discrete sizes 01005 to 0402 (Imperial) starts with optimizing the print.

The aperture design in the process of record (POR) for these component packages is shown in **FIGURE 1**. It is known as the “inverted home plate,” “crown,” “bowtie” or “Pac Man” aperture design. This is a common aperture design to minimize solder paste under the terminations, and therefore the propensity for mid-chip solder balls (MCSBs). It was identified in 2004¹ as the optimum aperture design to limit MCSBs with SnPb solder paste and 5 or 6 mil foils. At the time of the study, 0402 packages were the smallest available to test. Today they are mainstream, and many lessons have been learned. The acute angles in the corners, although radial, are

still very tight on 0402s and can create release issues for solder paste. The release issues can then lead to defect modes such as tombstoning, skews or non-wets, especially if placement is slightly off-target.

This experiment examines the printability of the POR aperture design with a simple rectangular one with a 10% area reduction for 0402s. Printability of the two aperture types are compared using transfer efficiency and coefficient of variation as output variables, on the assembler's production line using its qualified solder paste.

The next experiment does the same thing with the same solder paste, but in a laboratory environment as opposed to a production line, and uses an earlier model SPI machine from the same manufacturer.

The final test also takes place in the laboratory, comparing a slightly newer version of SnPb solder paste with a SnPb paste made with a “backwards-compatible” flux. The term backwards-compatible indicates the flux was designed for higher-temperature, lead-free products, but works well with SnPb solder powder and does not present electrochemical reliability concerns after a cooler, SnPb reflow cycle.

The assembler cannot bring the solder paste in-house to test, so the study looks for correlations in SPI readings on the control paste to determine if the experimental product will make enough impact on print quality to invest in the qualification process.

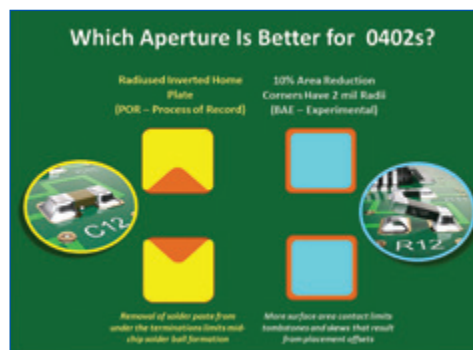


FIGURE 1. Aperture designs tested for 0402 (1005M).

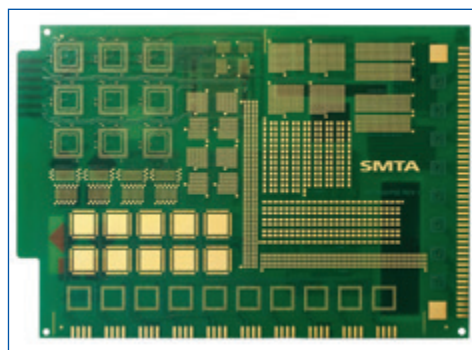


FIGURE 2. Test PCB.^{2, 3}

Experimental Design

Test vehicle. The test used the SMTA miniaturization test vehicle (FIGURE 2). It contains numerous miniaturized components; the ones primarily studied in this test are:

- Ten 0.5mm BGAs
- Nine 0.4mm BGAs
- Eight blocks of 01005 (0402M) components, 100 each
- Eight blocks of 0201 (0603M) components, 100 each
- Eight blocks of 0402 (1005M) components, 100 each

Sample sizes for each 10-print test were:

- 2880 0.5mm BGA deposits
- 5,580 0.4mm BGA deposits
- 16,000 0402 (1005M) deposits
- 16,000 0201 (0603M) deposits
- 16,000 01005 (0402M) deposits

Stencils. Six of each stencil thickness were tested, configured as described in TABLE 1. All stencils were laser-cut from fine-grain stainless steel and mounted at standard tension (~34N/cm). Six each were produced in 4 and 5 mil thicknesses. Three of each thickness had the POR aperture design (per IPC-7525⁴), and three had the experimental aperture design (abbreviated BAE in the data reduction). Each set of three stencils was then subdivided by coating. One had no coating (naked), one had ceramic coating (cured on), and one had a phosphate coating (wipe-on).

Based on experience with variability on the 0402 POR apertures and the sizes of 0201 and 01005 apertures, inverted home plate designs were not attempted for the smaller devices. Both the POR and BAE stencils used the same aperture sizes for 0201 and 01005 components. They are shown in TABLE 2.

Test execution. Each print test consisted of 10 prints, with a wipe between each print. The assembly line used:

- Vac, wet, oscillate
- Vac, dry, oscillate
- Dry, vac, oscillate

The laboratory used a dry/vac, dry/vac between prints.

The assembler’s production floor used a new EKRA Serio 4000 stencil printer certified by Cetaq⁵ and a Koh Young Aspire 3 with four projectors and a 12Mp camera at 15µm resolution.

The laboratory used a new MPM Edison 2 stencil

printer that had been recently certified via Cetaq, and a Koh Young 8030, a two-projector system with a 4Mp camera at 15µm resolution. It was later upgraded to an Aspire 3 with four projectors and a 12Mp camera at 10µm resolution between the incumbent paste print tests and the followup ones.

Both facilities used handheld ultrasonic stencil cleaners⁶ to ensure the best possible removal of residual solder paste from the apertures before transferring stencils to the other facility. Also, stencils were cleaned with ultrasonic cleaning systems upon arrival from the stencil manufacturer.

Note that it is important to clean new stencils before they are put into service to remove any residual burrs or contaminants from the cutting process. Stencils with cured-on coatings do not need to be cleaned upon arrival because they receive a thorough cleaning before the coating is applied. In fact, they should not be exposed to any harsh flux-dissolving solvents for 72 hr. after their cure, to permit complete cure of the coating.

Both the control and experimental solder pastes were Type 3, SnPb, no-clean products. Because the boards in this test were not populated, flat plates were used for tooling support on the production floor. Custom tooling plates were used in the laboratory. Again, because nothing was populated, the PCB support – a key element of the printing process – was excellent regardless of facility.

The production facility used metal squeegees mounted at 65° angles, and the laboratory used surgical steel squeegees mounted at 60° angles.

Data analysis. Data were output from the SPI machines into comma-separated files and opened and saved in Microsoft Excel format. In Excel, columns were added for:

- Stencil thickness (4 or 5)
- Aperture design (POR or BAE)
- Stencil coating (naked, cured-on or wipe-on)
- Solder paste (control or experimental)
- Location – Nashua, NH, or Hopkinton, MA.

Each facility produced 12 SPI files with 187,000 lines of data for each solder paste.

Results

This section contains detailed statistical results from the tests. For an overview of the findings, see the Discussion and Conclusions sections.

TABLE 1. Stencils Used in Test

STENCIL THICKNESS (MILS)	APERTURE SHAPE	COATING
4	POR - Inverted home plate 1:1 with pads	Wipe On
		Naked
		Cure On
4	BAE - squircle with 10% area reduction (01005 and 008004 are 1:1)	Wipe On
		Naked
		Cure On
5	POR - Inverted home plate 1:1 with pads	Wipe On
		Naked
		Cure On
5	BAE - squircle with 10% area reduction (01005 and 008004 are 1:1)	Wipe On
		Naked
		Cure On

TABLE 2. Aperture and Pad Sizes for Miniaturized Discretes

PACKAGE	0201 (0603M)	01005 (0402 M)
Pad Size	12 x 15 mil	8 x 8 mil
Aperture Size	10.8 x 13.5 mil	8 X 8 mil
Area Ratio 4 mil	0.75	0.50
Area Ratio 5 mil	0.60	0.40

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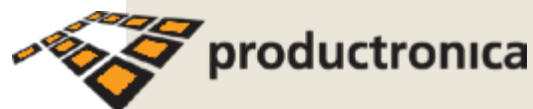
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Key findings. The purpose of the study was to answer specific questions about process changes before implementing any on high-reliability products, especially those currently in production. Questions included:

- What is the impact of migrating from 5 mil foils to 4 mil foils?
- Would different aperture designs improve the repeatability of the print process?
- What is the smallest device we can repeatably print with the current solder paste formulation?
- Would qualifying a new solder paste provide enough quality and cost improvement to justify the effort?

Foil thickness. Neither foil thickness could adequately print 01005s with the production solder paste on the production line. For both foil thicknesses and all surface treatments, coefficients of variation (CVs) ranged from 25 to 45%. The CV is simply the standard deviation divided by the mean, expressed as a percent. Typically, less than 10% is preferred, 10 to 15% is considered acceptable or marginal, and greater than 15% is considered unacceptable. These features were not expected to print well, given their area ratios and the older, Type 3 solder paste.

The 0201s showed good capability for all stencil types. CVs ranged from 5.8 to 7.0, all in the preferred range. The best performer was the cured-on coating. In the boxplots (FIGURE 3 and 4), the apertures labeled BAE are the experimental (short for BAE modifications), and the POR are the current process of record that reflects the current aperture library.

The volumes are relatively the same between the BAE and POR apertures. They should be, because in the case of 0201s, they are the same.

The 4 mil foil prints a much tighter distribution than the 5 mil foil. The 5 mil foil also tends to produce more insufficients (lower area ratio). The 5 mil foil deposits a mean volume of 630 mil³, whereas the 4 mil foil deposits approximately 500 mil³. The roughly 20% reduction in solder volume is not expected to impact solder joint integrity, as the 500 mil³ average is still typical for the package type. The reduction in variation – especially the limiting of insufficient deposits that cause tombstone, skew and non-wet defects – should improve end-of line quality. A 4 mil foil is preferred for 0201s for higher quality output.

Aperture designs. Two different aperture designs were tested on two different component types. For 0402 components, the POR aperture is the radiused inverted home plate, and the BAE aperture is a rectangle with radiused corners, also known as the “squircle.” The corner radii are 2 mil; the radii help prevent solder paste buildup in the aperture corners. For the 0.5mm BGA components, the POR aperture is a circle at 1:1 with the pad (10 mil), and the BAE aperture is a squiracle the same size with 2 mil radii.

Radiused rectangle vs. inverted homeplate on 0402s. FIGURES 5 and 6 show the boxplots for 4 and 5 mil stencils with the cured-on coating. Both aperture designs on both stencil thicknesses showed good capability, with CVs well below 10%. Both aperture designs showed similar mean volumes on their respective stencil thicknesses, despite having different geometries. The reduction of volume of approximately 20% when thinning the stencil 20%, with no impact on variation, indicates area ratio is not a factor on the 0402s.

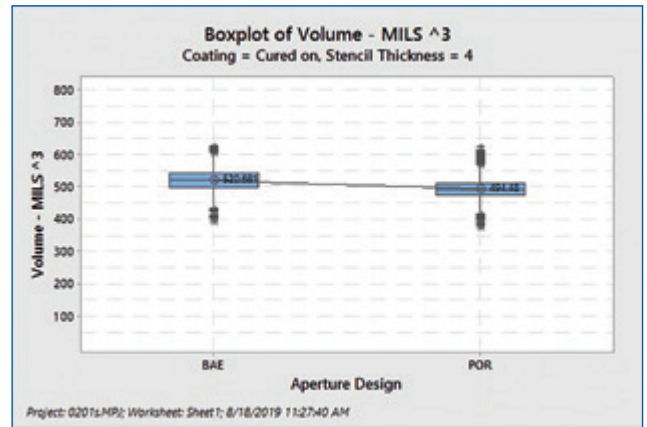


FIGURE 3. Boxplot and statistics for 0201 prints with a 4 mil foil and cured-on coating.

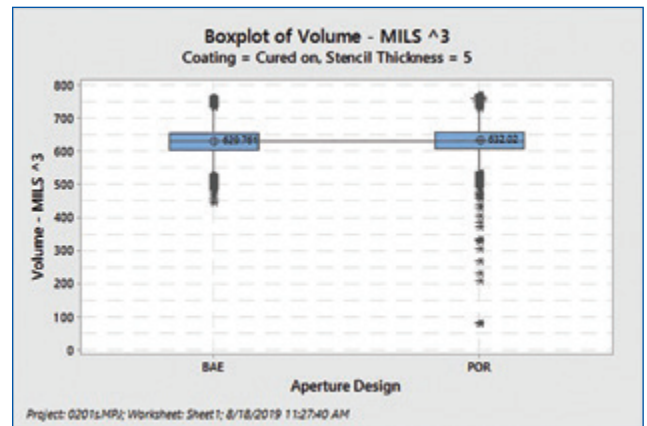


FIGURE 4. Boxplot and statistics for 0201 prints with a 5 mil foil and cured-on coating.

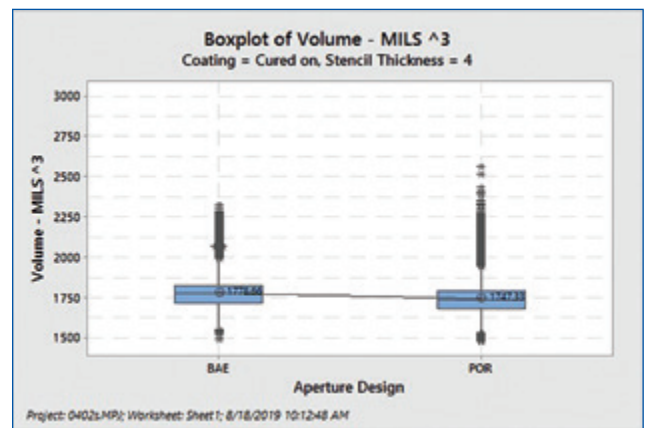


FIGURE 5. Boxplot and statistics for 0402 prints with a 4 mil foil and cured-on coating.

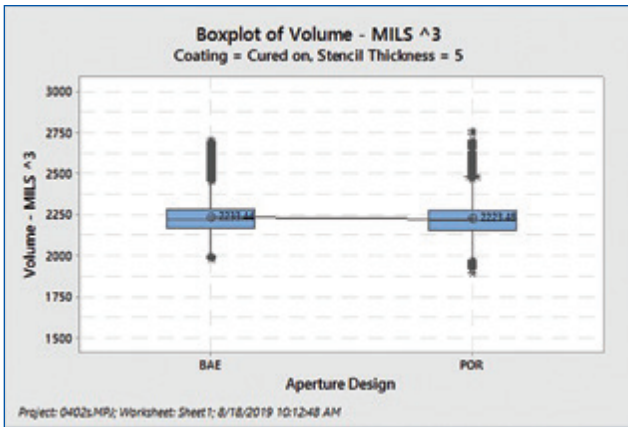


FIGURE 6. Boxplot and statistics for 0402 prints with a 5 mil foil and cured-on coating.

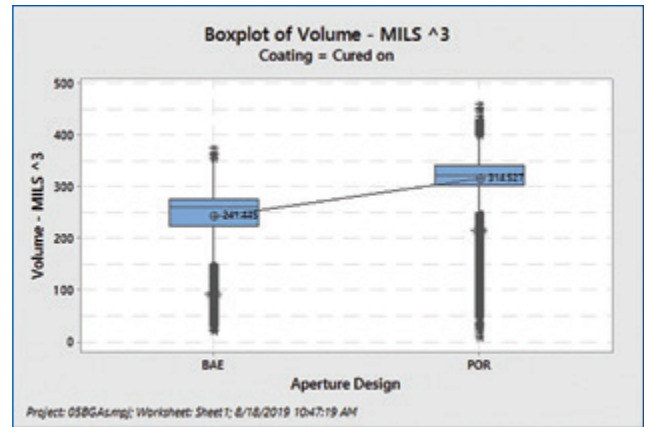


FIGURE 7. Boxplot and statistics for 0.5mm BGA prints with a 4 mil foil and cured-on coating.

Either stencil thickness or aperture design appears equally viable from a print capability perspective. Therefore, moving to a POR aperture or 4 mil foil will not negatively impact print quality, and merits investigation into its effects on end-of-line yield, particularly with respect to the production of tombstone/skew vs. MCSB defects.

Circle vs. radiused square for BGAs. In the case of the 0.5mm BGAs, the circular aperture has a 10 mil diameter, and the squircle aperture also has a 10 mil side length, with 2 mil radii. Data were only analyzed for the 4 mil foil. If the 4 mil foil showed good capability, the 5 mil would have been analyzed. Data for the 4 mil foil with cured-on coating are shown in **FIGURE 7**. The circular (POR) aperture produced higher volumes, with less variation, but more outliers than the squircle (BAE) aperture; however, both have unacceptable CVs.



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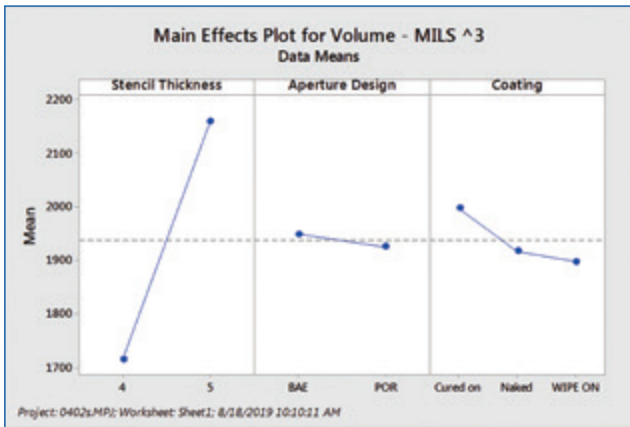


FIGURE 8. Main effects plot for volume on 0402s on production line.

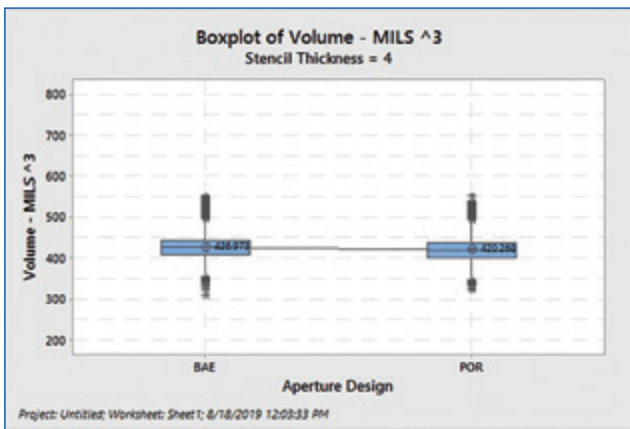


FIGURE 9. Boxplot and statistics for 0201 components printed with a 4 mil foil in laboratory.

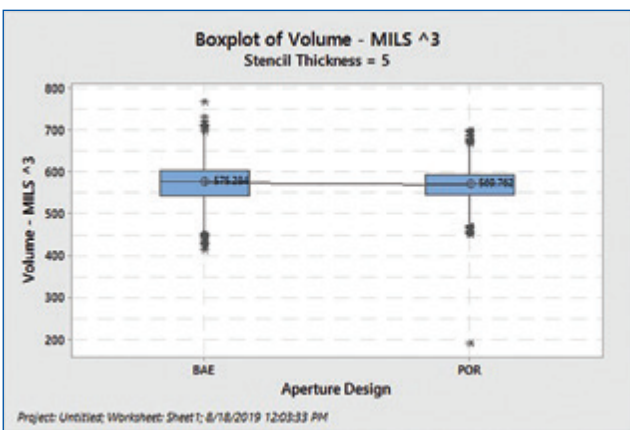


FIGURE 10. Boxplot and statistics for 0201 components printed with a 5 mil foil in laboratory.

sets, i.e., 0201, 0402 and 0.5mm BGA apertures with cured-on coating, were compared. These tests used the same SnPb solder paste as the assembler.

FIGURES 9 and **10** show the data for the 0201s from the laboratory for comparison with data in Figures 3 and 4 generated on the assembler’s production line. The assembly line and laboratory both produced prints with CVs of approximately 6%. The

Previous studies^{7,8} have shown typical 0.5mm BGA volumes in the 300 to 350 mil³ range for newer solder paste formulations. If the variations in these datasets were acceptable, the larger volume would likely be preferred. However, no realistic conclusions regarding volume and variation can be made with CVs over 15%.

The 0.5mm BGA print process is currently in place in production using POR apertures. Based on these test data, it is recommended to maintain the POR apertures while investigating other ways to improve print performance. Given the production process already uses the best-performing stencil technology, and best-in-class tooling and squeegee blades, and the printers are certified by a third party, the remaining option is to investigate the performance of newer solder paste formulations.

The 0.4mm BGAs showed complete incapability on the 4 mil foils, with CVs upward of 50% for cured-on coating, 60% for wipe-on coating and 80% for no coating. No inferences or conclusions can be drawn based on this dataset.

For reference, the POR aperture on the 0.4mm BGAs is an 8 mil circle; the BAE experimental is a 7.5 mil squircle with 2 mil radii on the corners.

Coating comparison. **FIGURE 8** shows the main effects plot for volume for 0402 components. The trends shown for the 0402s are mimicked throughout the results for all datasets. The main driver for volume differences is foil thickness. Secondary to that, cured-on coatings showed higher volumes than naked stencils or wipe-on coatings, in that order. Not shown in the main effects plot are the variations of each coating. Review of all the data shows the cured-on coatings produced lower CVs than the wipe-on coatings or naked stencils, in that order.

These test results showed the print process is robust down to 0201 components, using the current equipment and solder paste. It also shows that 4 mil foils are better than 5 mil foils for this package size, because the 5 mil foils tend to produce more insufficient deposits. The 0.5mm BGAs were borderline marginal at best using the 4 mil foil with cured-on coating. They showed lower-than-expected volumes and 15% CV.

Note the population density of this PCB puts more demands on the solder paste than would a typical production PCB. A print process considered borderline on this PCB layout will likely perform better on less densely populated production boards with fewer apertures and less fine-feature component types.

Will moving to a newer formulation improve the process? Qualifying a new solder paste requires tremendous effort for any PCB assembler, let alone a high-reliability one. When considering undertaking such a substantial mission, it is important to understand if it is worth it.

To understand if a newer formulation SnPb solder paste will afford a wider process window, sample tests were run in a nearby laboratory. First, the current production solder paste was processed, then the newer products. The strongest data

volume readings on the line were higher than those in the lab. This could possibly be due to the difference in SPI machines or the difference in printers. As with the previous 0201 data, the volumes are similar because the apertures are similar.

FIGURES 11 and **12** show the data for the 0402s from the laboratory, for comparison with data in Figures 5 and 6 generated on the assembler's production line. As with the 0201s, the CVs of the two processes are very close. And again, the mean of the volumes is lower for the lab than the assembly line.

The 0.5mm BGA, the finest feature to be compared, showed far less variation in the laboratory than on the assembly line. CVs for both aperture designs were acceptable. However, the distribution is much tighter for the BAE aperture (squirrelle) than for the POR one (round).

Considering this a viable dataset based on its CV of ~10%, the BAE aperture (squirrelle) is strongly preferred. Similar to the assembly line tests, it has fewer outliers than the POR, which produces many more insufficients. Also similar to the assembly line tests, the POR averages higher volumes. Similar to the comparisons of the 0201s and 0402s, the average volumes measured in the lab were lower than those measured on the line.

In an overall comparison of the datasets for 0402, 0201 and 0.5mm BGA, the assembly line readings were consistently higher. The variations however were consistent, as were the main effects. A direct statistical correlation cannot be established, but the trends are consistent.

Next, a follow-up run with two potential replacement solder pastes were printed in the laboratory using the same stencils with cured-on coatings. Because the 0.5mm BGA and 0201s printed better with a 4 mil foil, and the foil thickness had no impact on print quality for 0402s, only the 4 mil foils were print tested.

Newer SnPb or backwards-compatible Pb-free flux with SnPb powder? Two solder paste “upgrade” options are available to the assembler:

- Investigate a newer formulation SnPb solder paste that is well known as an excellent printing product.
- Investigate a formulation that was developed for Pb-free solders but provides the needed electrochemical reliability when used with SnPb alloy in SnPb reflow profiles.

Both were print tested in the laboratory. The results are shown in **FIGURES 14** to **16**.

All the aperture sizes tested (0.4mm BGA and 01005 not shown) demonstrated similar trends in the data: very tight distributions with an unusually high number of outliers. Comparing the 0.5mm BGA print volumes for BAE apertures shown in Figure 16 against those in Figures 7 and 13 exemplifies the differences.

The follow-up dataset printed in the laboratory – the newer SnPb and Pb-free/backwards-compatible solder pastes – was on a new lot of test boards. Subsequent investigation of the boards revealed the solder mask was higher than the pads, creating contact and gasketing problems between the stencil and pad. This provides a highly plausible explanation for the atypical distribution of the volume data. An example of solder mask higher than the PCB pad is shown in **FIGURE 17**.

Additionally, between the original print tests and the final set on the newer solder pastes, the SPI in the laboratory was upgraded to a Koh Young Aspire 3 with 10µm resolution and four 12MP cameras. It is faster and more accurate than the earlier model used

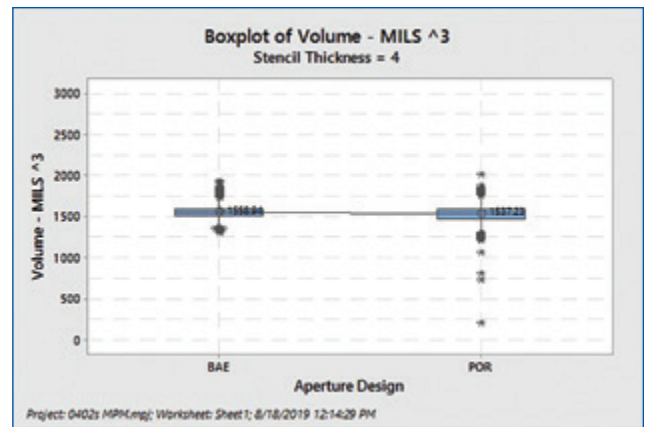


FIGURE 11. Boxplot and statistics for 0402 components printed with a 4 mil foil in laboratory.

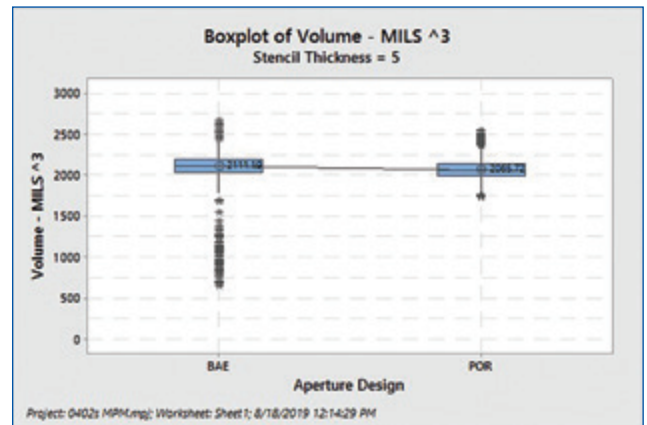


FIGURE 12. Boxplot and statistics for 0402 components printed with a 5 mil foil in laboratory.

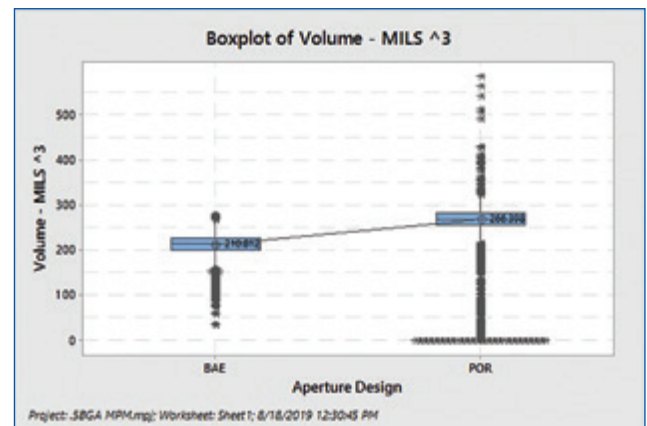


FIGURE 13. Boxplot and statistics for 0.5mm BGA components printed with a 4 mil foil in laboratory.

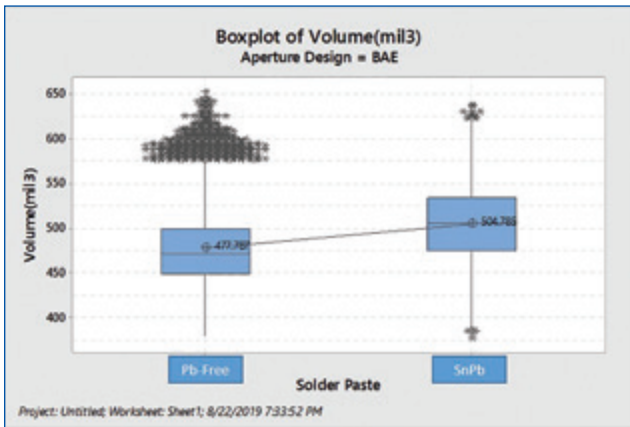


FIGURE 14. Boxplot and statistics for 0201 volumes with newer solder pastes.

in the main part of the laboratory study. There is little likelihood that the new machine contributed to the different distribution trends, however, other than measuring them more accurately than its predecessor.

The last two datasets for the newer solder pastes showed extremely good repeatability, despite the print deficit of solder mask above the pads on the second set of test PCBs.

Discussion

If each print process is evaluated using criteria based on CVs, where less than 10% is considered capable, 10 to 15% is considered marginal, and over 15% is considered not capable, performance can be easily categorized.

On the assembler's line using the current SnPb solder paste, this test showed the process was completely capable of printing 0201 and 0402 components, preferably with a 4 mil nano-coated foil to help get sufficient release on the 0201s. It also showed a borderline marginal/incapable CV of 15.4% on 0.5mm BGAs with the POR aperture only, and complete incapability on smaller components. Again, it should be noted the capabilities will improve on less densely populated production PCBs, as this test layout is designed to stress solder paste.

On the laboratory line using the current SnPb solder paste, the process was also capable of 0402, 0201 and marginally capable 0.5mm BGAs (11% CV), regardless of aperture design. The volumes were slightly lower in all cases, and the CVs were much lower on the smaller apertures. The differences could be attributed to either the printer or the SPI machines.

The process improved with the newer SnPb solder paste formulation, which demonstrated good capability on 0.5mm BGAs and good/marginal on 01005s. Finally, the newest solder paste performed the best, showing good capability on all component sizes, including 0.4mm BGA and 01005, despite the handicap of excessive solder mask.

The best print performance was realized with the cured-on nanocoating, followed by the wipe-on nanocoating, with the naked stencil consistently showing the most variation. The assembler currently uses the cured-on nanocoating as the preferred finish on all its stencils.

TABLE 3 summarizes the results for a 4 mil foil with cured-on nanocoating.

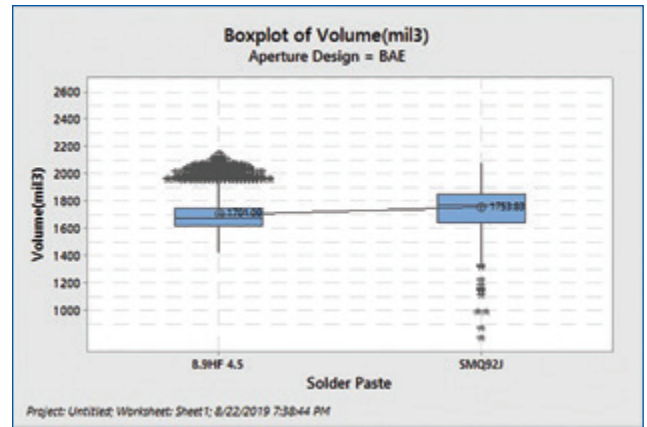


FIGURE 15. Boxplot and statistics for 0402 volumes with newer solder pastes.

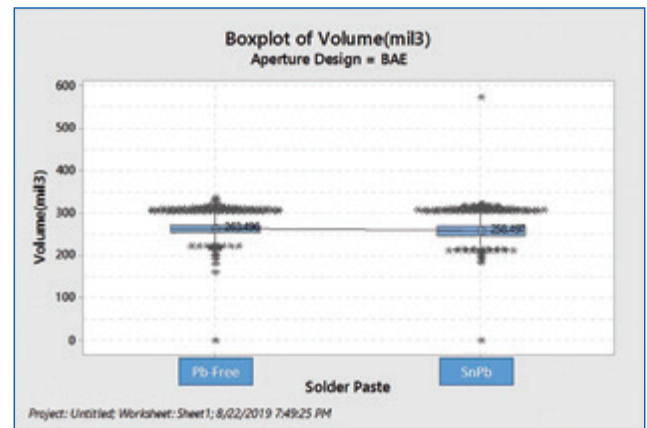


FIGURE 16. Boxplot and statistics for 0.5mm BGA volumes with newer solder pastes.

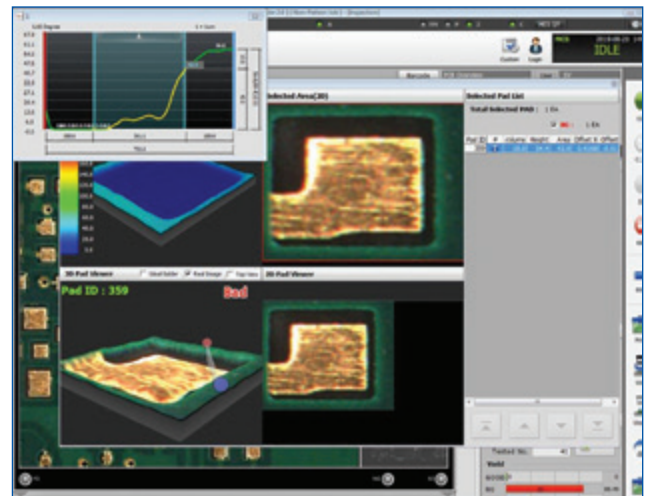


FIGURE 17. SPI screenshot showing solder mask taller than PCB pad, which prevents proper gasketing of the stencil to the board.

Conclusions

The information sought and gained by the test includes:

What is the impact of migrating from 5 mil foils to 4 mil foils? Reducing the stencil thickness from 5 mil to 4 mil reduces the volume on the 0402s by approximately 20% but maintains excellent repeatability and provides enough solder to form a proper joint. Reducing the thickness helps improve the 0201 process by eliminating insufficient deposits that lead to wetting problems. It also helps the 0.5 and 0.4mm BGA deposition processes in a similar fashion.

The 0.5mm and 0.4mm BGAs showed poor print performance with the incumbent solder paste on 4 mil foils and complete incapability on 5 mil foils, but fared better with the newer solder paste formulations, particularly on the 4 mil foils. The main differences between BAE and POR aperture outputs on the 0.5mm deposits were the volumes, not the repeatability, as both showed similar CVs. The two designs' performance was almost identical on the 0.4mm deposits with the only capable solder paste (the newest).

TABLE 3. Solder Paste Print Capability

SOLDER PASTE	COMPONENT SIZE	APERTURE DESIGN	MEAN VOLUME (CU MIL)	CV - %	CAPABLE?
Current (Production Line)	1005	POR/BAE are the same	159	53	No
	201	POR/BAE are the same	520	5.9	Yes
	402	POR - IPC 7525	1747	5.6	Yes
		BAE Experimental	1779	5	Yes
	05BGA	POR - IPC 7525	315	15	Marginal
		BAE Experimental	241	23	No
	04BGA	POR - IPC 7525	105	52	No
		BAE Experimental	108	54	No
Current (Lab)	1005	POR/BAE are the same	141	17	No
	201	POR/BAE are the same	427	6.7	Yes
	402	POR - IPC 7525	1537	5.8	Yes
		BAE Experimental	1559	5	Yes
	05BGA	POR - IPC 7525	266	11	Marginal
		BAE Experimental	211	11	Marginal
	04BGA	POR - IPC 7525	100	26	No
		BAE Experimental	96	28	No
Newer Gen SnPb (Lab)	1005	POR/BAE are the same	197	10.4	Marginal
	201	POR/BAE are the same	505	8.4	Yes
	402	POR - IPC 7525	1686	5.7	Yes
		BAE Experimental	1754	7.3	Yes
	05BGA	POR - IPC 7525	310	4.8	Yes
		BAE Experimental	259	6.3	Yes
	04BGA	POR - IPC 7525	145	17	No
		BAE Experimental	151	25	No
Newest Pb-Free SnPb Compatible (Lab)	1005	POR/BAE are the same	195	8.7	Yes
	201	POR/BAE are the same	478	8.3	Yes
	402	POR - IPC 7525	1768	5.8	Yes
		BAE Experimental	1701	7	Yes
	05BGA	POR - IPC 7525	322	4.9	Yes
		BAE Experimental	264	5.8	Yes
	04BGA	POR - IPC 7525	162	8.8	Yes
		BAE Experimental	166	8.5	Yes

Note: Data for 4 mil foil with cured-on coating

Would different aperture designs improve the repeatability of the print process? For 0402s, the POR and BAE apertures deposit equivalent amounts of solder paste, but the BAE experimental aperture is believed to limit tombstone defects better than the POR. Because the volumes are similar, it should be easy to implement on an assembly line to see if it helps with tombstone and other wetting-related defects.

For BGAs, the POR is currently better for the 0.5mm prints, but neither aperture is acceptable for 0.4mm prints in the current process. With the newest solder paste, the 0.5mm benefited from the BAE experimental aperture, whereas the 0.4mm did not show a significant difference between the two designs.

What is the smallest device we can repeatably print with the current solder paste formulation?

Answer: 0201s. A 4 mil foil provides better quality in terms of fewer insufficient deposit volumes.

Would qualifying a new solder paste provide enough quality and cost improvement to justify the effort? Based on the findings in the laboratory, the assembler can gain a great deal of print capability by modernizing its solder paste formulation. Increases in print capability lead directly to decreases in defects, rework, scrap and lost time.

A tremendous amount of effort is required to change solder pastes, so the increase in productivity must be weighed against the investment and timed appropriately to continue the flow of new product introductions with miniaturized components. If the investment is made, the obvious choice would be to qualify the newest flux formulation in the backwards-compatible SnPb solder paste. The print performance difference is considerable and will eventually be needed as miniaturization continues.

Future Work

The stencils have been preserved to continue studying print capability on the fine features. The assembler may use them to further investigate new solder paste products to improve the assembly process. Additionally, other solder pastes may be printed in similar tests to benchmark performance among popular products. □

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Dedicated vs. Flexible BOARD SUPPORT

A good seal between stencil aperture and solder pad ensures the best solder paste deposition. BY MIGUEL ARROYO COLOMER

ENHANCED FUNCTIONALITY DEMANDED by today's increasingly miniaturized PCBAs has added to their complexity and density but has also decreased their rigidity. PCBs used to be more rigid and less dense. Solder printing of double-sided boards was performed using standard support pins. In some cases, customized tooling was required to ensure board support.

Today, dedicated tooling and flexible support systems are more frequently employed than ever before. They are easy to set up and provide excellent support. This is in part because the support pins typically supplied with the printer are often perceived as being too difficult to set up, and there never seem to be enough to properly support the board.

Why are organizations moving toward dedicated or flexible supports, instead of the inexpensive support pins that come with the equipment? PCB assemblers have found the process of setting up the support pins depends highly on the user. The manufacturing engineer can document the best methodology for determining the optimum locations for best board support. Implementation will be the responsibility of the operator, however.

Manual support pins are efficient and flexible. That flexibility is also its vulnerability, however. A single missing or misplaced support pin can severely impact product quality. A missing pin can change the PCB rigidity, causing more variation in solder paste deposition (**FIGURE 2**). This variation is sometimes overlooked, especially if it does not result in a visual defect after the print. A misplaced support pin can damage a component on the bottom side of the board and thereby change the board contour (**FIGURE 3**). The defects caused in both instances may emerge later in the process, i.e., post reflow. This is one reason manufacturers are moving away from support pins and opting for a different solution.

One solution is a system of dedicated support plates. These are easy to set up and guarantee repeatable results. However, they require time for development (design) and are difficult to modify once delivered. Not every facility has a machine shop available, so the plates must be fabricated externally. Some products cannot be shipped outside the facility due to certain

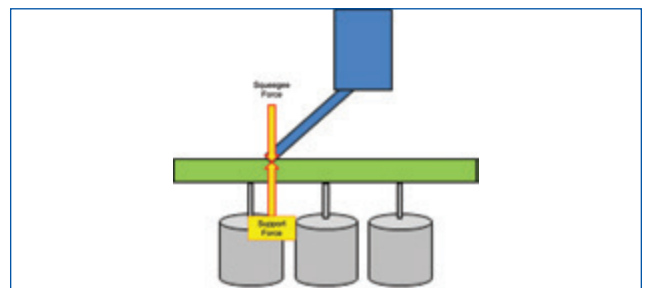


FIGURE 1. Ideal forces at one point. Note there are only two forces, each cancelling the other.

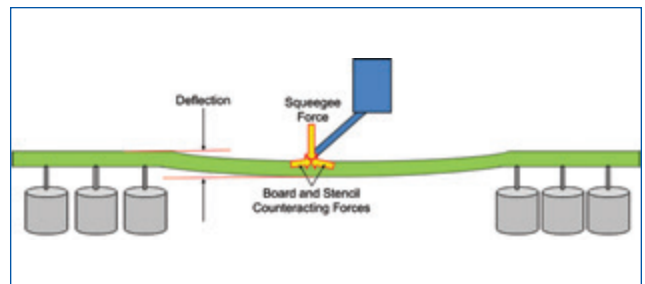


FIGURE 2. When there is not enough support, the stencil/board counteracts the squeegee force.

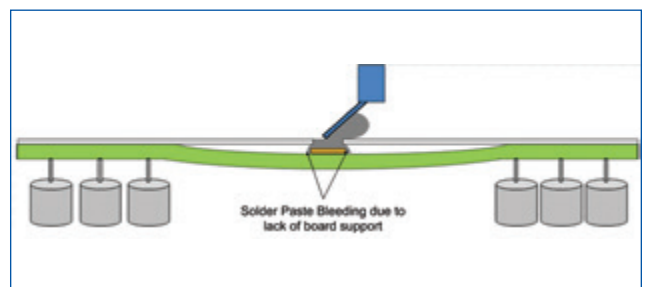


FIGURE 3. One effect of insufficient PCB support is misregistration between apertures and solder pads. There is a poor seal between them, and solder paste bleeds out from under the stencil aperture.



FIGURE 4. Flexible support system. Note how the system conforms to the PCB bottom's profile.

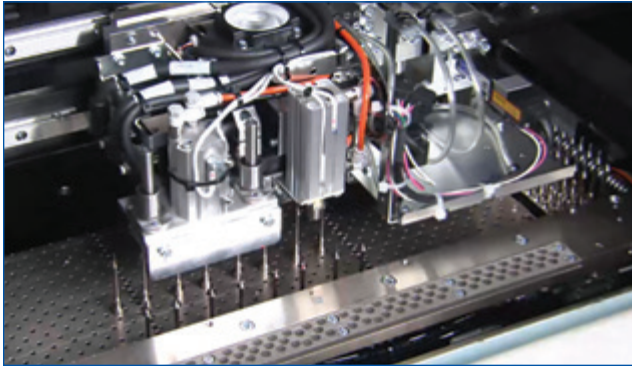


FIGURE 5. Automatic support system. This system places, removes and verifies pin position.

regulations. Therefore, the process engineer must provide the key dimensions required to design and manufacture them without a sample PCB. A lead time is also associated with this process. The logistics and traceability of these plates are also critical. They must be tagged, and all changes documented and implemented across all the plates created for the same product. Every product will require a set, and if there are multiple lines running the same product, a set for each line is required. These

plates must be properly stored and maintained, since printing process defects may surface downstream. A quality improvement that requires a modification of a plate will be expensive and take time to implement.

Flexible tooling lies between the two extremes in the middle of the spectrum. As named, it is flexible and easy to set. Flexible tooling works well when properly maintained, and when the minimum number of modules required per product is installed. These systems require integration with the screen printers. This is easy to do and best done before delivery at the screen printer manufacturer's site. These systems are not especially effective when the PCBs are extremely warped. This is because the systems conform to the board's contours, and as a result, warpage is difficult to correct once the system is locked (FIGURE 4).

Support systems like the one shown in Figure 4 have advantages and disadvantages. Another way to make the support pin approach more attractive is with automation (FIGURE 5). The pins have the rigidity of the dedicated plate, and using automated pin placement, it becomes a flexible support system. With the aid of software, pin locations are assigned, and the screen printer automatically places them in the predetermined location. The system also checks to ascertain that all pins are in their proper locations. Also, pins can be added in the program if more support is required at a specific location (FIGURE 6). Once the program is modified and propagated across the machine, the new support pin array will be executed automatically, without the need for operator intervention.

Our hypothesis: There is no significant solder paste deposition variation between a dedicated support and an array of support pins.

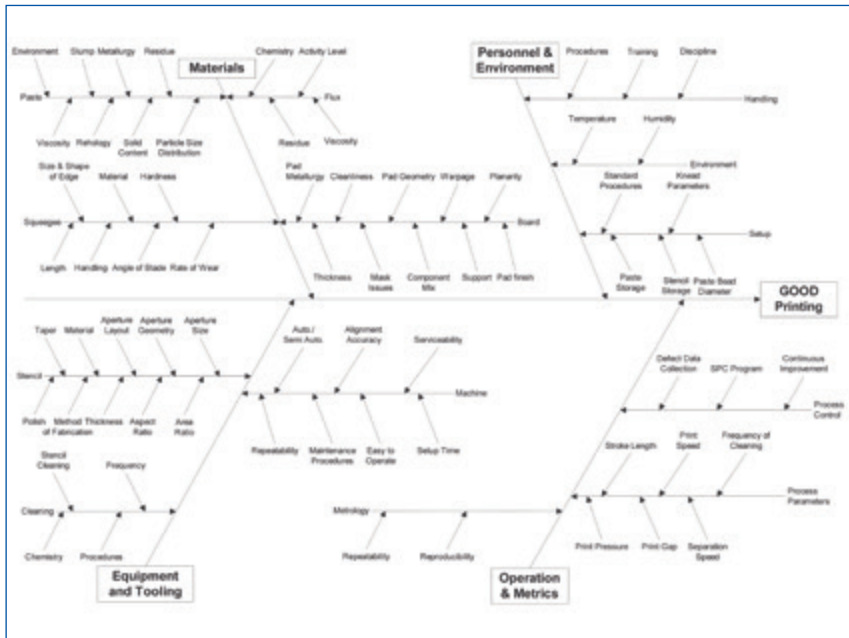


FIGURE 6. Cause-and-effect (fishbone) diagram of a good print. Board support is a key factor in achieving a good print.

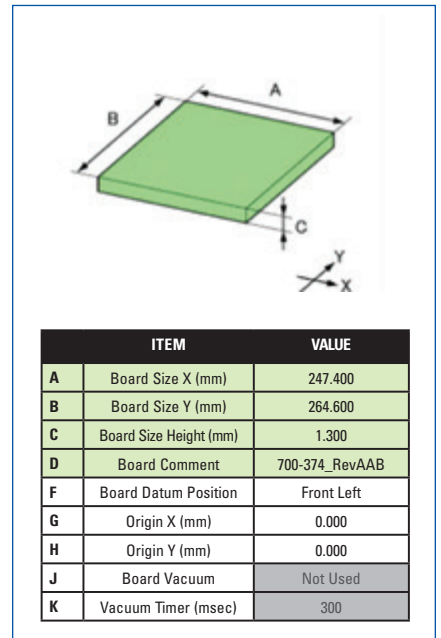


FIGURE 7. PCBA panel dimensions.

Experiment

To test our hypothesis, a double-sided board (FIGURE 7) was printed using a dedicated support plate (FIGURE 8), and then with support pins (FIGURE 9). A customer provided the board, dedicated support plate, stencil, and screen printer program. Thus, we can assume the user fine-tuned and validated the configuration. Two different configurations were evaluated.

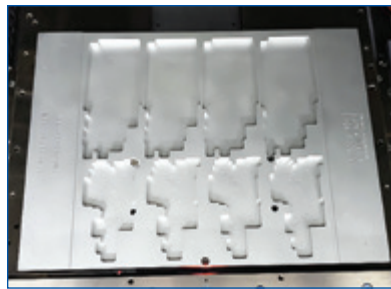


FIGURE 8. The dedicated support plate.

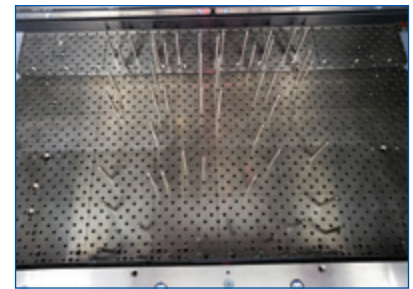


FIGURE 9. The support pin array.

The first configuration (baseline):

- Customer’s dedicated support plate
- Customer’s screen printer program
- Customer’s 5 mil-stencil, laser cut, and with nanocoating (Nanoslic) (FIGURE 10)
- 10 PCB assemblies with components on the first side
 - 4-up panel, with dimensions x = 247.4mm, y = 264.6mm, and t (thickness) = 1.30mm. The smallest passive component was an 0402, and the smallest pitch was 20 mils.
- Koki S3X58-M406-3 Type IV solder paste.

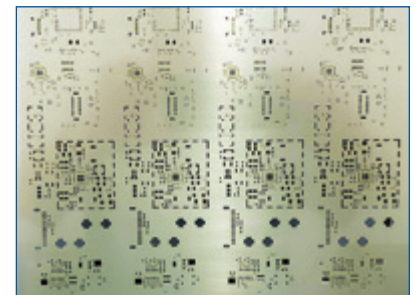


FIGURE 10. Bottom side of the stencil used for the evaluation.

The second configuration:

- Screen printer support pins – 76 support pins were used
- Customer’s screen printer program
- Customer’s 5 mil-stencil, laser cut, with a lubricating nanocoating (NanoSlic)
- 10 PCB assemblies with components on the first side
 - 4-up panel, with dimensions x = 247.4mm, y = 264.6mm, and t (thickness) = 1.30mm. The smallest passive component was an 0402, and the smallest pitch was 20 mils.
 - To avoid any noise during solder-paste deposition measurement, a new group of the same PCBAs were used to ensure there will be no noise in the measurements due to residues left during PCBA cleaning.
- Koki S3X58-M406-3 Type IV solder paste.

A new jar of solder paste was used to eliminate any interaction between the solder paste and print process that might skew the results.

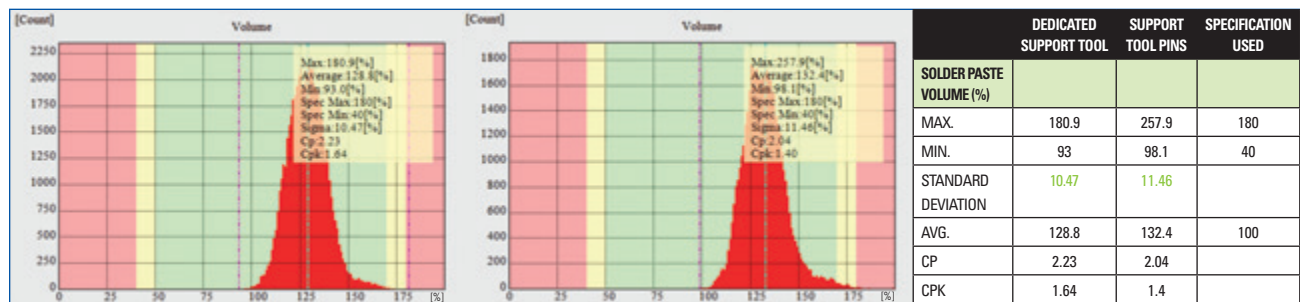


FIGURE 11. Dedicated support plate vs. pins: volume results.

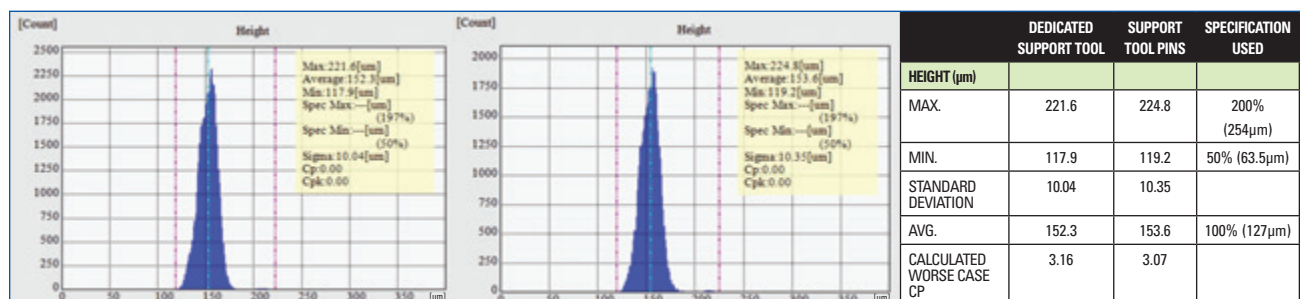


FIGURE 12. Dedicated support plate vs. pins: height results.

All printed PCBAs were inspected with a solder paste inspection (SPI) machine. The same SPI program was used for both conditions. Recorded data were analyzed to determine differences in the resulting print between the use of a dedicated support plate versus support pins.

Results

All data were analyzed using Yamaha YSi-SP SPI offline SPC software. The results shown in **FIGURES 11 to 14** are derived directly from the SPI application. Upon examination, no meaningful difference between the dedicated support plate and support pin printing results could be discerned.

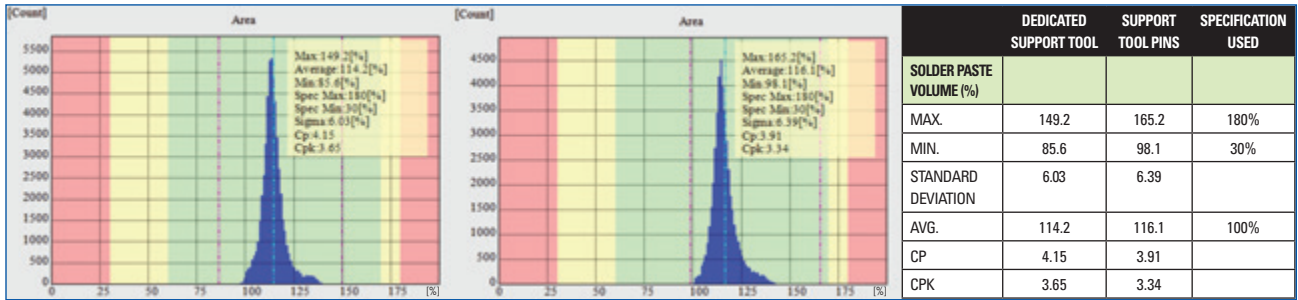


FIGURE 13. Dedicated support plate vs. pins: area results.

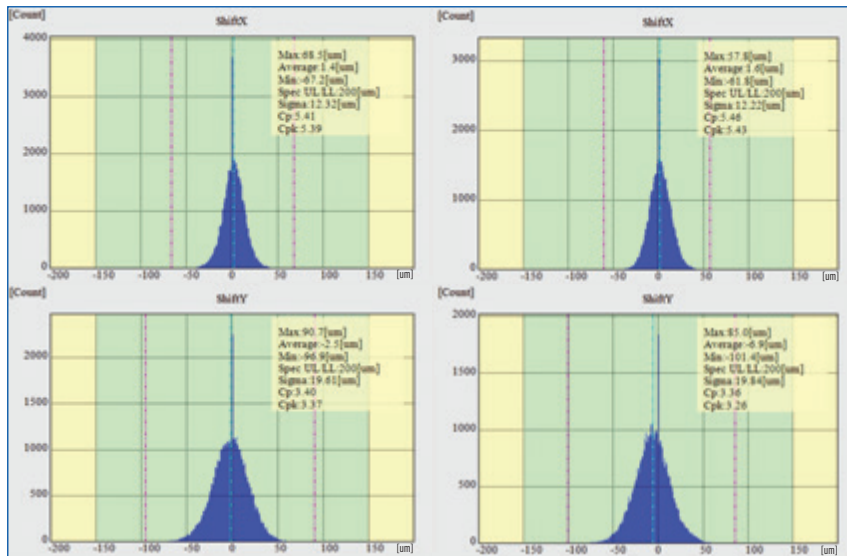


FIGURE 14. Dedicated support plate vs. pins: offset results.

TABLE 1. Dedicated Support Plate vs. Pins Offset Results

	DEDICATED SUPPORT TOOL	SUPPORT TOOL PINS	SPECIFICATION USED
SHIFT X (µm)			
Max.	68.5	57.8	180
Min.	-67.2	-61.8	-180
Standard Deviation	12.32	12.22	
Avg.	1.4	1.6	0
Cp	5.41	5.46	
Cpk	5.39	5.43	

	DEDICATED SUPPORT TOOL	SUPPORT TOOL PINS	SPECIFICATION USED
SHIFT Y (µm)			
Max.	90.7	85	180
Min.	-96.9	-101.4	-180
Standard Deviation	19.61	19.84	
Avg.	2.5	-6.9	0
Cp	3.4	3.36	
Cpk	3.37	3.26	

Conclusion

There is no significant difference between the results obtained with either support media (dedicated) or with pins. Therefore, we see that support pins can provide optimum board support during printing, without compromising the gasket between the PCB and stencil. Based on these results, we are proceeding to run products using only support pins. This will greatly reduce the time, resources and cost required to build a dedicated support plate for each product.

Automated support pin placement ensures the pin array will be the same every time, and the program is loaded without need for operator intervention. It is shown that an array of support pins can provide excellent support. Therefore, the quality of the solder deposition on the PCB will yield good results at the end of the process, every time a product is set up.

The advantage of the dedicated tooling plate is it provides the same support across the PCB every time and is easy to set up. However, it is not easy to modify and creates inventory. A screen printer that automatically sets the support pins will eliminate tooling inventory, provide process flexibility, and preserve yield quality. □

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Conformally Coated Chip Caps

While coatings are typically used on boards, some choose to coat components as well.

THIS MONTH WE show manual conformal coating on one component. One optical example is shown under normal lighting and then under UV light, to show the tracer added in coatings to allow easy manual or automatic inspection. This is not a defect. I asked if this was intended, however, as it was unusual.

Traditionally, coatings are used to protect circuit boards in humid environments and more so in condensing conditions to prevent corrosion. On some occasions design engineers also use coatings to provide that little stability.

FIGURE 1 shows a chip component manually coated with conformal coating. It was a specific requirement of the design engineer that this part required coating.

FIGURE 2 shows the capacitor under UV light. Manual coating has completely covered the part and the edges of the capacitor. It may not be pretty, but it is acceptable and met the design engineer's requirement.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at [youtube.com/user/mrbobwillis](https://www.youtube.com/user/mrbobwillis). □



FIGURE 1. A capacitor manually coated with conformal coating under normal lighting.

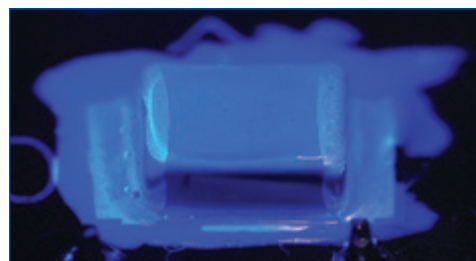


FIGURE 2. The same capacitor under UV light.

BOB WILLIS

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Clarifying Through-Hole Fill Levels

IPC-STD-001 is revising criteria for voiding and fill percentage.

IN MY SEPTEMBER column, I spoke with Dave Hillman about IPC committee work on voiding guidelines for QFN central pad terminations. But he also told me the J-STD-001 task group increasingly receives requests from users for additional information and clarification of x-ray usage in other areas. This is because use of x-ray technology for analyzing solder joints has resulted in significant soldering process improvements. As with all technology introductions, however, the benefits and questions that result from the new information provided must be characterized, assessed and disseminated into practical form. One such area where x-ray technology has provided a tremendous amount of new information is plated through-hole (PTH) solder joints. The “insides” of these joints were previously “hidden” from scrutiny, unless subject to destructive methods, and the standards writers will need time to carefully revise old criteria to accommodate this new information. With this in mind, IPC formed a task group (called Team Skeleton) to discuss this and other matters, with the goal to develop additional x-ray-related guidelines and requirements for inclusion in future IPC documentation. As usual, Dave says, “All are welcome to participate and provide their comments and suggestions.”

At present, through-hole joint fill requirements and inspection criteria are commonly identified and understood within the J-STD-001/IPC-A-610 specifications. Those indicate Class II/III assemblies should have at least 75% fill, based on the through-hole depth. An oblique angle view x-ray clearly shows the nature and depth of the fill nondestructively (FIGURE 1). Additionally, many x-ray systems offer software that indicates the fill level percentage (Figure 1, right). However, as I have said before, these measurements have a degree of error. As an alternative, simple operator examination can quickly determine what is obviously acceptable and unacceptable, with any subsequent measurement used for clarification in the subset of “not sure” joints. If you are “not sure,” and the fill is around the 60 to 80% level, is it not worth flagging a process issue indicator, even if the actual value is within specification requirements?

While that situation probably covers the most likely issue to befall through-hole joints, the task group suggests further clarification be added to cover more eventualities and better define what is and is not acceptable. In particular, it should clarify the implica-

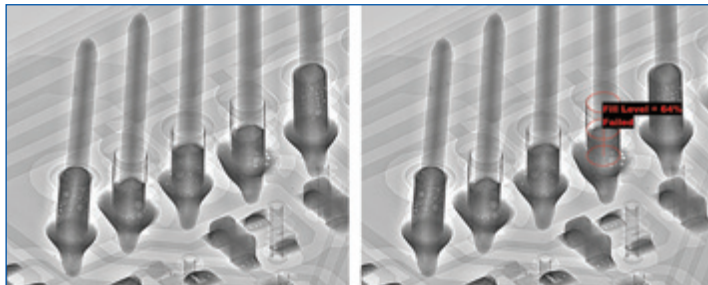


FIGURE 1. Plated through-hole joints (PTH) with varying levels of fill percentage. All joints show the presence of some voiding. The right image shows the fill calculation possible on some x-ray inspection systems.

tions if and where voiding occurs within the solder-filled portion of the joint, even if it is not 100%-filled. Further, the location of the absent fill material within the joint should be discussed, if it was not present at one end.

On the presence of voiding within the filled section of the joint (Figure 1), the task group suggests voiding inside these solder fillets is not unusual, and therefore any calculation of the level of voiding should not be subtracted from the fill percentage value.

On the location of the “missing” fill material, the task group suggests, when assessing solder fill in PTH joints (per J-STD-001, section 6.2 and Table 6-6), to define a “circumferential solder separation” to explain the missing fill (void) area and its location within the joint. This definition would be classified as an internal void in the solder fillet extending around the entire circumference of a plated through-hole and lead/wire. In other words, there is no continuous flow of solder between the solder-source side fillet and the solder-destination side fillet. Therefore, when using x-ray evaluation to assess solder fill percentage in plated through-holes, a continuous solder fill should be evident from the solder-source side toward the solder-destination side, even if it is not 100%. The proposed J-STD-001 requirements would not permit any continuous circumferential solder separation between a solder-source side fillet and a solder-destination side fillet (FIGURES 2 and 3).

Figure 2 shows one PTH (left) with 100% fill but also containing a void. This would still be considered 100% fill, and the voiding level would not be subtracted. The other PTH (right), however, has solder at the top and bottom but none in the center, thereby failing the proposed criteria, and is markedly different in shape from the joints shown in Figure 1, where the fill extends from one side but does not reach all the

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way to the other. Figure 3 shows the same joints as in Figure 2 but through a nondestructive PCT examination. A reconstructed 2-D x-ray slice shows the presence and absence of solder around the respective leads at around the middle of the joint depth. A 3-D representation of the joints is also shown.

This is the current proposal. It helps define acceptable and unacceptable PTH joints and considers whether missing fill material lies between board and device, rather than just from one end, and explicitly indicates any voiding within the filled portion should not be included in any fill percentage calculation. If adopted, these clarifications will be included in future IPC document revisions. Contact the J-STD-001 Team Skeleton Task Group if you prefer otherwise. □

Au.: Images courtesy Peter Koch, Yxlon International.

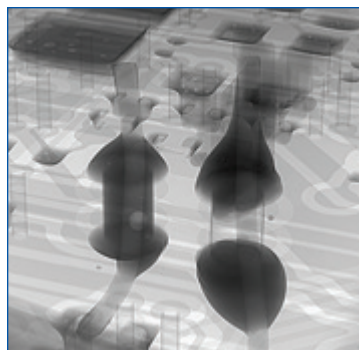


FIGURE 2. X-ray image of two PTH joints. One joint has 100% fill but also includes a void. The other includes a circumferential solder separation and would therefore fail the proposed criteria.

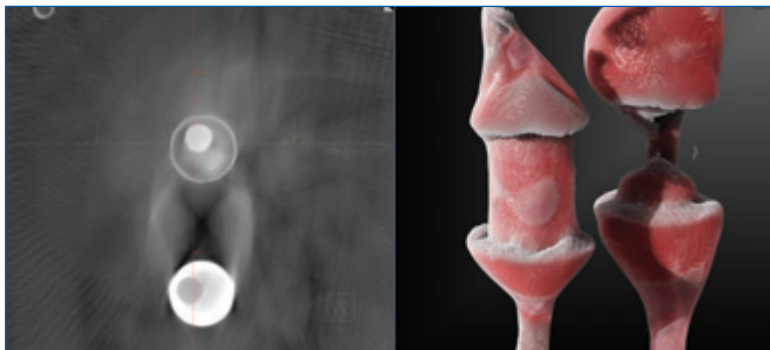


FIGURE 3. PCT reconstruction of the joints shown in Figure 2. A reconstructed 2-D x-ray slice through approximately the middle of the joint depth is shown on the left, and a 3-D representation of both joints is shown on the right.

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Thinking Lean in Test Strategy

Methods for 100% test coverage at the assembly level.

WHILE LEAN MANUFACTURING strategy is discussed in relation to test strategy, it often focuses on defect mitigation strategies such as integrating program, pack and test activities to minimize variation and transport. However, a Lean manufacturing philosophy can provide even better guidance as companies navigate test strategy options. There is one hurdle to overcome. Google the question, “Is test a value-added activity?” You will see answers in Lean manufacturing forums that range from “if the process is in control you don’t need to test” to “yes, if the customer is willing to pay for it.”

The reality is that in the electronics industry there are very real reasons robust inspection and test strategies are necessary. And, when the cost of field failures is fully considered, a robust inspection and test strategy eliminates much non-valued-added cost. One of the reasons 3-D solder paste inspection (SPI) has gained in popularity is companies have come to understand that the quality of solder paste disposition has a huge impact on whether there are workmanship-related defects later in the process. Screen for variations at that point, and a large percentage of potential defects are eliminated before components are attached to the PCB. Similarly, in-process inspection by automated optical inspection (AOI) and x-ray help screen out workmanship defects before product gets to test. In fact, the argument that a production line with tight process control and a series of inline inspections won’t generate workmanship-related defects is valid and is often used to justify little or no additional testing between the electronics contract manufacturer and the customer in outsourcing scenarios. The fallacy with that argument is it presumes that PCBAs are populated with 100% known good components. The reality is that while component quality has improved immeasurably since the days when contract manufacturers performed 100% component screening in incoming inspection, the rigors of shipment and high-temperature processing do create bad components. Legacy products have even higher risks in this area, since they often use aging component inventories.

Just as SPI helps reduce board-level rework and scrap early in the assembly process, board-level test helps eliminate higher level assembly rework prior to that assembly process. Additionally, when the cost of shipping and handling a defective PCBA is considered, the sins of overtransporting and overprocessing are put into the mix.

Consequently, the question becomes, What is the most cost-effective sequence of board-level testing?

This is the point where the conversation often turns to design constraints and the cost of fixturing. If a Lean perspective is taken, this question should focus on process throughput rather than cost of fixturing.

Assuming a PCBA can be designed with 100% coverage, in-circuit testing (ICT) will provide the best throughput. When product design engineers collaborate with test engineers to design in the needed accessibility and built-in test capability, ICT can be exploited to reduce the complexity or even the need for functional testing and/or added component accelerated lifecycle testing.

While ICT is typically seen as an electrical test, it can do a much wider range of diagnostic testing, including:

1. Memory testing.

- 0000
- FFFF
- A0A0
- 0A0A
- Walk across 0 to check shorts and opens for data and address lines
- Walk across 1 to check shorts and opens for data and address lines

2. Vector tests when boundary scan devices are incorporated.

- Read the device identification (ID)
- Exercise each vector, including testing for stuck @ 0 and stuck @ 1

The challenge is determining if the available PCBA real estate can provide the required level of accessibility. From a design for testability (DfT) perspective:

- Each single connection should be terminated either pull up or pull down, depending on the internal ICs. When terminated correctly, the circuit performs better, and there is less electrical noise during ICT.
- Even with multiple connections on the circuits, PCB layouts have very poor test accessibility if the PCB layout designer does not provide accessible vias. Unless the product incorporates RF or high-speed technology, the designer should bring all multiple connections to test vias that are accessible from the bottom side of the PCBA.
- The design challenge in providing test vias is that vias under pads can cause solder wicking, resulting in insufficient solder joints, making it imperative to have good spacing for test vias. Solder mask design must also account for accessibility of the test via. Ideally, test vias should be exposed up to 22-25 mils for test access.

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In cases where ICT test coverage is below 80%, evaluate different strategies. On a medium-sized PCBA with 650 components, 80% coverage can translate to over 100 untested components. While functional testing alone will detect some issues, it may not detect a component near failure and often isn't precise in identifying root cause. A combination of flying probe, functional testing and burn-in/accelerated life testing (ALT) may be the solution, particularly when flying probe's ability to measure component voltage is utilized.

"In cases where ICT test coverage is below 80%, evaluate different strategies."

In analog and digital components and bipolar transistors, a flying probe tester can detect the device voltage and determine if the device has issues based on the voltage it detects. Mosfet devices can also be detected this way. However, the voltage measurement is higher. With CMOS or a logic gate, the voltage of the interior transistors can be measured. Since BGAs are digital devices, their tests are different. In these cases, the capacitance value of the logic array is measured and compared to the standard. These tests can be conducted regardless of accessibility. If the layout is dense, the PCBA may be probed down to 10-15 mils for this testing. While flying probe is much slower than ICT from a throughput standpoint, it represents a faster option for detecting bad components than burn-in or ALT. A complex functional test can easily cost \$100,000 to develop, so evaluating initial pre-functional test screening options may save money. This type of testing also saves rework time and money, since flying probe will identify the component failure more precisely.

From a Lean perspective, early collaboration among design engineers at the OEM and test engineers in manufacturing will result in a lower cost, more efficient test process. ICT will offer the best cost and throughput if product volumes and test coverage justify it. When they don't, analyzing the mix of other test options for the best throughput and cost aligned with desired yields is a good strategy. All analysis should consider the cost of failures downstream in the process. □

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We will train you.

Job description: People will bring you stuff. Usually that stuff doesn't work. It just sits there passively when power is applied to it. The handover is usually not a happy occasion. (Note severely furrowed brow of customer as they hand you the malfunctioning item.) Check facial expression and nervous laughter of the person delivering the stuff. It conceals little. Much rides on the diagnosis (their job, perhaps). Failure in this instance is a career option for you. Diagnosing the source, that is. You just need to find the defective solder joint.

That inert object represents job security. Just do your job, using x-ray and CT scanning technology. Think of it as solder joint forensics in an x-ray cocktail, complete with a materials science chaser. The source of the defect might be obvious; then again, it might be elusive. That's what you're paid to do. If the art and science of detection attracts you, and you've ever wondered about doing the real thing, read on. You may have just found your future.

"Stuff," as we know it, is usually printed circuit board assemblies (PCBAs), either singular, or in larger combination with other assemblies. They are joined together, mostly by connectors or flex circuits and cables, sometimes by solder joints. Often the jumble comes encapsulated in a bigger box. The common thread is the assembly worked for a while, then it didn't. The culprit is embedded deep in that box, covered by other stuff that inhibits examination and discovery. Hence the customer's furrowed brow. Accelerated facial aging may be more pronounced and proportionate to dollars on hold (pending resolution) if the job of the subject engineer and/or their existing OEM business relationship is riding on the outcome of the stuff you are being asked to scan. Tangible, actionable results are needed quickly from the 3-D images you will produce. The customer will wait in the lobby – if not next to the x-ray system – for said images. No rush, except you need to do it now. You hold the key. No pressure here. That's our life.

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We need a special individual. For us to assume that risk, they should possess one or more of the following attributes:

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2. Technical aptitude. That is, numeracy: comfort with quantitative representations of reality. Whether expressed as linear measurements, area, volume, percentages or other values, you must understand them and be equipped to explain these same measurements to those who do not. The facts don't lie. They are necessarily inconvenient. In this role, you will deliver the facts, come what may.

3. Articulate nature. A comfortable, jargon-free facility with the local language. Since our local language is American English most days, make that written and spoken English.

4. Even keel. We work under pressure most of the time, intense pressure some of the time. Some of that pressure is fueled by unreasonable customers. Some of those same are jerks. Don't let that get to you. This too will pass. They may be jerks, but they're our jerks. They pay our bills. Do your job. Let management tell the jerks to go to hell. That's their job. Yours is to furnish the data to refute the jerks. Furnish data wisely.

5. Intellectual curiosity. A disposition to want to know why things work. Even better: an obsession with figuring out why they don't. If you are a tinkerer, you're home. This is your sandbox.

6. Willingness to learn, even if it leads to unexpected roads taken. Corollary to #5 above. When you set up a 225kV x-ray machine, and you have access to even bigger machines, word gets around.

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.



Engineers bring you unfamiliar things to inspect, observe and measure. Fossils. Citrus fruit. Rocket motor nozzles. You know, common household items with defects. Be open. Learn from it. Don't shy from admitting it's a new experience. It's no discredit for you to be honest. Your (our) customer may find it refreshing to hear that. They're used to sales speak, so you will stand apart in a good way. In doing so, you may well have discovered our next business. (Try doing that at one of the big Silicon Valley companies). Enjoy the discovery. We'll give you the credit.

7. Decisiveness. Given the facts and evidence our instruments produce, can you synthesize what it all means? Can you defend your conclusions? Can that synthesis help a desperate customer fix their problem? Can you engage with customers who have predetermined notions about why systems don't work, your contrary evidence notwithstanding?

8. Sense of humor. You will be working with a team, and that team will include your (our) customer. Everybody is different, but all are in the same rowboat for the duration of the current project. Sometimes humor defuses pressure-filled minutes and hours in that boat. Use it. Someone may remember you favorably one day.

9. Analytical and organizational proficiency. No fake news here. For that, consider politics as a career. Here we still traffic in hard evidence. Some of our decisions support equipment that preserves or saves lives. We need to be right, not biased or predestined in our outcomes. We go where the evidence – objective evidence – leads us.

10. Open mindedness. We're talking to you, aren't we? And you're reading this, at least so far. Q.E.D.

11. Trainability. See #10 above. If you are willing to invest in us, we will invest in you. Many companies shy away from this. They complain there are too few qualified candidates for the available positions. The question is are candidates born (plug-and-play) or made (we will train)? The truth is many companies are lazy or simply don't want to take the time and expense to develop their own workforce. We do. Hence this ad.

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Notice I didn't say a college degree is a prerequisite? Note this carefully. Yes, a college degree is nice to have, minus the debt, but interesting people come from all walks of life, and many don't walk the college path. Why foreclose opportunity to those who, for good reasons, make other choices besides college? Should lacking a scrap of paper exclude anyone demonstrating the right energy and aptitude? Having the "right" degree should not be a disqualifying factor either. STEM degrees are helpful, but let's face it: If you aren't scared of math, the textbook material can always be taught later. We don't want the nerd to obscure the poet. In certain situ-

ations, an English degree would be just as beneficial because you need to explain yourself – in an economy of words – to anxious customers. The same applies to defending your x-ray methodology. Written and spoken English is a time-tested and effective way to do that. Shakespeare as test engineer. Imagine that. Assuming he made it to the second interview.

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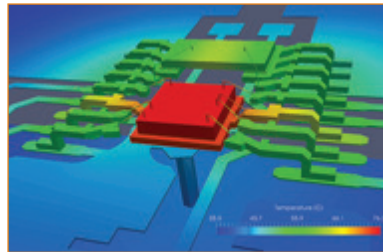


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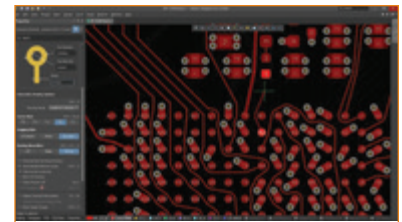


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macdermidalpha.com

MULTILAYER PRESS

X-Press maintains +/-1° control over temp. for every multilayer. Has ramp-up temp. rates up to 20°C/min. Cool-down temp. rates between 0.5° and 5°C/min. Applies up to 60 bar of pressure. Applies temp. of up to 450°C. Applies vacuum of less than 10 mbar. Can process between 1 and 50 multilayer panels at once.

Indubond

indubond.com

EMI INSULATOR

EtherNet/IP IO-Link master block insulates against inductive, conductive and capacitive noise produced by EMI. Reduces capacitive noise with thick profile that raises PCB away from backplane. Nonconductive PPS housing separates grounding plate.

Balluff

balluff.com

METALLIC OXIDE REMOVAL

VersaPrep cleans and microetches metallic substrates. Removes metallic oxides and provides micro-roughened surface to enhance dry film adhesion. Deoxidizes and microetches copper, copper alloys, stainless steel, aluminum and Inconel. Can be used in spray or immersion mode. Wet titration analysis helps maintain consistent operating performance. Operating temperatures can be adjusted depending on metal or metals to be processed.

RBP Chemical Technology

rbpchemical.com



SIR RELIABILITY TESTER

OE-200 SIR electrical test tool measures reliability per IPC J-STD-001G, amend. 1 in real-time on shop floor. Plug-and-play design tests reliability as needed and compares to historical test data. Real-time analytics and reporting. Works in conjunction with an environmental temperature-humidity chamber.

Magnalytix

magnalytix.com



EASY-CLEAN PASTE RETAINER

PLX-PR-DT paste retainer, gen. 4, incorporates new features and functions for SMT printing. Provides adjustability, up-down positions and left-right positions. Enables users to loosen and remove paste retainer for cleaning during product changeover. Features parallel leaf spring configuration, with a soft spring load in z direction that permits paste retainer to ride close to stencil or in contact with stencil without causing damage to or coining of foil.

Transition Automation

transitionautomation.com



3-D AOI

Zenith Alpha 3-D AOI collects, analyzes and manages data in real-time to dynamically formulate a multifaced view of assembly process. Provides reliable 3-D measurement. Supports KSMART factory optimization software suite, which integrates process management by linking SPI and AOI to production results. Automatically creates inspection programs 70% faster than before.

Koh Young

kohyoung.com

OTHERS OF NOTE

FLUID DISPENSER

Forte series handles applications such as flex circuit and PCB assembly, electromechanical assembly, MEMS, under-fill, precise coating, and encapsulation. Stable chassis and new electrical and mechanical architectures. Delivers units per hour gain of 20-50% higher productivity. Dual-valve-ready.

Nordson Asymtek

nordsonasymtek.com

BALL-BUMPING FLUX

NC 256 enables wetting of solders for wafer-ball bumping and other ball bumping, such as CSP, BGA, flip chip and PoP. Reportedly no contamination during reflow on solder ball or neighboring components. Can be screen- or stencil-printed or dispensed on lands or dipped on solder ball of components. Underfill-compatible. For mass reflow or rework.

Yincae Advanced Materials

yincae.com

TABLETOP PLACEMENT SYSTEM

Fineplacer Lambda 2 placement and assembly system places and connects components with accuracy of better than 0.5µm. Reportedly ideal for optoelectronics. In conjunction with optical systems with optical resolutions down to 0.7µm, it enables superimposed images of high optical quality for reliable detection and alignment of finest structures in micron range. Table is manual and partially motorized.

Finetech

Finetech.de

DUAL-LANE PRINTER

DEK TQ stencil/screen printer has high-speed dual-lane capability. Has linear drives, off-belt printing, and innovative transport and clamping systems. Features optional auto-coplanarity. Reportedly can operate up to 10 hr. without an assist.

ASM Assembly Systems

asm-smt.com

2-PART BONDING EPOXY

Supreme 112 is a two-part epoxy for bonding, sealing, potting, and impregnation applications. Is heat-curable with a viscosity of 50-200cps and an open time of 2-3 days at room temp. for a 100gm batch. Features a Tg of 190°-195°C. Serviceable up to 288°C (550°F). Retains electrical insulation properties at elevated temp.

Master Bond

masterbond.com

ROBOTS WITH VISION

iVY2 Scara, cartesian, orbital, single-, and multi-axis robots connect directly to RCX340 robot controller. Simplify setup, accelerate performance and now have vision. Support up to 5Mp cameras for high-resolution imaging for fast and stable workpiece detection. Wizard-assisted auto-calibration and easy three-step workpiece registration eliminate laborious setup tasks.

Yamaha

global.yamaha-motor.com



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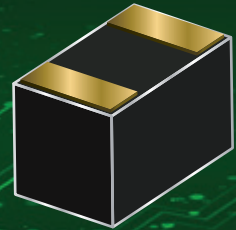
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In Case You Missed It

Chiplets

“Goodbye, Motherboard. Hello, Silicon-Interconnect Fabric”

Authors: Puneet Gupta, Ph.D. and Subramanian S. Iyer, Ph.D.

Abstract: The need to make some hardware systems smaller and others bigger has been driving innovations in electronics for a long time. The former can be seen in the progression from laptops to smartphones to smart watches to hearables and other “invisible” electronics. The latter defines today’s commercial data centers – megawatt-devouring monsters that fill purpose-built warehouses around the world. Interestingly, the same technology is limiting progress in both arenas, though for different reasons. The culprit is the printed circuit board. And the solution is to get rid of it. The authors’ research shows PCBs could be replaced with silicon. Such a move would lead to smaller, lighter-weight systems for wearables and other size-constrained gadgets, and to incredibly powerful high-performance computers. This all-silicon technology, called silicon-interconnect fabric, allows bare chips to be connected directly to wiring on a separate piece of silicon. Unlike connections on a printed circuit board, the wiring between chips on the fabric is just as small as wiring within a chip. Many more chip-to-chip connections are thus possible, and those connections are able to transmit data faster while using less energy. (*IEEE Spectrum*, Sept. 24, 2019, spectrum.ieee.org/computing/hardware/goodbye-motherboard-hello-siliconinterconnect-fabric)

Printed Electronics

“Three-Dimensional Curvy Electronics Created Using Conformal Additive Stamp Printing”

Authors: Kyoseung Sim, Ph.D., *et al.*

Abstract: Electronic devices are typically manufactured in planar layouts, but many emerging applications, from optoelectronics to wearables, require three-dimensional curvy structures. However, the fabrication of such structures has proved challenging, due to the lack of an effective manufacturing technology. The authors show conformal additive stamp (CAS) printing technology can be used to reliably manufacture 3-D curvy electronics. CAS printing employs a pneumatically inflated elastomeric balloon as a conformal stamping medium to pick up pre-fabricated electronic devices and print them on curvy surfaces. To illustrate the capabilities of the approach, it is used to create various devices with curvy shapes: silicon pellets, photodetector arrays, electrically small antennas, hemispherical solar cells and smart contact lenses. It is also shown that CAS printing can be used to print onto arbitrary 3-D surfaces. (*Nature*, nature.com/articles/s41928-019-0304-4)

PTH Reliability

“Failure Analysis on Cracking of Blind and Buried Vias of Printed Circuit Board for High-End Mobile Phones”

Authors: Jie Tang, Yi Gong and Zhen-Guo Yang

Abstract: Cracking of blind and buried vias of printed circuit boards for smartphones was encountered, leading to defects such as display problems like scrambled display or no display during service. To find the root causes of the failure, comprehensive failure analysis was performed on the PCBAs and PCBs of the failed smartphones. Tests performed included macrograph and micrograph observation, chemical composition analysis, thermal performance testing and blind via pull-off experiment. Blind via cracking was found to be the main reason for the scrambled display or no display conditions, and an incomplete cleaning process before copper plating was the root cause of the blind vias cracking. (*Soldering & Surface Mount Technology*, vol. 31 no. 4, Sept. 2, 2019)

Board Buying, continued from pg. 18

PCBs seem to be regarded today as a cookie-cutter commodity, despite being a highly customized product. Board buyers and program managers have sent the message that price is all that matters, with the level of service and quality provided by a PCB vendor a secondary consideration. They’ve had to fend for themselves when it comes to acquiring the specialized knowledge that would make them even better at buying PCBs and managing their vendor base.

Why would EMS companies or OEMs, especially those with ISO registration, not provide corporate training in buying the commodity that is the foundation of their assembly processes and one of their largest expenses? Good, open communication between buyers and vendors, along with some much-needed training, will boost PCB quality and delivery performance, and lower costs. □

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.



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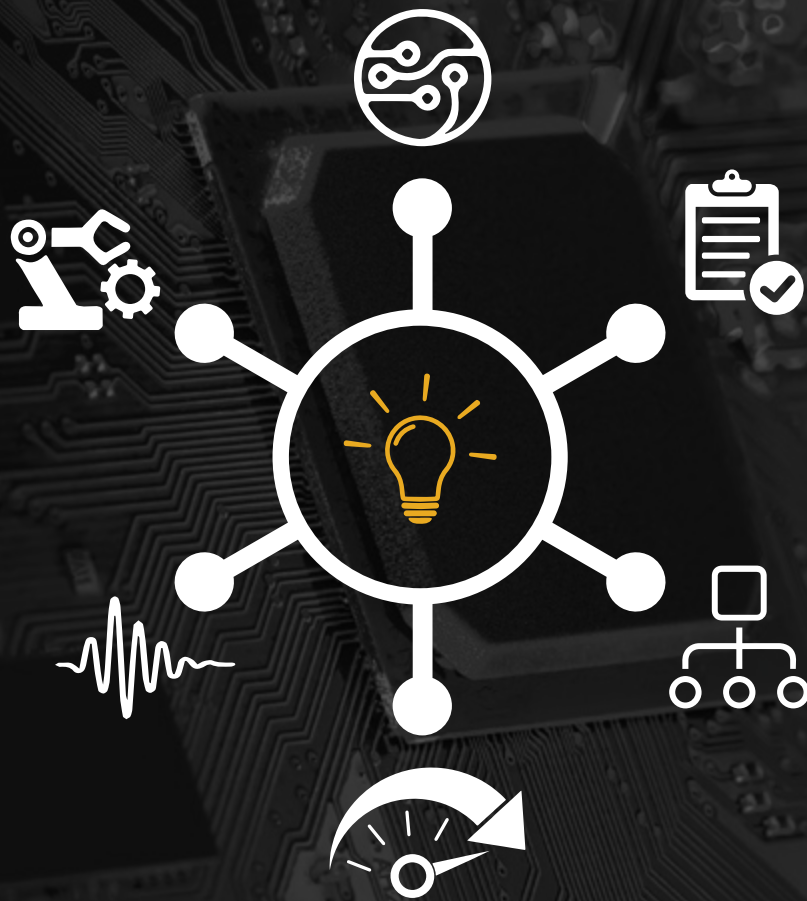
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