

# **Ultra High Efficiency Dual DC-DC Controller**

#### **FEATURES**

- Dual DC-DC SMPS controller with integrated drivers
- Two constant ripple-current controllers
- Constant ripple-current control allows optimum inductor size
- High full load efficiency; up to 94%
- High light load efficiency; >85% at 100mA
- Vout accuracy: 1% or better
- Input voltage; from 3V to 26V
- Output voltage adj. from 0.5V to 2.75V
- Output current up to 15A
- Independent
  - Power Good signals
  - ON/SKIP signals
- Soft-Start at start-up
- Soft-stop at shutdown
- Voltage Feed-Forward Compensation
- User adjustable operating frequency
- Dynamic voltage change support
- Output Protection:
  - Latched Over Voltage Protection
  - Latched Under Voltage Protection
  - Valley type Over Current Protection
- Input Protection:
  - Under Voltage Lock Out on VDDA
  - Under Voltage Lock Out on VIN

#### **APPLICATIONS**

Power Supplies for Notebook CPU and Peripherals

#### ORDERING INFORMATION

Part Number	Temp Range	Package	
OZ813LN	0°C to 85°C	QFN24 Lead-Free	

#### **GENERAL DESCRIPTION**

OZ813 is a DC/DC controller specially developed to design power supplies for next generation microprocessors, their peripherals and chipsets. OZ813 steps down the high battery voltage to low output voltages in the range of 0.5V to 2.75V. High efficiency, DC accuracy and excellent transient response make OZ813 suitable for supplying low voltage CPU peripherals, chipset cores, and graphics processors. OZ813 has two independent constant ripple-current buck controllers with powerful integrated drivers able to drive output currents up to 15A.

Voltage Feed-Forward compensation assures high rejection of input voltage transients typically occurring when the AC adapter is plugged in or removed.

Over Voltage Protection (OVP) acts when the output voltage exceeds the set voltage by more than 125mV. This protection condition is latched and initiates a ramp down of the output voltage.

Under Voltage Protection (UVP) acts when the output voltage falls below the set voltage by more than 133mV. This protection condition is latched and initiates a ramp down of the output voltage.

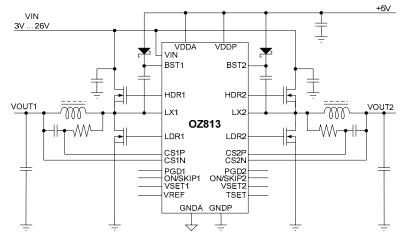
After an OVP or UVP event, the ON/SKIP pin should be toggled or VDDA/VIN cycled to restart the circuit.

Both outputs are protected against overload by individual, valley current type, cycle-by-cycle (Over Current Protection) OCP circuits.

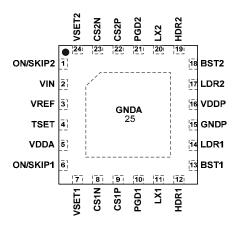
The Under Voltage Lock Out circuit monitors both, VDDA and VIN and lets the controller operate only if VDDA > 4.3V and VIN > 2.5V.

The Power Good signal is high as long as the output voltage is within +125mV/-133mV of the set voltage. At startup the output voltage ramps up in a controlled manner with a typical slew rate of 1V/ms and at shutdown the output voltage is ramped down in a controlled manner with the same slew rate.

# SIMPLIFIED APPLICATION DIAGRAM



## PIN DIAGRAM



# **PIN DESCRIPTION**

No.	Name	I/O	Туре	Description
			- 1	Enables Channel 2 operation.  If V <sub>ON/SKIP2</sub> > 0.6V, the Vout2 voltage ramps up to the voltage set on
1	ON/SKIP2	I	Digital	VSET2 pin with a slew rate of 1V/ms. If $V_{ON/SKIP2} > 2.1V$ the controller enters skip mode of operation. If both ON/SKIP1 and ON/SKIP2 pins are < 0.4V the chip is disabled and enters a very low consumption mode < 1 $\mu$ A. To re-enable the controller the voltage on at least one of the ON/SKIP pins need to exceed 1V. Once the chip is enabled the conditions
				above applies.
2	VIN	I	Analog	Input voltage sense. Used for feed-forward compensation. Also monitored by the Under Voltage Lock Out circuit. Let the controller operate only if Vin > 2.5V. Must be connected to the input voltage of the power stage.
3	VREF	0	Analog	2.75V +/- 1% precision reference voltage. A 0.1µF should be placed from VREF to GNDA.
4	TSET	Р	Power	Adjust the Ton of the controller according to the formula:  Ton = (1.6µs*V <sub>TSET</sub> )/(Vin-Vout)  A 0.1µF capacitor must be placed from TSET to GNDA.
5	VDDA	Р	Power	+5V supply for the controller analog circuits. A 1μF capacitor should be placed from VDDA to GNDA.
6	ON/SKIP1	I	Digital	Enables Channel 1 operation. If $V_{\text{ON/SKIP1}} > 0.6\text{V}$ , the Vout1 voltage ramps up to the voltage set on VSET1 pin with a slew rate of 1V/ms. If $V_{\text{ON/SKIP1}} > 2.1\text{V}$ the controller enters skip mode of operation. If both ON/SKIP1 and ON/SKIP2 pins are < 0.4V the chip is disabled and enters a very low consumption mode < 1 $\mu$ A. To re-enable the controller the voltage on at least one of the ON/SKIP pins need to exceed 1V. Once the chip is enabled the conditions above applies.
7	VSET1	I	Analog	Sets the Vout1 output voltage of the first controller. Uses a resistor divider from the reference voltage.
8	CS1N	I	Analog	Inverting current sense pin for channel 1.
9	CS1P	I	Analog	Non-inverting current sense pin for channel 1.
10	PGD1	0	Digital	Power Good output for Vout1.  It is an open drain output asserted high when the output voltage Vout1 is within +125mV/-133mV of the set value.
11	LX1	Р	Power	Inductor switching node for channel 1.
12	HDR1	0	Digital	Output of the high side driver for channel 1.
13	BST1	Р	Power	Positive supply for the high side driver of channel 1. A 0.1µF capacitor should be placed between BST1 and LX1.
14	LDR1	0	Digital	Output of the low side driver for channel 1.
15	GNDP	Р	Power	Power Ground.
16	VDDP	Р	Power	Positive supply for the low side driver. A 1µF capacitor should be placed from VDDP to GNDP.
17	LDR2	0	Digital	Output of the low side driver for channel 2.
18	BST2	Р	Power	Positive supply for the high side driver of channel 2. A 0.1µF capacitor should be placed between BST2 and LX2.
19	HDR2	0	Digital	Output of the high side driver for channel 2.
20	LX2	Р	Power	Inductor switching node for channel 2.
21	PGD2	0	Digital	Power Good output for Channel2.  It is an open drain output asserted high when output voltage Vout2 is within +125mV/-133mV of the set value.
22	CS2P	Ī	Analog	Non-inverting current sense pin for channel 2.
23	CS2N	I	Analog	Inverting current sense pin for channel 2.
24	VSET2	I	Analog	Sets the Vout2 output voltage of the second controller. Uses a resistor divider from the reference voltage.
25	GNDA	Р	Power	Ground for the controller analog circuits.

OZ813-SF-v1.3 Page 2

## **TYPICAL APPLICATION SCHEMATIC**

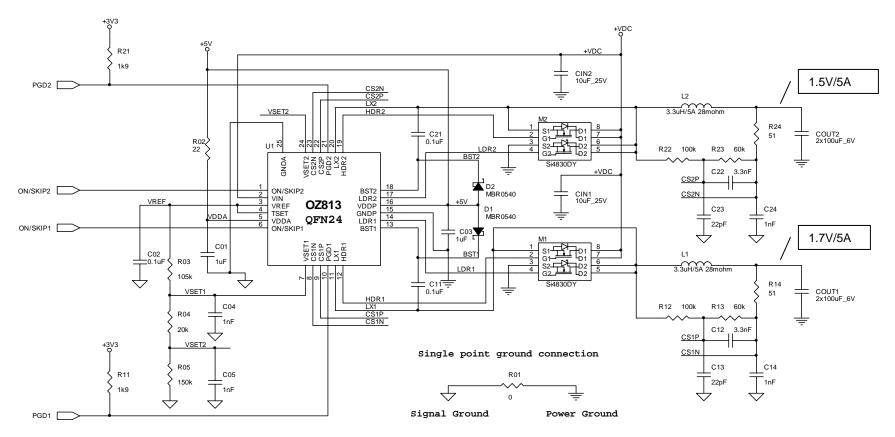


Figure 16. Typical Chipset Power Supply Schematic

OZ813-SF-v1.3 Page 3

# **BILL OF MATERIALS**

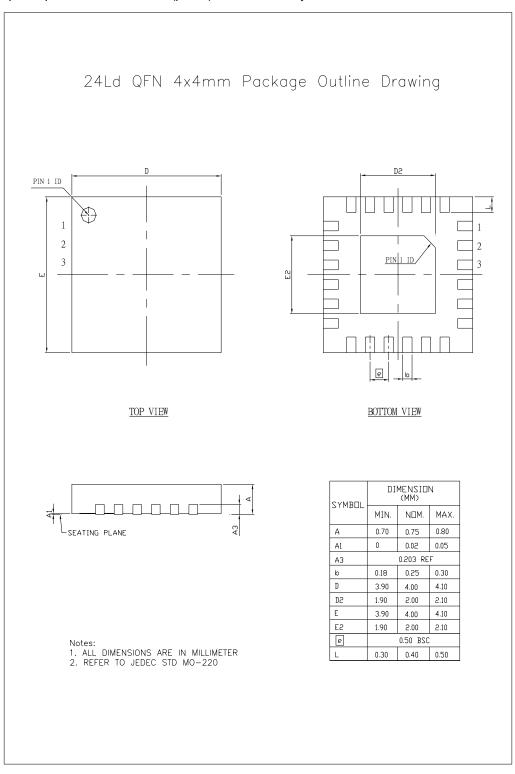
Item	Qty	Reference	Value	Vendor	Part Number	PCB Footprint	
	1 2	CIN1, CIN2		Taiyo-Yuden	TMK325BJ106MM-B	1210	
1			10u/25V	Johanson Dielectrics	250S41X106M		
				TDK	C3225X7R1E106M		
		COUT1, COUT2	2x100uF/6V	Taiyo-Yuden	JMK325BJ107MY-T	1210	
2	2			Johanson Dielectrics	6R3S41X107M		
				TDK	C3225X5R0J107M		
3	3	C02, C11, C21	0.1uF/10V	Any	Ceramic – X7R or X5R	0603	
		C01, C03	1uF/10V	Taiyo-Yuden	EMK107BJ105KA-B		
4	2			Johanson Dielectrics	100R14X105M	0603	
				TDK	C1608X5R1A105K		
5	2	C12, C22	3.3nF/25V	Any	Ceramic – X7R or X5R	0603	
6	4	C04, C05, C14, C24	1nF/6V	Any	Ceramic – X7R or X5R	0603	
7	2	C13, C23	22pF	Any	Ceramic	0603	
8	1	R01	0	Any		0603	
9	1	R02	22	Any		0603	
10	1	R03	105k 1%	Any		0603	
11	1	R04	20k 1%	Any		0603	
12	1	R05	150k 1%	Any		0603	
13	2	R11, R21	1k9	Any		0603	
14	2	R12, R22	100k 1%	Any		0603	
15	2	R13, R23	60k 1%	Any		0603	
16	2	R14, R24	51	Any		0603	
17	2	D1, D2	NONE	Vishay	MBR0540	SOD-123	
18	2	M1, M2	NONE	Vishay	Si4830DY	SO-8	
10		IVI I , IVIZ	INOINE	Fairchild	FDS6982S		
19	2	14.10	3.3u/5A	Vishay	IHLP2525CZ-01	2525	
19	2	L1, L2	3.3u/3A	TOKO	FDV0630 3R3		
20	1	U1	OZ813	O <sub>2</sub> Micro, Inc.	OZ813	QFN24	

# **COMPONENT SUPPLIERS**

Manufacturer	Contact Information			
Manufacturer	Phone	Website		
Power MOSFETs		·		
Vishay	1-402-563-6866	www.vishay.com		
Fairchild	1-703-478-5800	www.fairchildsemi.com		
Inductors		•		
Vishay	1-402-563-6866	www.vishay.com		
TOKO	1-408-432-8281	www.toko.com		
Diode				
Vishay	Vishay 1-402-563-6866			
Fairchild	1-703-478-5800	www.fairchildsemi.com		
Capacitors				
Taiyo-Yuden		www.t-yuden.com		
Johanson Dielectrics	1-818-364-9800	www.johansondielectrics.com		
TDK	1-800-344-2112	www.tdk.com		
Resistors		·		
Vishay	Vishay 1-402-563-6866			
TDK	1-800-344-2112	www.tdk.com		

## **PACKAGE INFORMATION**

Exposed pad at bottom is GNDA (pin 25) and must be fully soldered to PCB



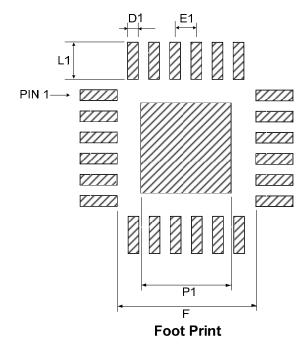
Rth j-a (QFN-24 4x4mm package) = 38°C/W Rth j-c (QFN-24 4x4mm package) = 4.8°C/W

## **DIMENSION TABLE**

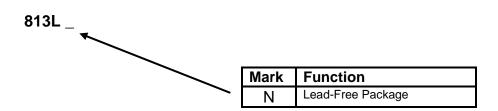
SYMBOL	SPECIFICATION		
Pitch 0.50	Min	Nom	Max
Α			0.90
В		4.00	
С		4.00	
D	0.18	.25	.30
E		.50	
L	0.30	0.40	0.50
Р			2.80
D1		0.25	
E1		0.50	
L1		0.80	
P1		2.50	
F		3.20	

- Controlling dimensions are in millimeters (mm).
   Pin #1 count orientation shall be in a counterclockwise direction as viewed in live-bug position.

## **LANDING PATTERN**



# PACKAGE MARKING (QFN24 PACKAGE)



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