




Gowin Software

User Guide

SUG100-2.6E, 11/02/2021

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Revision History

Date	Version	Description
11/08/2019	2.0E	<ul style="list-style-type: none"> ● Synplify Pro configuration options added. ● Synplify Pro attributes and values updated.
11/28/2019	2.1E	<ul style="list-style-type: none"> ● General option added in Place & Route: Promote Physical Constraint Warning to Error, Report Auto-Placed IO Information, Place Option, Route Option. ● Resource information display added in Hierarchy view. ● Three "Find" options supported in netlist file in Process view. ● Function of adding and removing comments supported in IDE built-in editor.
03/09/2020	2.2E	<ul style="list-style-type: none"> ● VHDL is supported in Hierarchy view. ● GowinSynthesis[®] supports the synthesis of VHDL and the mixed of Verilog and VHDL. ● Prompt pops up when the unsaved project is performed synthesis or PnR. ● The introduction to Tcl command usage added in Output view. ● The descriptions of Synthesize and PnR configuration options added. ● The introduction to the editor of User Flash initialization file added.
05/13/2020	2.3E	<ul style="list-style-type: none"> ● Unused Pin configuration added. ● Encryption function added in Hierarchy view.
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06/17/2021	2.5E	<ul style="list-style-type: none"> ● Screenshots and their descriptions updated. ● Synplify Pro removed.
11/02/2021	2.6E	<ul style="list-style-type: none"> ● SSPI and MSPI dual-purpose pins updated. ● The descriptions of -ireg_in_iob/-oreg_in_iob/-ioreg_in_iob updated. ● MODE dual-purpose configuration removed. ● Place & Route BitStream: Power On Reset added. ● The description of simulation files added.

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1 About This Guide

1.1 Purpose

This manual describes Gowin Software installation and operation, and it aims to help you be familiar with the use flow and improve design efficiency. The software screenshots in this manual are based on V1.9.8.01. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. [SUG940](#), Gowin Design Timing Constraints Guide
2. [SUG935](#), Gowin Design Physical Constraints Guide
3. [SUG114](#), Gowin Analyzer Oscilloscope User Guide
4. [SUG282](#), Gowin Power Analyzer User Guide
5. [SUG502](#), Gowin Programmer User Guide.
6. [UG285](#), Gowin BSRAM & SSRAM User Guide
7. [SUG283](#), Gowin Primitives User Guide.
8. [UG286](#), Gowin Clock User Guide
9. [UG287](#), Gowin Digital Signal Processing (DSP) User Guide
10. [UG289](#), Gowin Programmable IO (GPIO) User Guide
11. [UG295](#), Gowin User Flash User Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CRC	Cyclic Redundancy Check
FPGA	Field Programmable Gate Array
GowinSynthesis	GowinSynthesis
IP Core	Intellectual Property Core
PnR	Place & Route
GAO	Gowin Analyzer Oscilloscope
GPA	Gowin Power Analyzer
FloorPlanner	Physical Constraints Editor
Timing Constraints Editor	Timing Constraints Editor
Schematic Viewer	HDL Schematic Viewer

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction

Gowin design system is an integrated circuit design and implementation tool specifically for Gowin GOWINSEMI FPGA chips, and it has superior performance and easy to use. Gowin design system provides a comprehensive and optimized design for Gowin FPGA chips with the low-power and low-cost architecture, and it integrates the flow from RTL description to FPGA bitstream file generation, including design optimization, automatic design, and graphical interaction, etc.

Functions

- The software system supports all functions of Gowin FPGA chips, covering the complete design flow from the functional description of the RTL circuit to the generation of FPGA bitstream file.
- GowinSynthesis[®] supports high-performance logic design and synthesis.
- Supports automatic design and interactive graphical design in parallel.
- Supports Centos6.8/7.0/7.5 (64bits), Ubuntu18.04/20.04LTS, Win7/8/10(32bits/64bits), Win XP (32bits) systems.
- Hundreds of millions gate-level software.
- Supports VHDL, Verilog HDL and System Verilog languages.
- Supports optimized architecture of Gowin products.
- Supports original and high-performance algorithm PnR.
- Precise timing analysis and timing report.
- Clock analysis and control to ensure better timing performance.
- Supports various timing and physical constraints.
- Supports real-time monitoring of hardware circuit signals and storing them, along with timing waveform diagrams display.
- Resource sharing can improve chip utilization and reduce cost.

Features

- Integrated design
 - The design can be completed in stages or automatically as a package.
 - Supports command line mode or GUI mode.
 - You can use scripted design, and design any single module flexibly without affecting the integrated design throughout.
- Can optimize design
 - Netlist optimization
 - Quick timing optimization analysis and design
 - Resource analysis and optimization
- Hierarchy design and analysis
 - Supports hierarchical netlist input and output
 - Supports flattened netlist input and output
 - Can hierarchically display, trace, and analyze netlist
- Flexible interactive graphic design
 - Simple and clear user interface
 - Displays projects, modules, tools and output.
 - Design constraint input, selection and update.
 - Quick timing analysis and report
 - Push button design

2.2 Supported Devices

Gowin software supports the LittleBee[®] family and Arora family chips. For the details of chip types, resources and packages, etc., you can visit Gowin official website.

- LittleBee[®] family: www.gowinsemi.com/en
- Arora family: www.gowinsemi.com/en

Note!

The supported devices may vary according to the software version in use. Please refer to the software you use for more detailed device information.

2.3 Install and Start

The installation method in Windows system is the same; double-click the Gowin software installation package and install according to the prompt. After installation, the shortcut will be created on the PC desktop by default. The installation method in the Linux system is to decompress the installation file.

You need to configure the license when you start Gowin Software for

the first time after installation. The software license is a format contract between the users and GOWINSEMI to define and limit the rights of users and the obligations of GOWINSEMI.

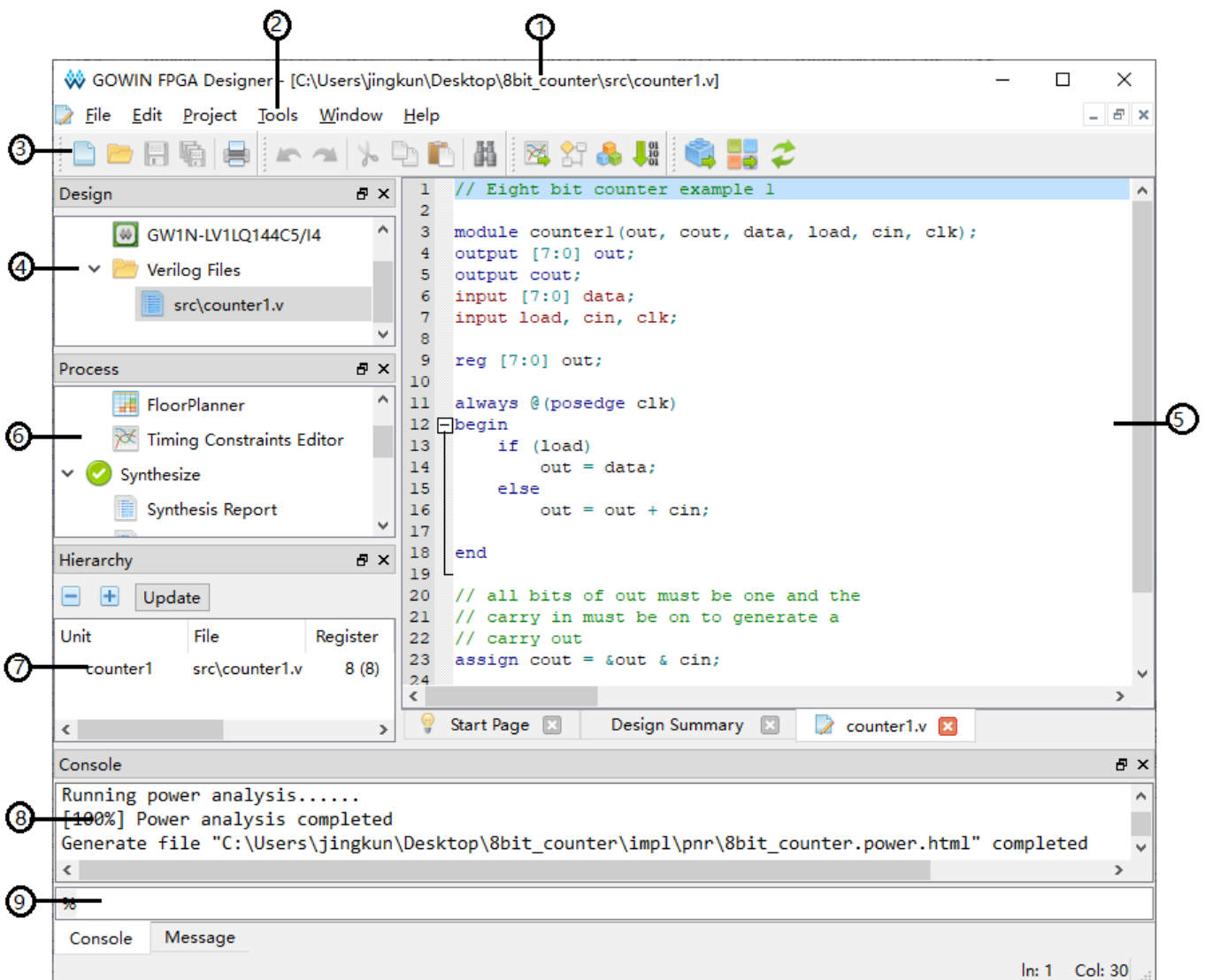
Note!

For the details, see [SUG501](#), Gowin Software Quick Installation Guide.

3 Gowin Software GUI

Gowin software GUI is as shown in Figure 3-1. It consists of the title bar, menu bar, tool bar, project area (Design), process area (Process), source file editing area, design hierarchy (Hierarchy), information output area and TCL command editing area.

Figure 3-1 GUI



- | | |
|----------------------------|---------------------------|
| ① Title Bar | ② Menu Bar |
| ③ Tool Bar | ④ Project Area |
| ⑤ Source File Editing Area | ⑥ Process Area |
| ⑦ Hierarchy Area | ⑧ Information Output area |
| ⑨ Tcl Command Editing Area | |

3.1 Title Bar

Title bar shows the current project path, name, and the files opened.

3.2 Menu Bar

The menu bar contains links to the tools and functionality that are commonly used in projects, including the File, Edit, Project, Tools, Window, and Help options. See the following for details.

3.2.1 File Bar

- New (Ctrl+N): Newly create
- Open (Ctrl+O): Open
- Save (Ctrl+S): Save
- Save As...: Save as
- Save All (Ctrl+Shift+S): Save all documents
- Close: Close
- Close All: Close all documents
- Close Project: Close current project
- Print Preview...: Print preview
- Print... (Ctrl+P): Print
- Recent Files: Show the files opened. You can click on the names of these files to re-open.
- Recent Projects: Show the projects opened. You can click on the names of these projects to re-open.
- Exit: Exit and close Gowin software

3.2.2 Edit Bar

- Undo (Ctrl+Z): Undo your last operation
- Redo (Ctrl+Y): Redo your last operation
- Cut (Ctrl+X): Cut
- Copy (Ctrl+C): Copy
- Paste (Ctrl+V): Paste
- Select All (Ctrl+A): Select all
- Find & Replace (Ctrl+F): Find or replace key words

- Toggle Comment Selection (Ctrl+/,): Add comments to the selected
- Macros
 - Start Record: Click Start Record, and the editing operations performed on editable files in the IDE will be recorded.
 - Stop Recording: Stop recording
 - Play Macro (Alt+R): Click Play Macro, and it will perform the recorded operations on the editable files.

3.2.3 Project Bar

- Archive Project: Archive project
- Restore Archived Project: Restore archived project
- Set Incremental: Set incremental
- Set Device: Set the device information of current project
- Configuration: Open configuration window
- Design Summary: Show details of current project

3.2.4 Tools Bar

- Start Page: Include Recent Projects, Quick Start, Tools, and User Manuals.
 - Recent Projects: Show the recently opened projects, and up to 10 projects will be kept.
 - Quick Start: Include New Project, Open Project, and Open Example Project.
 - Tools: Include Floorplanner, Timing Constraints Editor, and Programmer.
 - User Manuals: Manual for LittleBee and Manual for Arora
- Gowin Analyzer Oscilloscope: Gowin Analyzer Oscilloscope
- Schematic Viewer: HDL Design Schematic Viewer
- IP Core Generator: IP Core Generator
- Programmer: Pprogrammer
- FloorPlanner: Physical constraints editor
- Timing Constraints Editor: Timing Constraints Editor
- Options: Include Environment, Text Editor, and External Editor.
 - Environment: Set the IDE parameters, including Language, Toolbar Icon Size and the default path of new project. After setting the language, you need to restart the IDE, then the settings will take effect.

- Text Editor: Set the text editor attributes, including font, font size, color, line numbers display, blank characters visualization, the current line and matching parentheses highlight.
- External Editor: Set the third-party text editor, and you can choose whether to always use the third-party editor to open the design file.

3.2.5 Window Bar








- Full Screen (F11): Full screen
- Tile: Tile display
- Cascade: Cascade display
- Reset Layout: Restore initial settings
- Panels: Select whether to display the five panels:
Design, Hierarchy, Process, Message, and Console
- Start Page: Display start page in source file editing
- Design Summary: Display design page in source file editing area, including General and Target Device.
 - General: Project information, including project path and the synthesis tool used.
 - Target Device: Engineering device information, including package, speed grade, and core voltage.












3.2.6 Help Bar

- View Help: View help documents
- Contact Us: Click to contact us
- Manage License: Manage license, and you can refer to [SUG501](#), Gowin Software Quick Installation Guide.
- About: Show software version and copyright information

3.3 Tool Bar

It provides quick access to some commonly used functions, and from left to right are:

-  (Ctrl+N): Create a new file or project
-  (Ctrl+O) : Open a file or project
-  (Ctrl+S) : Save
-  (Ctrl+Shift+S): Save all
-  (Ctrl+P): Print
-  (Ctrl+Z): Undo your last operation
-  (Ctrl+Y): Redo your last operation

-  (Ctrl+X): Cut
-  (Ctrl+C): Copy
-  (Ctrl+V): Paste
-  (Ctrl+F) : Find
- : Start Gowin Analyzer Oscilloscope
- : Start Schematic Viewer
- : Start IP core Generator
- : Start Programmer
- : Run Synthesis
- : Run Place & Route
- : Run Synthesis and Place & Route

3.4 Project Area (Design)

The project area shows projects and the related files. You can check or change the project device information, user design files, user constraints files, configuration files, etc.

3.5 Process Area (Process)

The process provides FPGA design flow, including synthesis, place & route, and the download of bitstream files. You can also double-click timing constraints editor and physical constraints editor to edit the constraints files.

3.6 Hierarchy Area (Hierarchy)

After loading the design files, software will parse the design files first. The hierarchy window shows the hierarchy of current project. In Hierarchy view, you can locate the definition and instance of a module in a design file. You can also set a module to top module. The Unit column shows module hierarchy of the design files, and the Files column shows the file where the module definition is. Hierarchy has supported Verilog, VHDL and System Verilog.

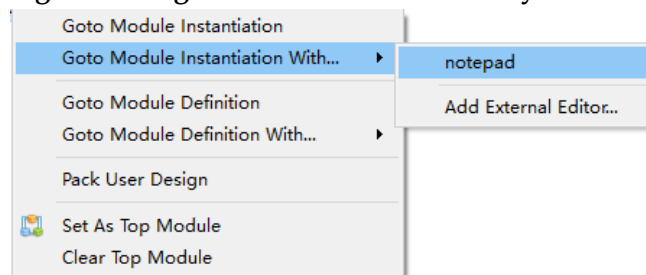
3.6.1 Right-click Menu

Functions supported in the right-click menu in the Hierarchy view are as follows:

- Goto Module Instantiation: Goes to the module instance in the source file and open it with the editor built in Gowin software. If you configure a third-party editor in "Tools > Options > External Editor" and "Always Use External Editor" is checked, you can open the source with a third-party editor by default via Goto Module Instantiation.

- Goto Module Instantiation With...: Goes to the module instance in the source file. As shown in Figure 3-2, you can choose the "notepad" or "Add External Editor". If you select "Add External Editor", "External Editor" dialog box pops up.
- Goto Module Definition: Goes to the module in the source file and open it with the editor built in Gowin software. If you configure a third-party editor in "Tools > Options > External Editor" and "Always Use External Editor" is checked, you can open the source with a third-party editor by default via Goto Module Instantiation.
- Goto Module Definition With...: Goes to the module in the source file. As shown in Figure 3-2, you can choose the set editor or "Add External Editor". If you select "Add External Editor", "External Editor" dialog box pops up.
- Pack User Design: Packs the module and its sub-module.
- Set As Top Module: Sets the module as top module; the module set as the top will be marked "🏠" to indicate that the current module is the top module, and the original hierarchy remains.
- Clear Top Module: Clears the top module setting.

Figure 3-2 Right-click Menu of Hierarchy

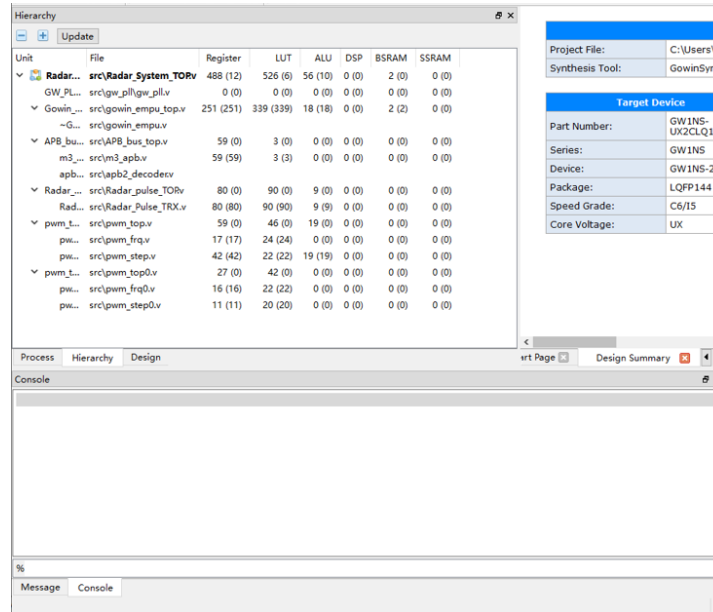


If there is an error in hierarchy parse of the project files, the prompt "RTL Analysis Error" marked in red will pop up at the top right of the hierarchy view.

3.6.2 Resources Display

The Hierarchy view will automatically display the resources of the current project after synthesis, as shown in Figure 3-3. If a module is defined as a pack module in the design, its resource is not displayed, and its resource will be counted in its upper module. The resources used by each module will be displayed with two data. As shown in Figure 3-3, the number of module Radar_System_TOP registers is 488 (12), where 12 is the number of registers used by the module itself and 488 is the total number of registers used by the module and its sub-modules.

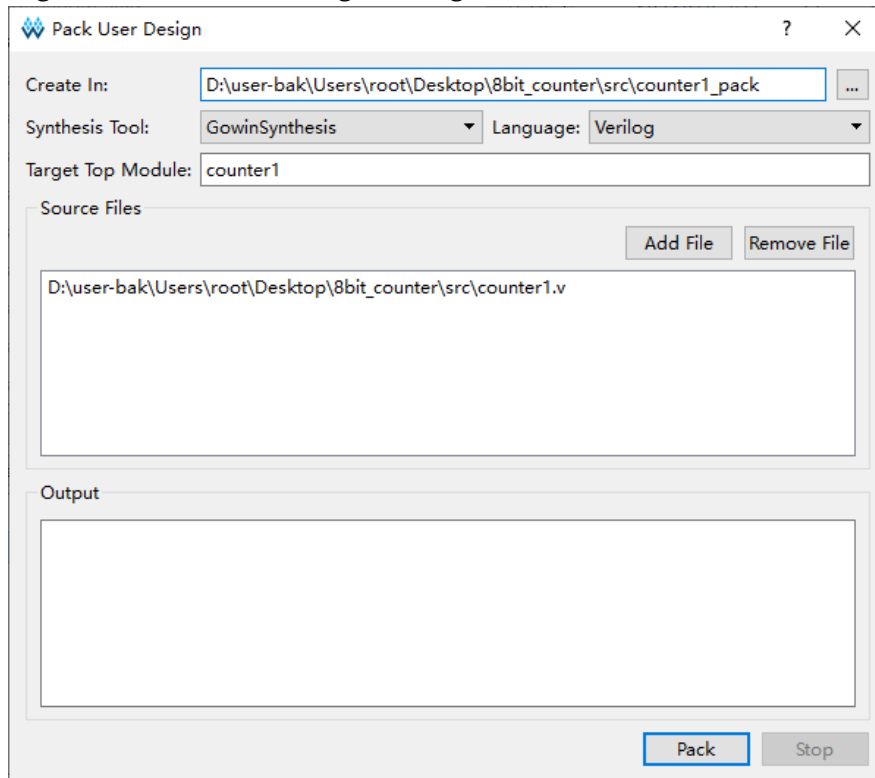
Figure 3-3 Resources Display in Hierarchy View



3.6.3 Pack File

When you open a project, if you need to pack all/some source files, you can right-click the module to be packed in the Hierarchy view, and choose "Pack User Design" to generate a post-synthesis pack file. "Pack User Design" dialog box as shown in Figure 3-4.

Figure 3-4 Pack User Design Dialog Box



The Pack User Design configurations are as follows:

- Create In: The path of the generated pack files. The default path is \src\- Synthesis Tool: Specifies a synthesis tool.
- Language: Verilog and VHDL, and the default is Verilog.
- Target Top Module: Top module to be packed. The default is the module selected in the Hierarchy view. You can change it.
- Source Files: Lists the source files of module and sub module selected in the Hierarchy view.
- Add File: Adds a file
- Remove File: Remove a file
- Output window: Output information
- Pack: Run Pack
- Stop: Stop Pack

Information will be printed in the Output view, as shown in Figure 3-5. When pack starts, if there is an error, the error will be reported in the Output view, and the information of pack failure will be printed, as shown in Figure 3-6.

Figure 3-5 Output Information in Pack User Design View

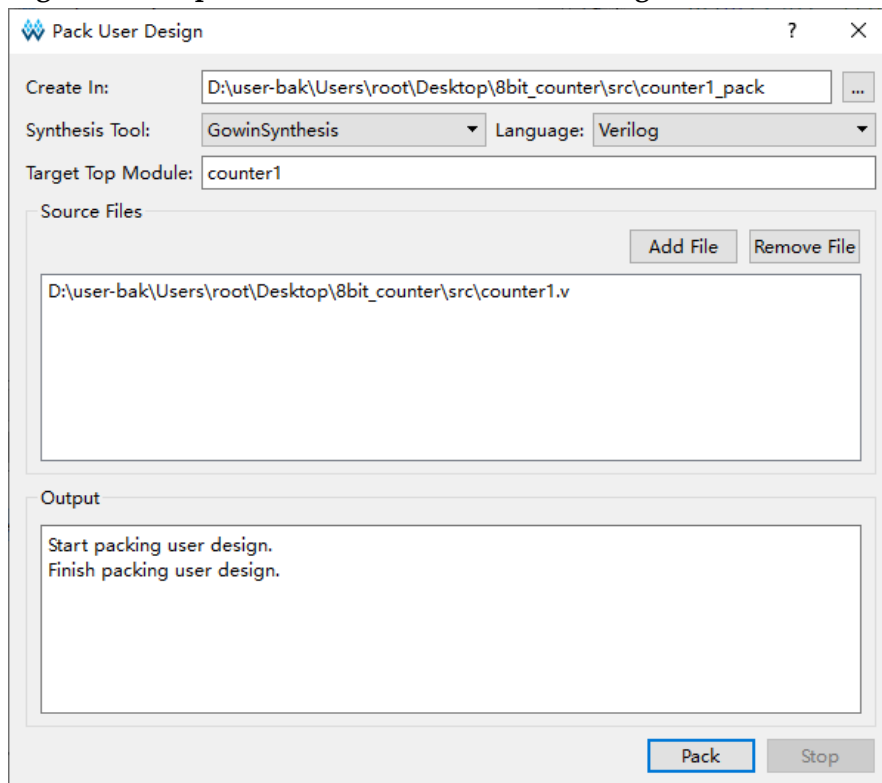
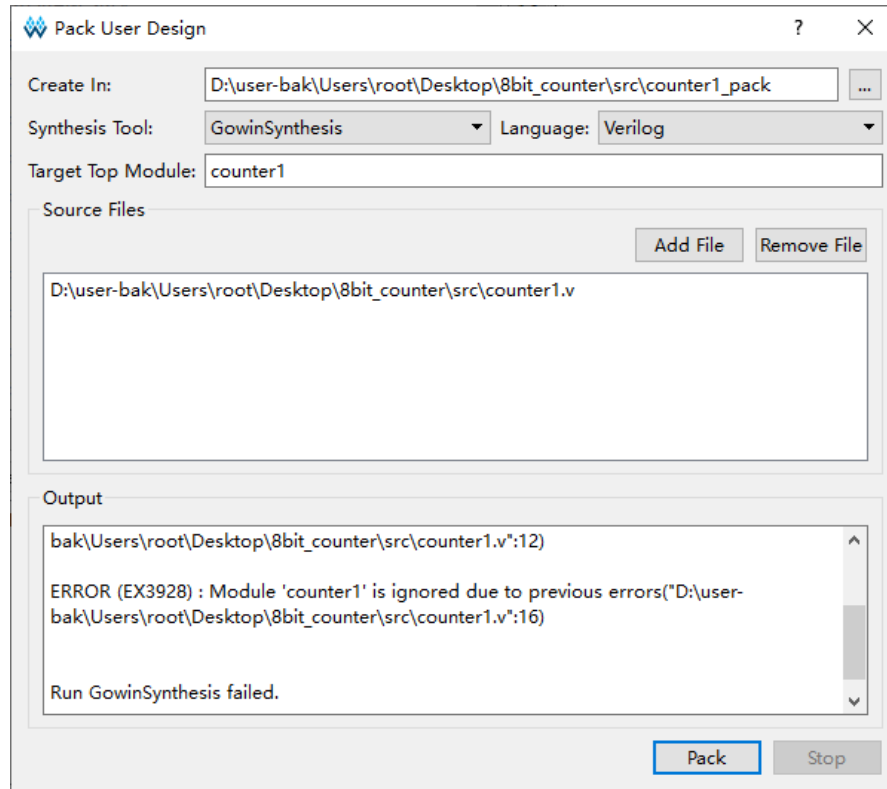


Figure 3-6 Error Prompt

After pack, two files are generated under the target path. If Verilog selected, the two files are <topmodule_name>_gowin.vp and <topmodule_name>_sim.v. If VHDL selected, the two files are <topmodule_name>_gowin.vhdp and <topmodule_name>_sim.v. <topmodule_name>_gowin.vp and <topmodule_name>_gowin.vhdp are pack file and can be used by others. <topmodule_name>_sim.v is a flattened plain netlist that can be used for internal simulation. <topmodule_name>_sim.v is a flattened plain netlist that can be used for internal simulation.

3.7 Source File Editing Area

You can view, edit and highlight source files in the source file edit area.

The source file editing area shows different files, including new files or opened files, the generated files after synthesis or Place & Route, and it also shows "Start Page" and "Design Summary".

If the file is displayed in the editing area and a modification is performed on the file externally, "File Changed" will pop up in the file editing area. Select "Reload" to reload the file.

Click "File > Close", or click the icon "✕" in the file editing area to close current files.

Click "File > Close All" to close all the files in the file editing area.

Open a file, and you can open "Find & Replace" dialog box by shortcut Ctrl+F or clicking "Find & Replace" in the toolbar. There are three options in

"Find All": Current File, Open Files and Current Project, as shown in Figure 3-7. After clicking "Find All", "Search Result" view will pop up and the search content will be highlighted, and the total number of matches is displayed at the end of the first line, as shown in Figure 3-8.

Figure 3-7 Find & Replace Dialog Box

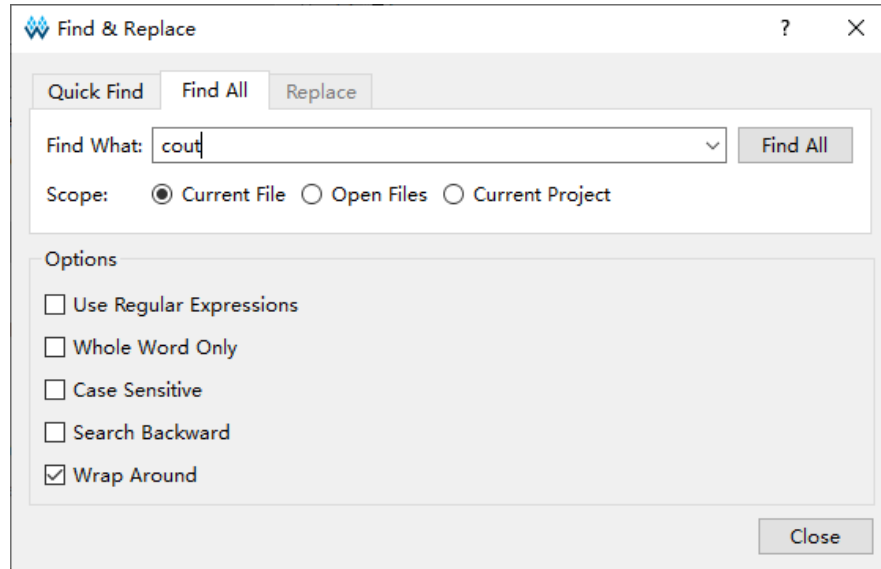
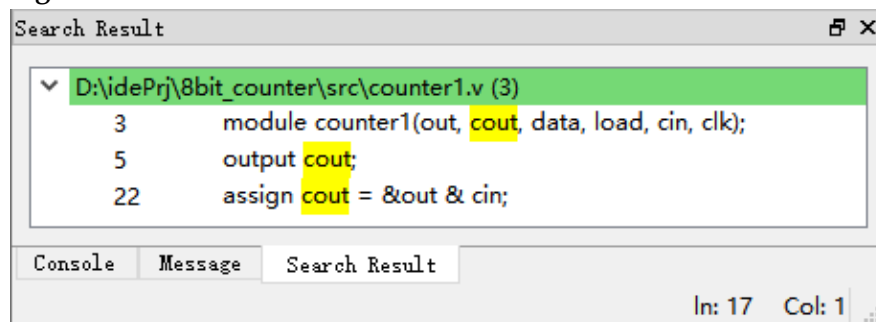


Figure 3-8 Search Result View

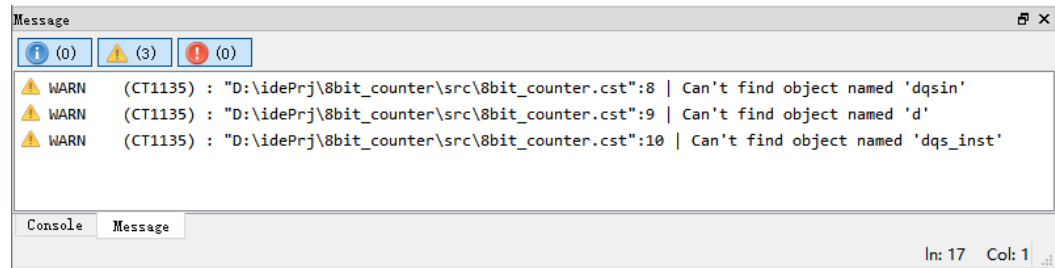


3.8 Information Output area

The information output area displays the processing information when the software is running. You can view different outputs by manually switching between the tabs:

- Console page includes tcl commands, warnings, errors, etc.
- Message page includes note, warning, error.

In Console page, right-click and select "Clear" to clear all the information in the tab. You can configure the message page to display note only, warning only or error only. The number of notes, warnings and errors will be recorded and shown on each of the corresponding tabs, as shown in Figure 3-9. Right-click and select "Clear" on "Message" page to clear the page information.

Figure 3-9 Information Output Area

After selecting an Error or Warning message reported by PnR, right-click and select "Help" or press the shortcut key "F1", the "GOWIN Help" of this error or warning will pop up, and the help information of this error or message will be described in details in the document. Some common warnings or errors are shown in Table 3-1, and help documents can be viewed by clicking "Help > View Help", which supports Chinese and English versions.

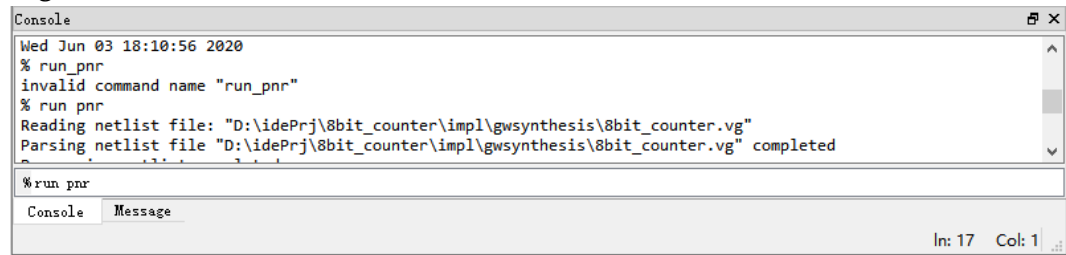
Table 3-1 Common Warnings and Errors

Name	Code	Description
Warning	WARN (PA1002): <file>:<line> Invalid parameterized value <value>(<parameter>) specified for instance <instanceName>	The specified instance sets invalid parameters.
	WARN (PA1008): <file>:<line> Object <name> is already defined	The net or port has already been defined.
	WARN (PA1001) : Dangling net <netName>(source:<instanceName>) in module <moduleName> has no destination	The net in the specified module has no destination.
	WARN (CT1098) : <file>:<line> Group name <name> is already defined	The constraints group name has already been defined.
	WARN (CT1101) : <file>:<line> Location column <number> is out of chip range(<maxColumn>)	The location column is out of chip range.
Error	ERROR (PA2000): <file>:<line> Syntax error near token <name>	There is an error near token.
	ERROR (PA2001): <file>:<line> Module <moduleName> is already defined	The module name has already been defined.
	ERROR (PA2017): The number(<value>) of <instType> in the design exceeds the resource limit(<maxValue>) of current device	The number of the devices in the design file exceeds the resource limit.
	ERROR (PA2025): No <instType> resource in current device	There are resources that are not supported by the chip in the design.
	ERROR (PA2054): <file>:<line> <name> is already declared	The name has already been declared.

The Tcl editing window locates at the bottom of the Console page. You

can enter Tcl commands in the window and press the Enter key to execute, as shown in Figure 3-10. For the details of Tcl, please refer to [8 Tcl Commands](#).

Figure 3-10 Tcl Commit Window



```
Console
Wed Jun 03 18:10:56 2020
% run_pnr
invalid command name "run_pnr"
% run_pnr
Reading netlist file: "D:\idePrj\8bit_counter\impl\gwsynthesis\8bit_counter.vg"
Parsing netlist file "D:\idePrj\8bit_counter\impl\gwsynthesis\8bit_counter.vg" completed

%run_pnr
Console Message
In: 17 Col: 1
```

4 Gowin Software Usage

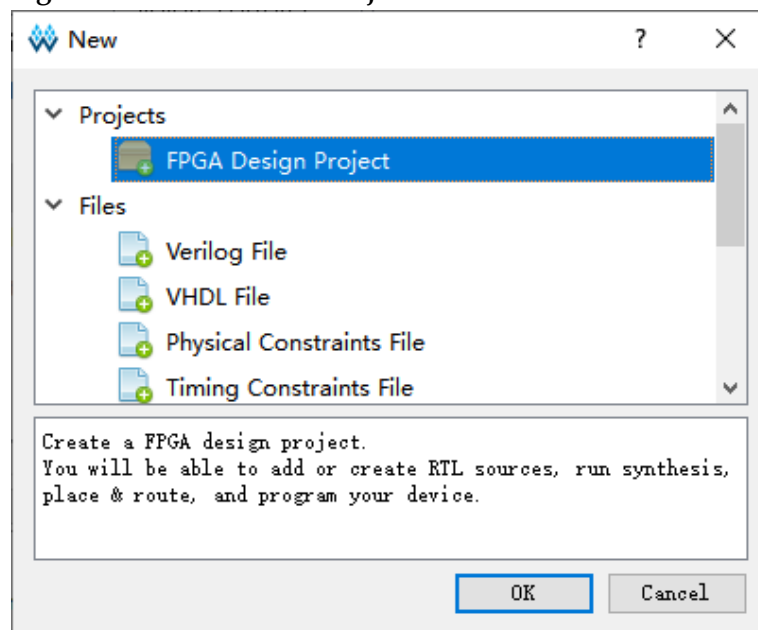
Gowin Software supports interface mode and command line mode. For command line mode, please refer to [8 Tcl Commands](#).

Take Gowin Software in Windows10 as an example to introduce how to use the software.

4.1 Create a New Project

1. From the File menu, choose "File> New..." to open the "New" dialog, as shown in Figure 4-1.

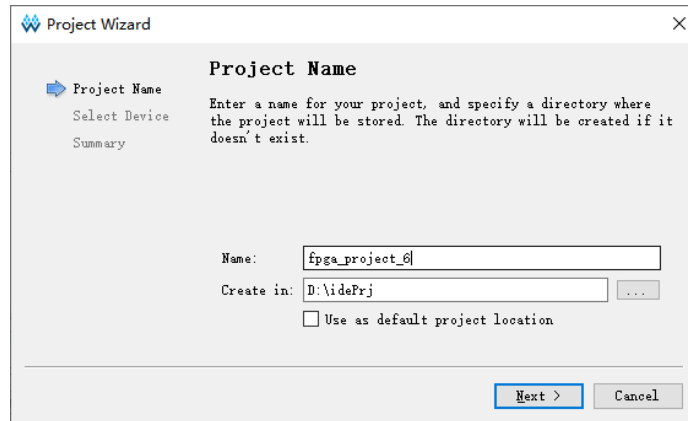
Figure 4-1 Create a New Project




Note!

There are three ways to open a "New" dialog:

- Use the "Ctrl+N" shortcut.
 - Click the "New File or Project" icon in the toolbar.
 - Click "Quick Start > New Project" on the Start Page.
2. Select "FPGA Design Project", and then click "OK" to open "Project Wizard", as shown in Figure 4-2.

Figure 4-2 Project Wizard

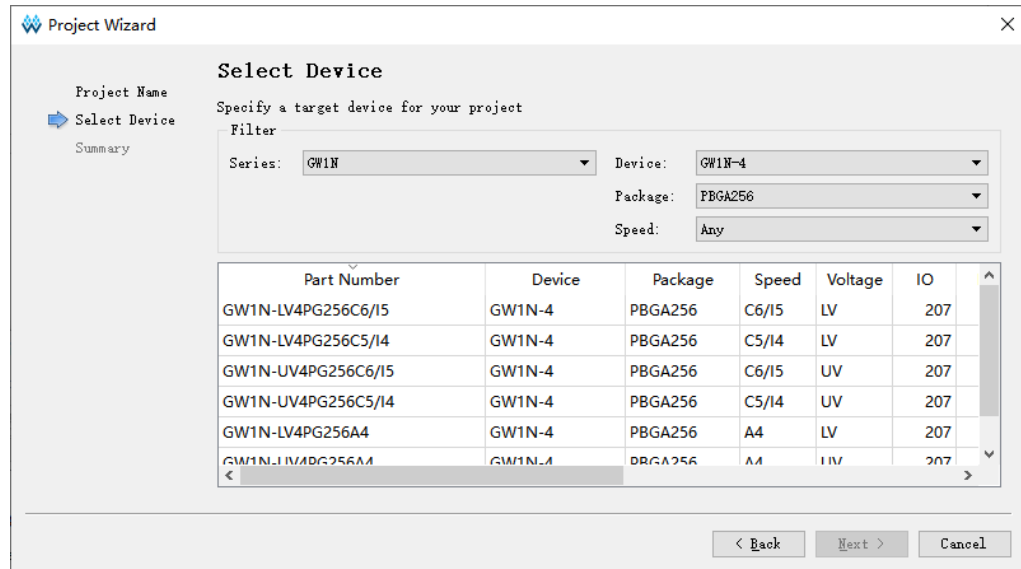
3. Create the project "Name" and "Create in", as shown in Figure 4-2.

- a) Type the project name in the "Name" text box.
- b) Click the " " icon to choose the project path.

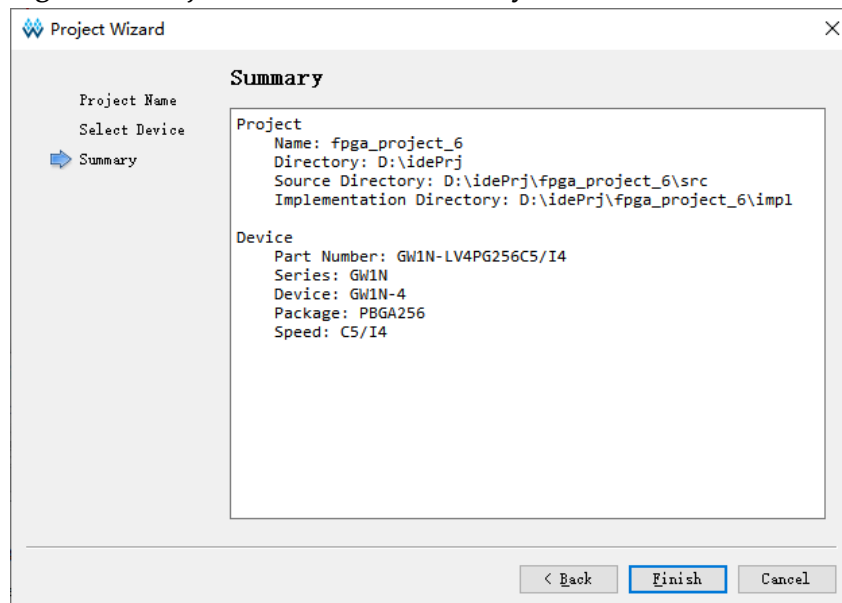
If you select "Use as default project location", the project location will be set as the default, and all later projects you create will be saved to this location.

Note!

- The file path length is limited in Windows and Linux, with a limit of 260 characters in Windows and 4096 characters in Linux. If beyond the limit, you cannot delete or copy the file path.
 - The path separator is "\" in Windows; for example, E:\Gowin\ide.
4. Click "Next" to set the device, including Series, Device, Package, and Speed.
- You can select series in Series.
 - You can select device in Device.
 - You can select package in Package.
 - You can select speed in Speed.
 - You can select part number in Part Number, and it displays the detailed information, as shown in Figure 4-3.

Figure 4-3 Select Device

5. Click "Next" to open the project information summary window, as shown in Figure 4-4 .

Figure 4-4 Project Information Summary

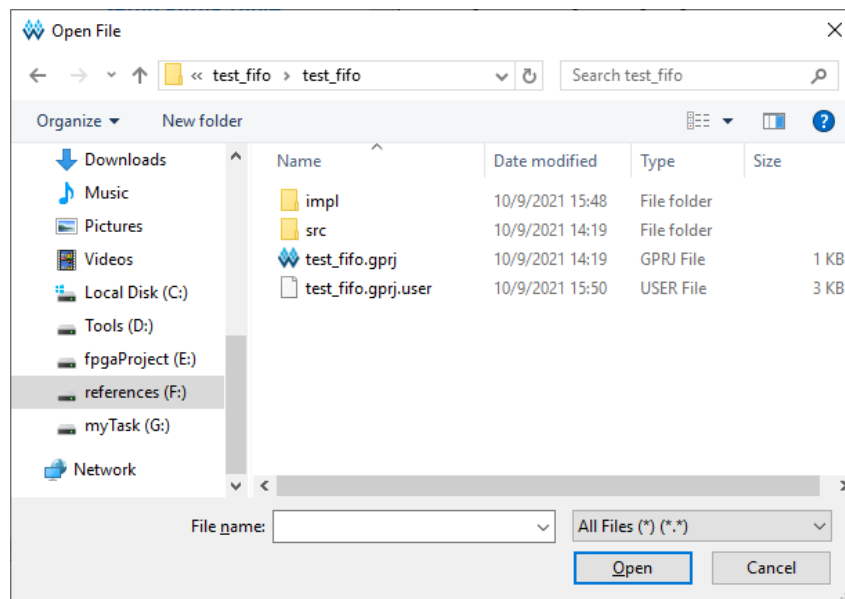
6. Click "Finish", and the project now is created.

4.2 Open an Existing Project

Use one of the following five methods to open an existing project.

Open From Tool Bar

1. You can click the "📁" icon in the tool bar to open the "Open File" dialog box, as shown in Figure 4-5.
2. Choose the project file (*.gprj) and click "Open" to open it.

Figure 4-5 Open an Existing Project**Open From Menu Bar**

1. In the menu bar, select "File > Open ..." to open the "Open File" dialog box, as shown in Figure 4-5.
2. Choose the project file (*.gprj) and click "Open" to open it.

Open from Start Page

1. On the start page, click "Open Project..." to open "Open Project" dialog box.
2. Choose the project file (*.gprj) and click "Open" to open it.

Open from Recent Projects

In the menu bar, click "File > Recent Projects" to open your required project.

Note!

- You can also open the project in the "Start Page > Recent Projects" list.
- The "Recent Projects" list shows the recently opened projects.
- If the project has been deleted, the "Open Project" dialog box will pop up.

Open From Project File

Find the *.gprj file, and double-click on *.gprj file to open the project automatically.

4.3 Edit a Project

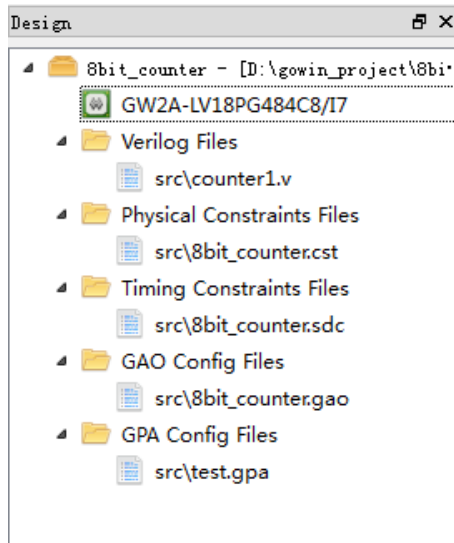
After creating or opening a project, you can edit the device information and the related files in the project design area, as shown in Figure 4-6.

The Project Design Area contains the following:

- The project path
- Part number

- The current project files, including user design files , physical constraints files (.cst.), timing constraints files (.sdc), GAO config files (.gao, .rao), and GPA config files (.gpa), etc

Figure 4-6 Project Design Area



4.3.1 Edit a Project Device

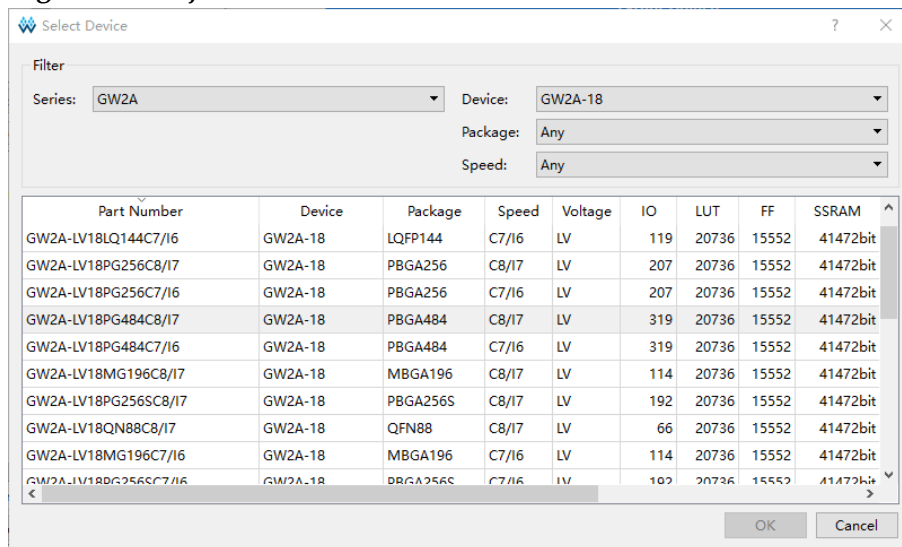
The chip information used in the current FPGA project can be edited in the project design view.

1. As shown in Figure 4-6, double-click "GW2A-LV18PG484C8/I7" to open the "Select Device" dialog box, or choose "Set Device" from Project pull-down list, as shown in Figure 4-7.
2. In the "Select Device" dialog box, select part number from the "Part Number".

Note!

The "Part Number" will display the detailed resource information related to the selected device.

Figure 4-7 Project Device Info.



4.3.2 Edit a Project File

Files that need to be added in projects include RTL design files (Source Files), constraints files, and configuration files. Refer to the following descriptions to edit the project files.

Create Design and Constraints Files


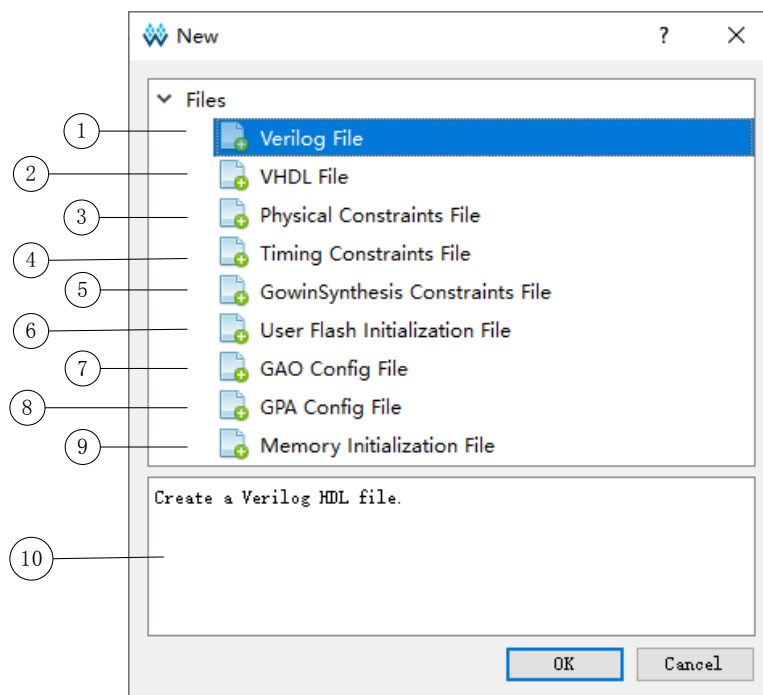
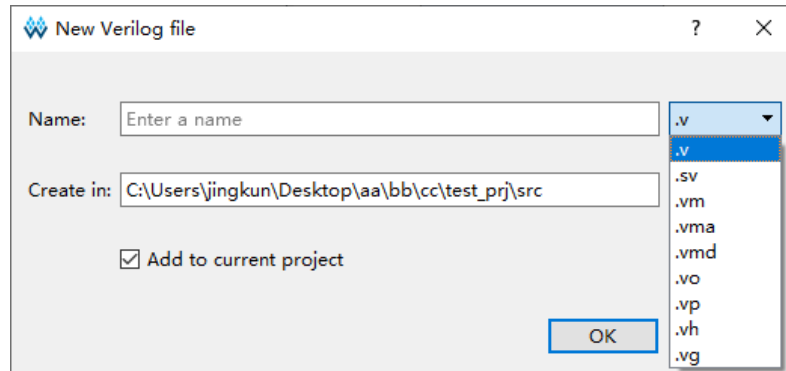
1. Click " " in the tool bar, or select "File > New File..." in the menu bar to open the "New..." dialog box.
2. As shown in Figure 4-8, select a file.

Figure 4-8 Create a New File Dialog Box



- | | |
|-----------------------------------|----------------------------------|
| ① Verilog File | ② VHDL File |
| ③ Physical Constraints File | ④ Timing Constraints File |
| ⑤ GowinSynthesis Constraints File | ⑥ User Flash Initialization file |
| ⑦ GAO Config File | ⑧ GPA Config File |
| ⑨ Memory Initialization File | ⑩ File Description |

3. Take creating a Verilog File for an instance. Select "Verilog File" to open the Verilog File dialog box, as shown in Figure 4-9. Check "Add to current project" by default, i.e. the new design file will be added to the current project by default.

Figure 4-9 Create Verilog File Dialog Box

4. Type the file name and click "OK".

Create a Configuration File


1. Click " " in the tool bar, or select "File > New File..." in the menu bar to open the "New..." dialog box, as shown in Figure 4-8.
2. As shown in Figure 4-8, select a file. Take creating a GPA Config File for an instance. Select "GPA Config File" and to open New GPA Config File dialog box; type the file name, click "OK", and the new GPA profile will be automatically added to the project design area, as shown in Figure 4-10.
3. Double click on this configuration file in the project design area to open a window for editing, as shown in Figure 4-11.

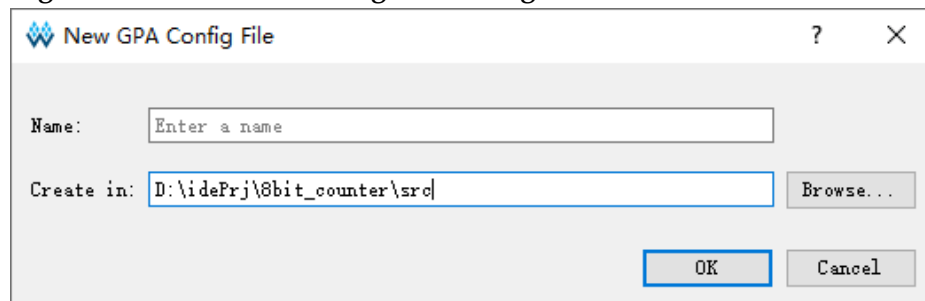
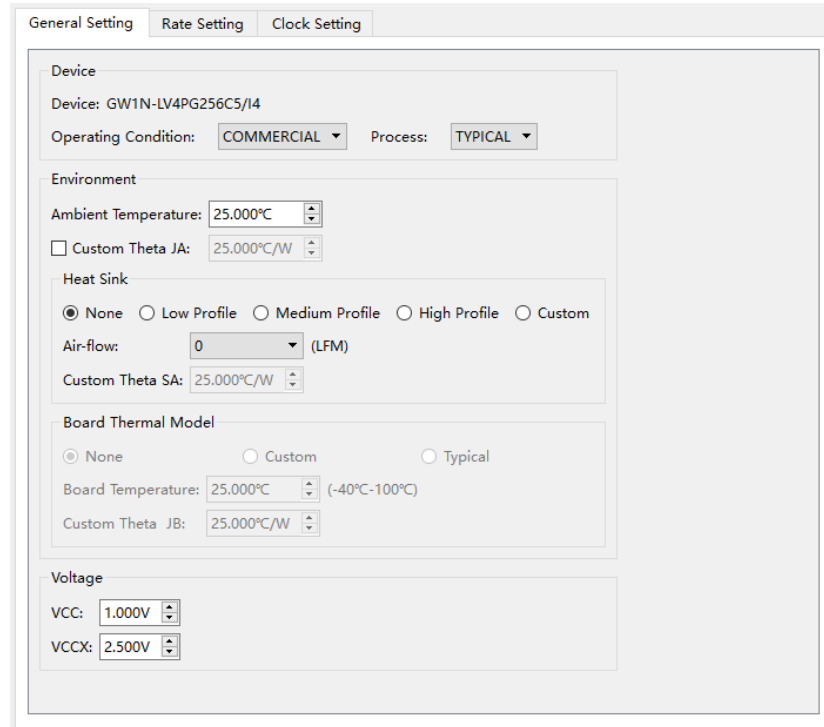
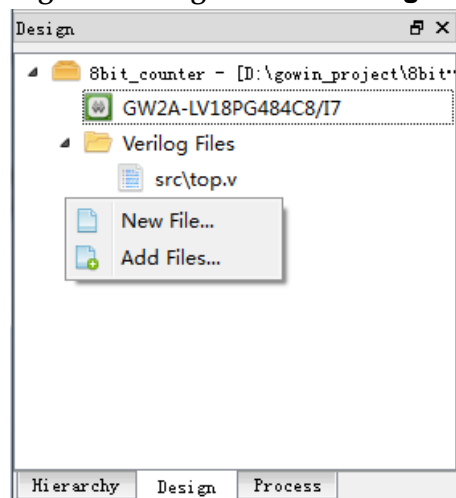
Figure 4-10 New GPA Config File Dialog Box

Figure 4-11 GPA Config File Window

Add Project Files

1. As shown in Figure 4-12, right-click in the blank of the project design area, select "Add Files..." to open the "Select Files" dialog box.
2. Select single or multiple project files to add. Gowin Software will automatically classify the files in the project design area. If the added files are not RTL design files, netlist files, constraints files, GPA configuration files, or GAO configuration files, "Other Files" will be added in the project design area.

Figure 4-12 Right-click in Design View

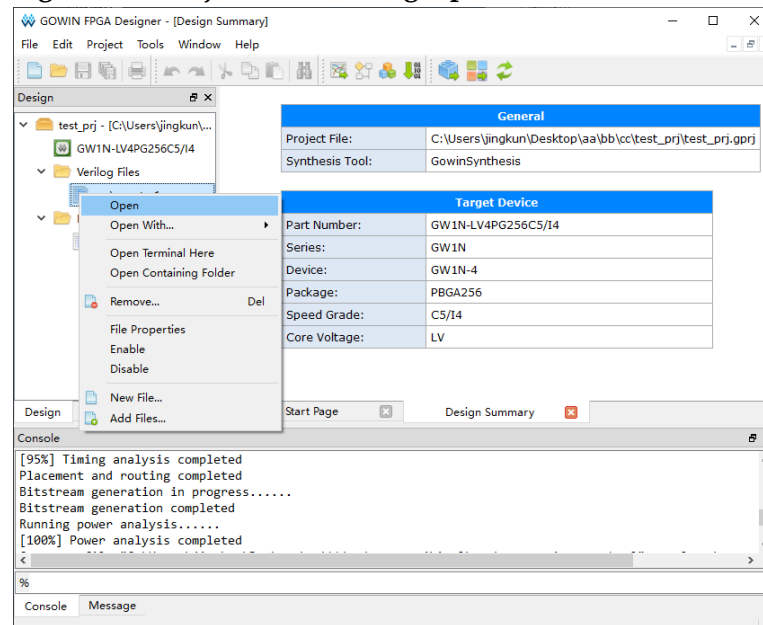
Modify Project Files

Use the following two methods to open the project files, as shown in

Figure 4-13.

1. Double-click any file in the project design area; the file will open in the source file editing area.
2. Right-click on the file that is to be modified and click "Open".

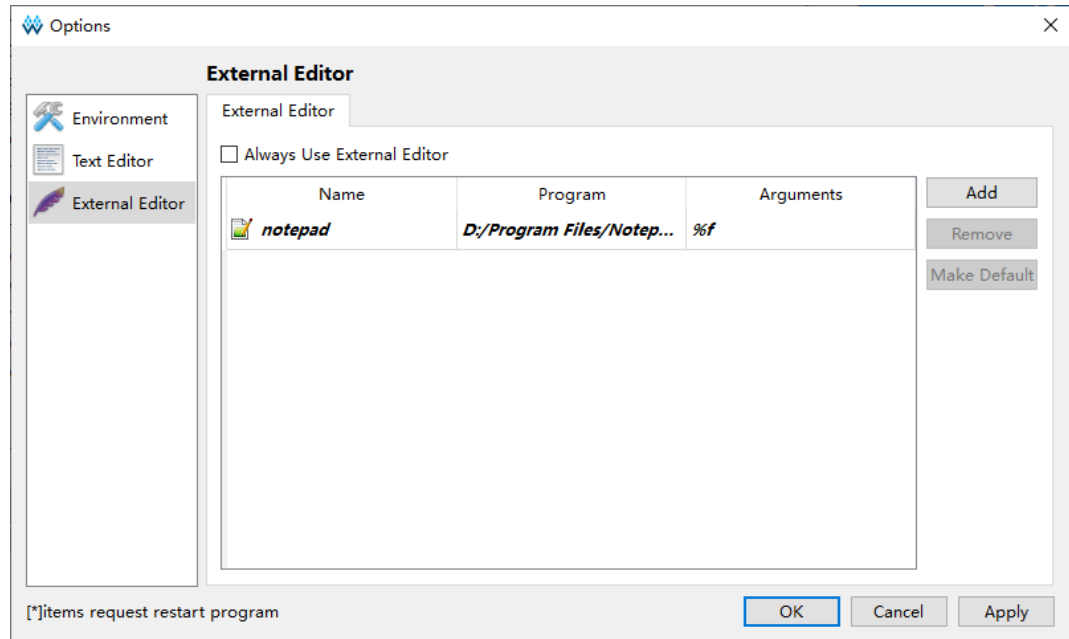
Figure 4-13 Project Files Editing Options



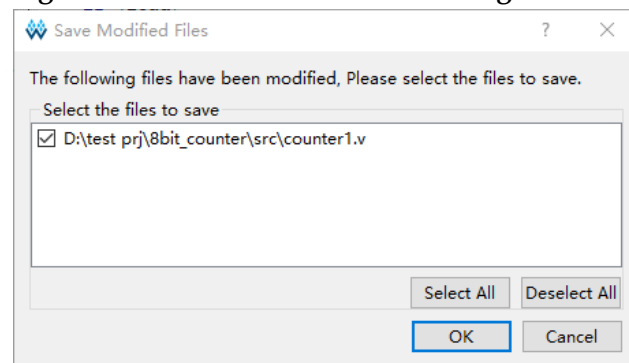
If you have configured a third-party text editor by clicking "Tools > Options", select "Open With..." to open the design file with the third-party text editor. If you select "Add External Editor", you can add other external editor, as shown in Figure 4-14. If you check "Always Use External Editor", the external editor will always be used to open files. If you select "Open Containing Folder", you can open the folder. If you select "Open Terminal Here", you can use command line mode.

If you modify and save a file by an external editor, Gowin software will generate a reload prompt.

If you close the unsaved file after editing, Gowin will pop up a warning.

Figure 4-14 External Editor

After project files are modified, if you run Synthesize or Place & Route before saving these files, the "Save Modified Files" dialog box will pop up, as shown in Figure 4-15.

Figure 4-15 Save Modified Files Dialog Box

Click "OK"; the files will be saved and then perform previous operations automatically. Click "Cancel"; the files will not be saved and Synthesize or Place & Route will not be performed.

Delete Project Files

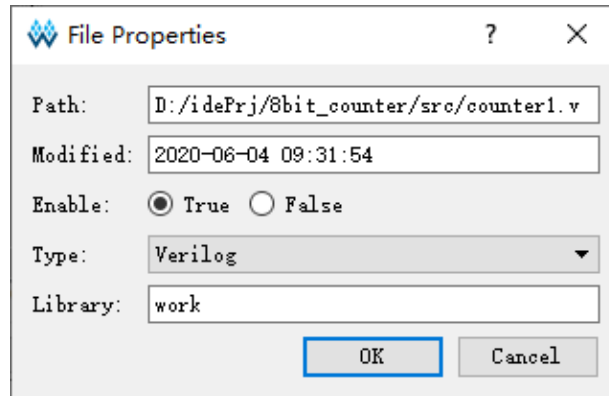
1. Select the file in the project design area.
2. Right-click and select "Remove", or directly press the Delete key to open the "Delete File" dialog box. If you select the "Delete Permanently" check box, the file is deleted from the current project and on disk. Otherwise, the file is deleted only from the current project.

Edit Project File Attributes

Right-click any file in the project design area, select File Properties from the right-click list, and "File Properties" dialog box pops up, as shown

in Figure 4-16. The path, modified time, Enable, Type, and Library information are displayed in the dialog box. The file type can be modified in the Type drop-down list. After clicking "OK", the file will automatically move to the selected type in the Design view. Library is used to specify the library used by VHDL files synthesis, and the default is work.

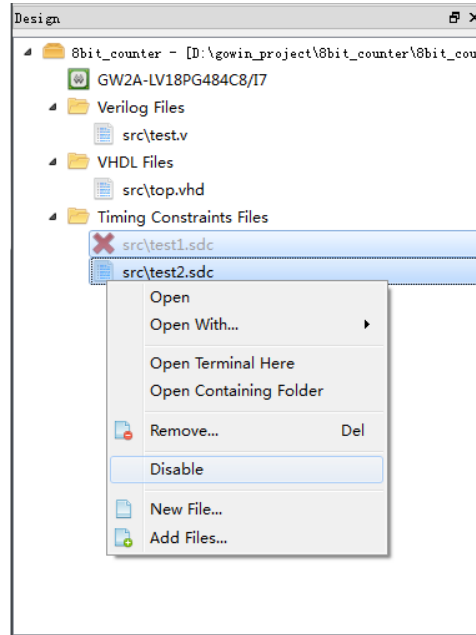
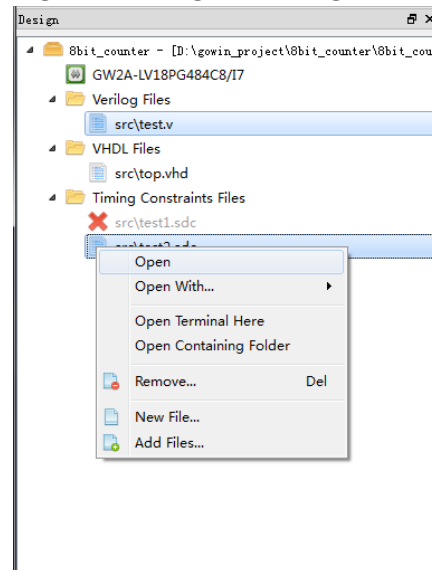
Figure 4-16 File Properties Dialog Box



Enable Project Files

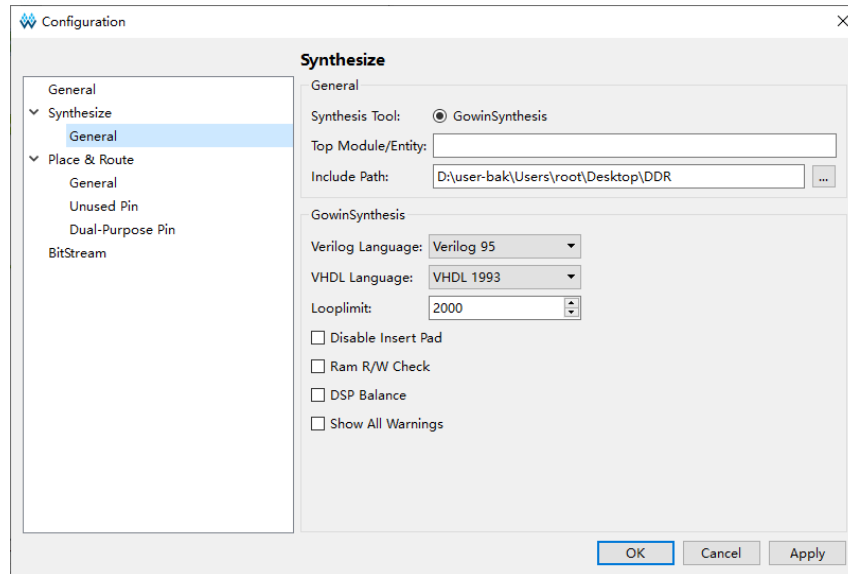
You can see the "Enable" and "Disable" options by right-clicking on any files in the project design area, as shown in Figure 4-13. The files are in the project compilation process when it is enabled, and out of project compilation process when it is disabled.

1. Set Enable/Disable by right-clicking, including single/batch files setting.
2. If multiple design files (Verilog Files、VHDL Files or Netlist Files) are selected, "Enable" and "Disable" are both available.
3. If multiple constraints files or configuration files are selected, "Enable" is not available, and "Disable" is available, as shown in Figure 4-17.
4. For constraints files or configuration files of the same type, only one file can be in "Enable"; when you create or add a new file of the same type, the previous one will be disabled; when multiple files of different types are selected, both "Enable" and "Disable" are not available, as shown in Figure 4-18.

Figure 4-17 Right-clicking of Selecting Same Type Files**Figure 4-18 Right-clicking of Selecting Different Types Files**

4.3.3 Edit Project Configuration

Right click "Synthesize" or "Place & Route" in the Project Design area to open the project configuration dialog box, as shown in Figure 4-19.

Figure 4-19 Project Configuration Dialog Box

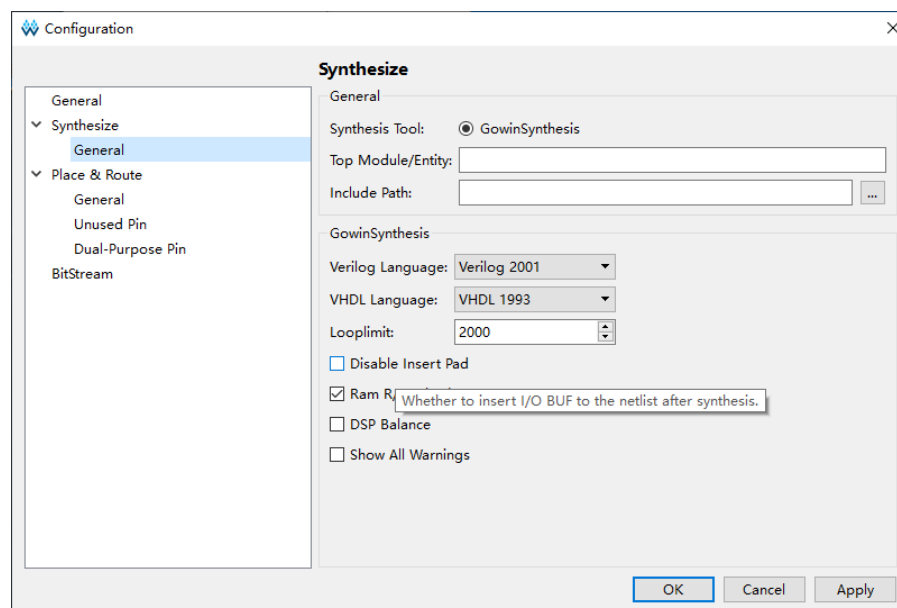
As shown in Figure 4-19, the project configuration includes General, Synthesize, Place & Route and BitStream. The details of the options are as follows.

General

Project basic option; specify the name of the output file, and the default is the name of the current project.

Synthesize

The synthesis tool is GowinSynthesis[®]; hovering the mouse over some options will display their explanations, as shown in Figure 4-20.

Figure 4-20 GowinSynthesis Configuration Options

The detailed descriptions are shown below.

- Top Module/Entity: Specifies top module/entity
- Include Path: Specifies include path
- Verilog Language: System Verilog 2017, Verilog 2001 and Verilog 95, and the default is Verilog 2001.
- VHDL Language: VHDL 1993 and VHDL 2008, and the default is VHDL1993.
- Looplimit: Sets the loop limit value of the default editor in RTL, and the default Value is 2000.
- Disable Insert Pad: Whether to insert I/O buffer to the post-synthesis netlist, not checked by default.
- Ram R/W Check: If there is a read or write conflict in RAM, check this option and bypass logic will be inserted around RAM to prevent simulation mismatches. If this option is disabled, bypass logic will not be generated, checked by default.
- DSP Balance: If the DSP resource exceeds the limit when the design is synthesized, check this option to synthesize the excess DSP to registers, not checked by default.
- Show All Warnings: All warnings will be printed during synthesis if this option is checked, not checked by default.

Note!

For the details, see [SUG550](#), GowinSynthesis User Guide

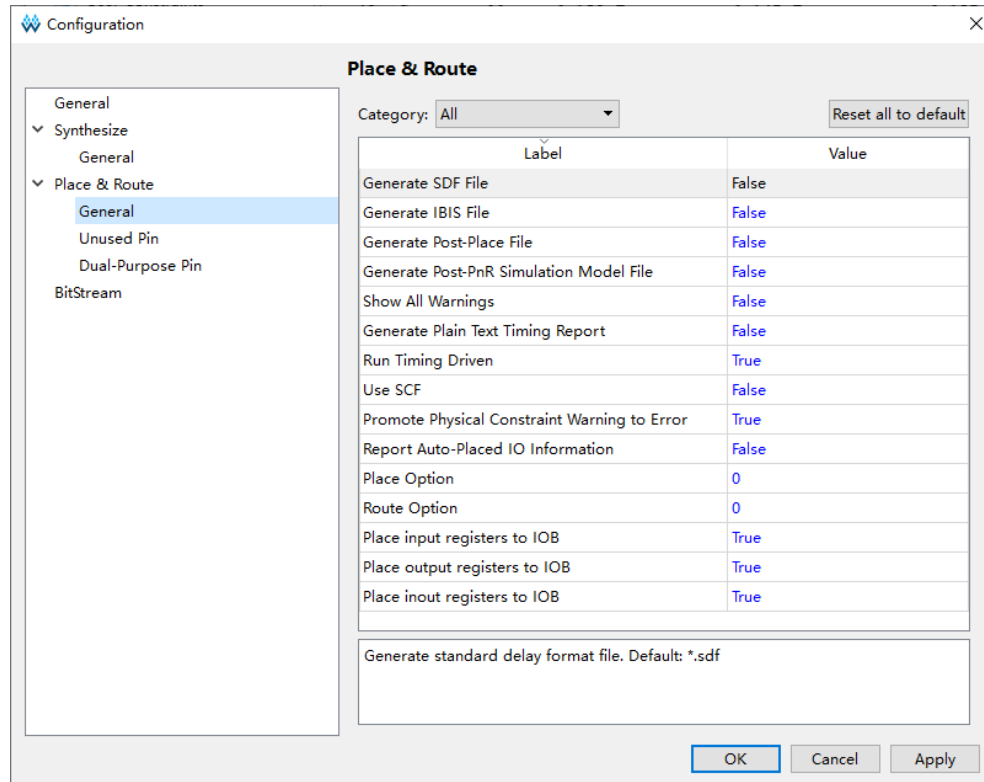
Place & Route

Place & Route includes General, Unused Pin and Dual-purpose Pin, and the detailed descriptions are shown in Table 4-1.

Table 4-1 PnR Configuration Options

Option	Description
General	Set PnR parameters
Unused Pin	Set different IO types and properties for unused pin (except for unused pins of the dual-purpose pins)
Dual-Purpose Pin	Used to configure the I/O corresponding to the package in the selected device, mainly for configuring dual-purpose pins.

Reset all to default: Resets all configurations on the page to the default values. The General configuration is as shown in Figure 4-21.

Figure 4-21 Place & Route Configuration

The descriptions of options in Figure 4-21 are as follows.

- **Generate SDF File:** Generates a standard delay format file with the extension .sdf for netlist timing simulation after PnR, and the default value is False. For the usage, see [7 Simulation Files](#).
- **Generate IBIS File:** Generates the file specified by the input/output buffer information, with the extension .ibs, and the default is False.
- **Generate Post-Place File:** Generates a file containing only BSRAM placement information, with the extension .posp, and the default value is False.
- **Generate Post-PNR Simulation Model File:** Generates a timing simulation model file for timing simulation, with the extension .vo, and the default value False.
- **Show All Warnings:** Outputs all the Warning information when PNR is running, and the default value is False.
- **Generate Plain Text Timing Report:** Generates a timing report in text format, with the extension .tr, and default value is False.
- **Run Timing Driven:** Optimizes PnR by timing driven, and the default value is True.
- **Promote Physical Constraint Warning to Error:** Promotes the physical constraint warning to an error, and the default value is True.
- **Report Auto-Placed IO Information:** Reports the location information of auto-placed IO, and the default value is False.

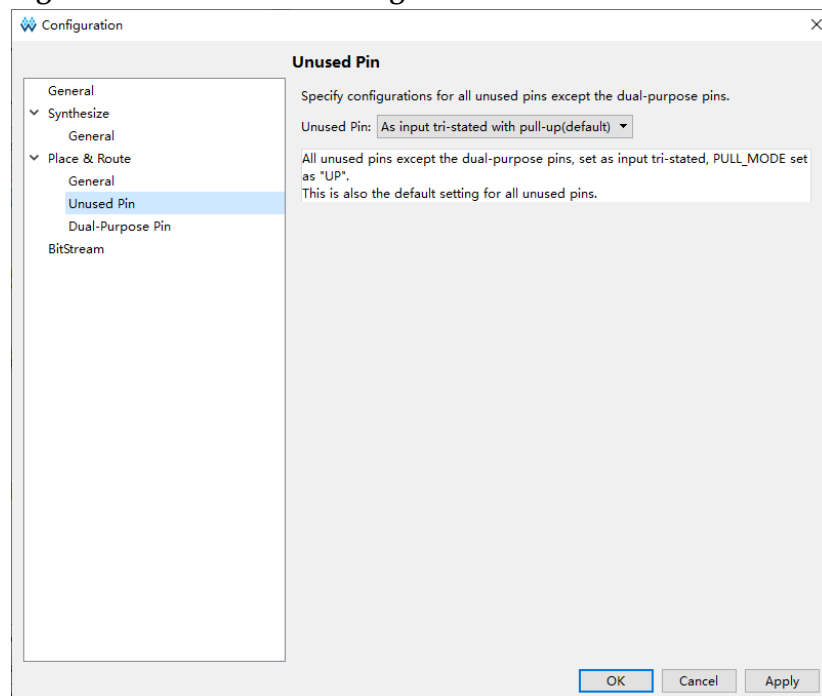
- **Place Option:** Place algorithm with the value of 0 and 1, and the default value is 0.
 - If it is 0, the default place algorithm is used.
 - If it is 1, some time efficiency is sacrificed to try to find a better place based on algorithm 0.
- **Route Option:** Route algorithm with the value of 0, 1 and 2, and the default value is 0.
 - When it is 0, the default route algorithm is used, and the route is adjusted according to congestion.
 - When it is 1, the route is adjusted according to the timing.
 - When it is 2, the route speed will be relatively fast.

If the route algorithm of 0 does not work well, it is recommended to try algorithm 1 or 2.
- **Place input register to IOB:** Places registers driven by input Buffer to IOB, and the default value is True.
- **Place output register to IOB:** Places registers driven by output/tristate Buffer to IOB, and the default value is True.
- **Place inout register to IOB:** Places registers driven by in/out Buffer to IOB, and the default value is True.

Unused Pin

You can configure packaged but unused pins (except for dual-purpose pins) via Unused Pin option. There are two options: As input tri-stated with pull-up (default) and As open drain driving ground, as shown in Figure 4-22.

Figure 4-22 Unused Pin Configuration

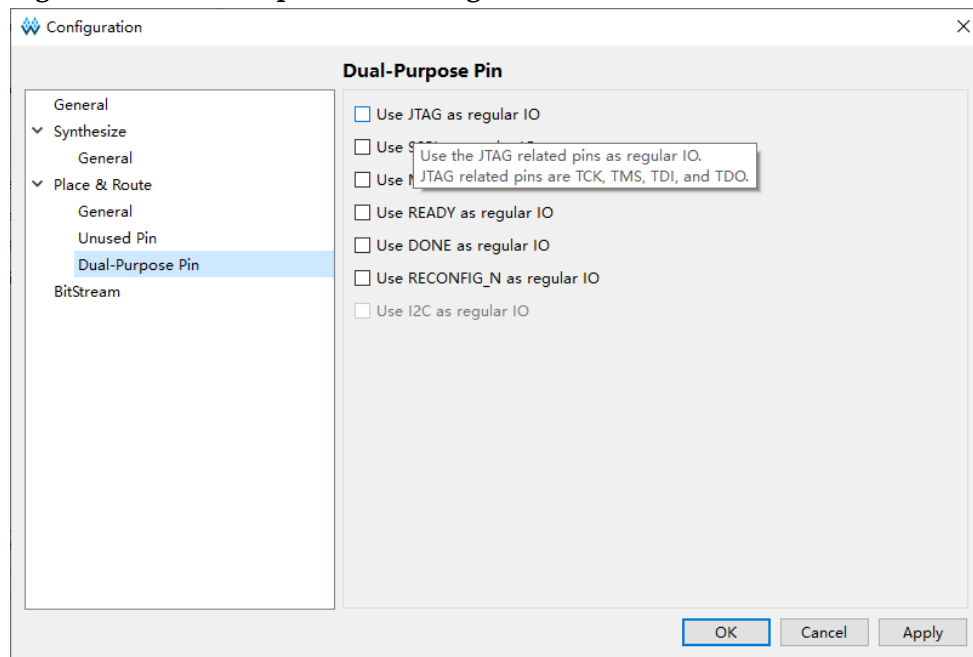


- As input tri-stated with pull-up (default): All pins that are not used by you (except for the dual-purpose pin) are configured to input tri-stated with pull-up.
- As open drain driving ground: All pins that are not used by you (except for the dual-purpose pin) are configured to output with OPEN_DRAIN ON.

Dual-Purpose Pin

The Dual-purpose Pin is a configuration that conforms to the Gowin device customization, and hovering the mouse over the option will display its explanation. The configuration is as shown in Figure 4-23.

Figure 4-23 Dual-Purpose Pin Configuration



The dual-purpose pins are described as follows.

- Use JTAG as regular IO: Use relevant pins of JTAG as regular IO pins. These relevant pins are TCK, TMS, TDI, and TDO.
- Use SSPI as regular IO: Use relevant pins of SSPI as regular IO pins. These relevant pins are SCLK, CLKHOLD_N, SI, SO, SSPI_CS_N.
- Use MSPI as regular IO: Use relevant pins of MSPI as regular IO pins. These relevant pins are MCLK, MCS_N, MI, MO.
- Use READY as regular IO: Use the READY pin as regular IO pin.
- Use DONE as regular IO: Use the DONE pin as regular IO pin.
- Use RECONFIG_N as regular IO: Use the RECONFIG_N pin as regular IO pin.
- Use I2C as regular IO: Use relevant pins of I2C as regular IO. These relevant pins are SCL and SDA. The supported device and package are as follows.

- GW1NR-2/GW1NR-2B/GW2AN-9X/GW2AN-18X
- GW1N-2/GW1N-2B package: LQFP100X/LQFP144X/ MBGA132X/WLCSP42/QFN48/ QFN48E/ MBGA132H/ WLCSP42H/QFN48H
- GW1N-1P5/ GW1N-1P5 package: LQFP100X.

Bitstream

You can configure the bitstream file format and frequency, etc. via BitStream. Hovering the mouse over the option will display its explanation. The configuration option is as shown Figure 4-24.

Figure 4-24 Bitstream Configuration

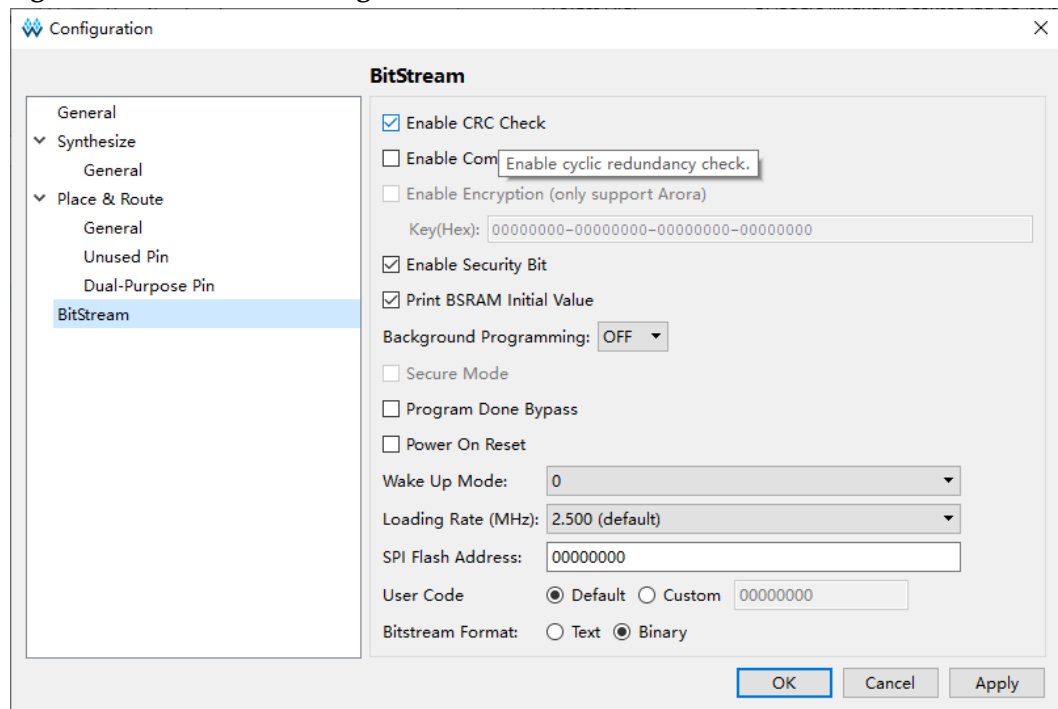


Figure 4-25 Set Background Programming to I2C

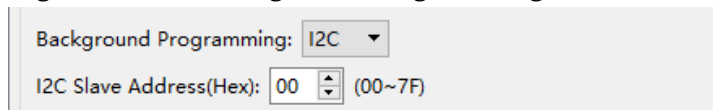
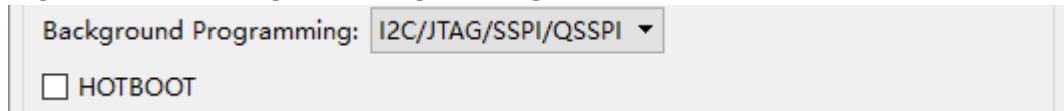


Figure 4-26 Set Background Programming to I2C/JTAG/SSPI/QSSPI



The description for each parameter is as follows.

- Enable CRC Check: Enable CRC Check, checked by default.
- Enable Compress: Enable bitstream file compress, not checked by default.

- Enable Encryption (only support Arora family): Encrypt the bitstream file, supporting Arora only, not checked by default.
- Key(Hex): Key(Hex) can be configured only when "Enable Encryption (only supports Arora)" is checked. This enables you to customize the secret key, and key is all 0 by default.
- Enable Security Bit: Enable security bit, and add security bit to the bitstream file; after adding, the bitstream cannot be read back again, checked by default.
- Print BSRAM Initial Value: Print BSRAM initial value to the bitstream file, checked by default.
- Background Programming: You can re-program Flash without interrupting the current FPGA running.

The devices that support background programming and their values are shown in Table 4-2.

Table 4-2 Background Programming Value

Device	Background Programming Value
GW1N-1P5/GW1N-2/GW1NR-2, GW1N-4/GW1N-4B, GW1NR-4B/GW1NR-4D/GW1NRF-4B, GW1NS-4/GW1NSR-4, GW1N-9/ GW1N-9C, GW1NR-9/GW1NR-9C, GW1NZ-1/GW1NZ-1C	OFF, JTAG; OFF by default
GW1N-1P5B/GW1N-2B/GW1NR-2B	OFF, JTAG, I2C; OFF by default
GW2AN-18X/GW2AN-9X	OFF, Internal, I2C/JTAG/SSPI/QSSPI; OFF by default

Each value of Background Programming is described as follows.

- OFF: Off Background Programming, if the device is GW2AN-18X or GW2AN-9X, "Use MSPI as regular" in the "Dual-Purpose Pin" dialog box is unchecked and not configurable.
- JTAG: Use JTAG mode for background programming
- I2C: Use I2C mode for background programming; "I2C Slave Address (Hex)" is used to set the address of the I2C device, with the value range of 00~7F, as shown in Figure 4-25. After selecting I2C, "Use JTAG as regular IO" in the "Dual-Purpose Pin" dialog box is unchecked and not configurable.
- Internal: Use internal logic for background programming, and "Use MSPI as regular IO" in the "Dual-Purpose Pin" dialog box is checked and not configurable.
- I2C/JTAG/SSPI/QSSPI Use I2C/JTAG/SSPI/QSSPI mode for background programming, and "Use MSPI as regular IO" in the "Dual-Purpose Pin" dialog box is unchecked and not configurable.

- When Internal or I2C/JTAG/SSPI/QSSPI is selected, the configuration option "HOTBOOT" will display in the dialog box, as shown Figure 4-26, optional and unchecked by default.
- When the configuration or "HOTBOOT" is changed, Place & Route will be changed to expired. If the I2C is included before and after the configuration switch, Synthesize and Place & Route will be changed to expired.

Note!

The Background Programming cannot be checked when there is User Flash in the design, otherwise the Error prompt will be reported.

- Secure Mode (device can be programmed only once): Enable secure mode. Use JTAG pin as GPIO, and device can be programmed only once. This function is only supported by GW1NSE-2C and GW1NSER-4C, unchecked by default.
- Program Done Bypass: When the Done Final signal takes effect, the external Done pin keeps low, so that the new bitstream can be forwarded after the bitstream is loaded.
- Power On Reset: Enable power on reset, unchecked by default. When this option is checked, it will enter to reset mode when power on and clear all RAM bits; and set the used I/O to tri-state through the internal weak pull-up resistor, then complete the configuration and initialization.
- Wake Up Mode: Enable wake up mode, with the value of 0 and 1, and the default is 0.
 - When wake up mode is "0", DONE pin can be pulled up or down.
 - When wake up is "1",
 - a) if the DONE pin is pulled up, download and run normally.
 - b) If the done pin is pulled down, download normally; and DONE pin needs to be pulled up and keep TCK connected to the pulse signal to wake up chip.
- Loading Rate: In AutoBoot mode and MSPI mode, the rate of loading bitstream from Flash to SRAM is 2.500MHz by default. For the details, see [UG290](#), Gowin FPGA Products Programming and Configuration Guide; the loading rate and calculation method of different devices are different.
 - The loading rate and calculation method of following devices is as shown in Table 4-3.
 - a) GW1NZ-1/GW1NZ-1C
 - b) GW1N-2/GW1N-2B/GW1NR-2/GW1NR-2B/GW1N-1P5/GW1N-1P5B
 - c) GW1NSER-4C/GW1NS-4/GW1NSR-4/GW1NS-4C/GW1NSR-4C
 - d) GW1N-4B/GW1NR-4B/GW1N-4D/GW1NRF-4B/GW1N-4/GW1NR-4/GW1NR-4B/GW1NR-4D

- e) GW1N-9/GW1N-9C/GW1NR-9/GW1NR-9C
- f) GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C
/GW2ANR-18C
- g) GW2A-55/GW2A-55C/GW2AN-55C

Table 4-3 Loading Rate and Formula 1

Loading Rate (MHz)	Formula
2.500 (default)	250 / 100
5.435	250 / 46
5.682	250 / 44
5.952	250 / 42
6.250	250 / 40
6.579	250 / 38
6.944	250 / 36
7.353	250 / 34
7.812	250 / 32
8.333	250 / 30
8.929	250 / 28
9.615	250 / 26
10.417	250 / 24
11.364	250 / 22
12.500	250 / 20
13.889	250 / 18
15.625	250 / 16
17.857	250 / 14
20.833	250 / 12
25.000	250 / 10
31.250	250 / 8
41.667	250 / 6
62.500	250 / 4
125.000	250 / 2

- The loading rate and calculation method of following devices is as shown in Table 4-4.

- a) GW1N-1/GW1N-1S
- b) GW1NS-2/GW1NSR-2/GW1NS-2C/GW1NSR-2C/
GW1NSE-2C

Table 4-4 Loading Rate Value and Formula 2

Loading Rate (MHz)	Formula
2.500 (default)	240 / 96

Loading Rate (MHz)	Formula
2.553	240 / 94
2.609	240 / 92
2.667	240 / 90
2.727	240 / 88
2.791	240 / 86
2.857	240 / 84
2.927	240 / 82
3.000	240 / 80
3.077	240 / 78
3.158	240 / 76
3.243	240 / 74
3.333	240 / 72
3.429	240 / 70
3.529	240 / 68
3.636	240 / 66
3.750	240 / 64
3.871	240 / 62
4.000	240 / 60
4.138	240 / 58
4.286	240 / 56
4.444	240 / 54
4.615	240 / 52
4.800	240 / 50
5.000	240 / 48
5.217	240 / 46
5.455	240 / 44
5.714	240 / 42
6.000	240 / 40
6.316	240 / 38
6.667	240 / 36
7.059	240 / 34
7.500	240 / 32
8.000	240 / 30
8.571	240 / 28
9.231	240 / 26
10.000	240 / 24
10.909	240 / 22
12.000	240 / 20

Loading Rate (MHz)	Formula
13.333	240 / 18
15.000	240 / 16
17.143	240 / 14
20.000	240 / 12
24.000	240 / 10
30.000	240 / 8
40.000	240 / 6
60.000	240 / 4
120.000	240 / 2

- The loading rate and calculation method of following devices is as shown in Table 4-5.

- a) GW2AN-9X
- b) GW2AN-18X

Table 4-5 Loading Rate and Formula 3

Loading Rate (MHz)	Formula
2.500 (default)	200 / 80
1.562	200 / 128
1.587	200 / 126
1.613	200 / 124
1.639	200 / 122
1.667	200 / 120
1.695	200 / 118
1.724	200 / 116
1.754	200 / 114
1.786	200 / 112
1.818	200 / 110
1.852	200 / 108
1.887	200 / 106
1.923	200 / 104
1.961	200 / 102
2.000	200 / 100
2.041	200 / 98
2.083	200 / 96
2.128	200 / 94
2.174	200 / 92
2.222	200 / 90
2.273	200 / 88

Loading Rate (MHz)	Formula
2.326	200 / 86
2.381	200 / 84
2.439	200 / 82
2.564	200 / 78
2.632	200 / 76
2.703	200 / 74
2.778	200 / 72
2.857	200 / 70
2.941	200 / 68
3.030	200 / 66
3.125	200 / 64
3.226	200 / 62
3.333	200 / 60
3.448	200 / 58
3.571	200 / 56
3.704	200 / 54
3.846	200 / 52
4.000	200 / 50
4.167	200 / 48
4.348	200 / 46
4.545	200 / 44
4.762	200 / 42
5.000	200 / 40
5.263	200 / 38
5.556	200 / 36
5.882	200 / 34
6.250	200 / 32
6.667	200 / 30
7.143	200 / 28
7.692	200 / 26
8.333	200 / 24
9.091	200 / 22
10.000	200 / 20
11.111	200 / 18
12.500	200 / 16
14.286	200 / 14
16.667	200 / 12
20.000	200 / 10

Loading Rate (MHz)	Formula
25.000	200 / 8
33.333	200 / 6
50.000	200 / 4
100.000	200 / 2

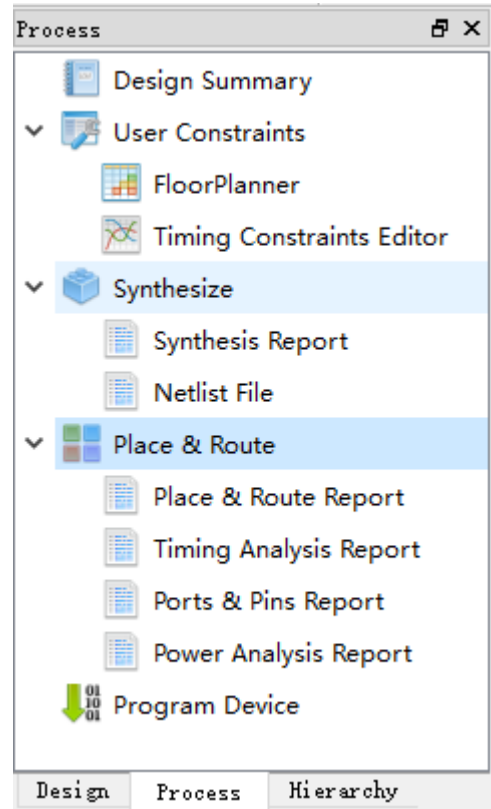
- **SPI Flash Address:** Specifies SPI Flash address. The SPI Flash address refers to the initial address to which the bitstream will be loaded for the next multiboot, and the default is 00000000. For further details, see [SUG502](#), Gowin Programmer User Guide.
- **User Code:** You can customize User Code, and the defined value will be reflected in the generated bitstream file, and the User Code will be checked when the bitstream file downloaded through the programmer. The default value is Default (00000000).
- **Bitstream Format:** Used to specify the bitstream file format, Text and Binary, and Binary by default. When the Text is selected, the *.fs file in plain text format is generated; when the Binary is selected, a bitstream file in *.fs, *.bin, and *.binx formats is generated. *.bin and *.binx are bitstream files in binary format, *.binx file contains header annotation information, and *.bin does not have header annotation information.

4.4 Manage a Project

The Process view provides the process of FPGA design flow, as shown in Figure 4-27. The Process View includes following operations.

- View design summary
- Start physical constraints editor
- Start timing constraints editor
- Run Synthesis
- View Synthesis report
- Run Place & Route
- View reports generated after Place & Route
- Start Programmer

Figure 4-27 Project Process View



4.4.1 Design Summary

A new project created, the software will analyze the project and provide a report of Design Summary, which will include the project file path, synthesis information and device information, as shown in Figure 4-28. There are three following ways to open the Design Summary:

- From the menu bar, select "Window > Design Summary".
- In the Process View, double-click "Design Summary".
- In the Process View, right-click "Design Summary", and select "Open".

Figure 4-28 Project Summary

General	
Project File:	D:\user-bak\Users\root\Desktop\8bit_counter\8bit_counter.gprj
Synthesis Tool:	GowinSynthesis

Target Device	
Part Number:	GW2AN-LV18XUG400C8/I7
Series:	GW2AN
Device:	GW2AN-18X
Package:	UBGA400
Speed Grade:	C8/I7
Core Voltage:	LV

4.4.2 User Constraints

User constraints provide quick access to open and create constraints files. User constraints include physical and timing constraints.

For the details, please refer to [SUG940](#), Gowin Design Timing Constraint User Guide, and [SUG935](#), Gowin Design Physical Constraints User Guide.

4.4.3 Synthesize

GowinSynthesis[®] is the synthesis tool developed by Gowin. It supports GOWINSEMI library files and their implementations. It supports System Verilog 2017, Verilog 2001, Verilog 95, VHDL 1993 and VHDL 2008.

Right-click "Synthesize" and select "Configuration" in the Project Design area to open the configuration dialog box, as shown in Figure 4-20.

Synthesize provides functions of running synthesis, setting synthesis parameters, and managing Netlist File and Synthesis Report. For the Synthesis Report, see [6.1 Synthesis Report](#).

Refer to the following steps to run Synthesize.

1. Configure synthesis, and you can refer to 4.3.3 Edit Project Configuration.
2. Run Synthesize
3. In the Process pane, double click "Synthesize" or right-click "Synthesize" and select "Run" to start synthesis of source files. If the synthesis is successful, the icon "✔" appears before Synthesize; if not, the icon "❗" appears.
4. After synthesis completed successfully, double click "Netlist Report", "Synthesis Report" or right-click and select "Open" to view the Netlist Report and synthesis report. The post-synthesis generated netlist file is *.vg, and synthesis report file is *_syn.rpt.html.

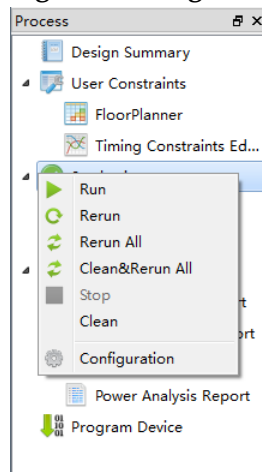
If the Synthesize icon is "🔵" before synthesis, double click "Netlist File", "Synthesis Report" or right click to select "Open" to synthesize first, and the netlist file or synthesis report can be opened after successful synthesis.

The right-click operations of Synthesize is as shown in Figure 4-29.

- Run: Only when the icon before Synthesize is "🔵", "❗", or "❓", you can select Run to start synthesis of source files.
- Rerun: No matter what Synthesize status is, you can select Rerun to restart synthesis of source files.
- Rerun All: If this option selected, regardless of the status of "Place & Route" and "Synthesize", the source file will be synthesized and placed & routed again

- Clean & Rerun All: Clean the gwsynthesis and pnr folders under the project folder impl, and synthesize and place & route the source files again.
- Stop: Stop Synthesize
- Clean: Clean the generated folder after synthesis (a folder generated by GowinSynthesis is gwsynthesis). Click it and a prompt will pop up.
- Configuration: Configure Synthesis parameters

Figure 4-29 Right-click Synthesize



4.4.4 Place & Route

Place and route provides the functions of running PnR, setting parameters, and managing the generated files.

Note!


Place & Route will be implemented after running Synthesize.

Refer to the following steps to run Place & Route.




1. Configure Place & Route, please refer to 4.3.3 Edit Project Configuration.
2. Run Place & Route, double-click "Place & Route", or right-click and select "Place & Route > Run " to generate bitstream files and related reports. If running successfully, the "✓" icon will appear before Place & Route. Otherwise, the "!" will appear;
3. After Place & Route has been run successfully, double-click on "View Post PnR Report" or right- Click and select "Open" to view the report.
4. You can view four kinds of reports: Place & Route Report, Timing Analysis Report, Ports & Pins Report, and Power Analysis Report. These reports can not be edited. See [6.2 Place & Route Report](#) , [6.3 Ports and Pins Report](#) , [6.4 Timing Report](#) , [6.5 Power Analysis Report](#) for the details.

Note!

- If the report is already opened and it is regenerated by running Place & Route again, a update prompt will pop up.

- Before running Place & Route, if the status icon before Place & Route is "  ", double click the report or right-click and select "Open" to run Place & Route first. The report will be opened after Place & Route runs successfully.

Right-click operations of Place & Route are as follows.

- Run: You can select "Run" to start Place & Route only when the icon before Place&Route is "  ", "  ", or "  ".
- Rerun: Regardless of the Place & Route status, you can select Rerun to rerun Place & Route.
- Rerun All: If this option selected, regardless of the status of "Place & Route" and "Synthesize", the source file will be Synthesize and placed & routed again.
- Clean & Rerun All: Clean the gwsynthesis and pnr folders under the project folder impl, and synthesize and place & route the source files again.
- Stop: Stop Place & Route
- Clean: Clean all the generated files after PnR; a prompt will pop up when you clicks this option. A Warning message will be reported if the deletion of a folder fails.
- Configuration: Configure Place & Route parameters.

4.4.5 Program Device

Bitstream files will be generated after Gowin Software has run placement and routing. Start Gowin FPGA programmer to download the bitstream files to the chip to realize user-required functions.

Note!

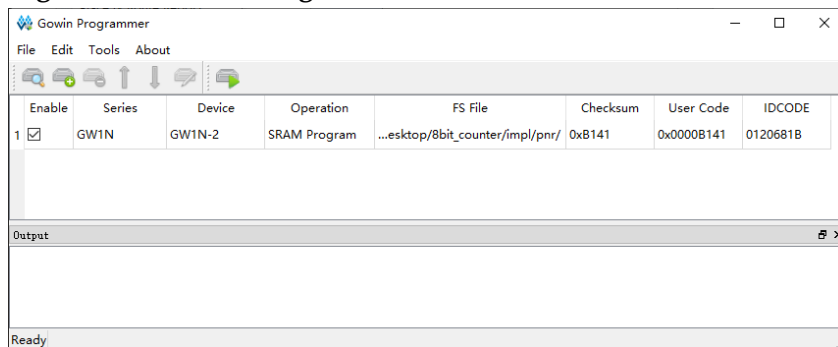
Program Device will be implemented after running Synthesize and Place & Route. If you do not run synthesize and Place & Route first, warnings will appear.

Double-click "Program Device" or right click and select "Run" to open Gowin FPGA Programmer, as shown in Figure 4-30.

Note!

The Programmer in the Linux installation package does not work with Linux Red Hat 5.10, only works with Red Hat 6 and above, and the Linux core version needs to be 2.18 and above.

Figure 4-30 Gowin Programmer



For the usage, please refer to [SUG502](#), Gowin Programmer User

Guide.

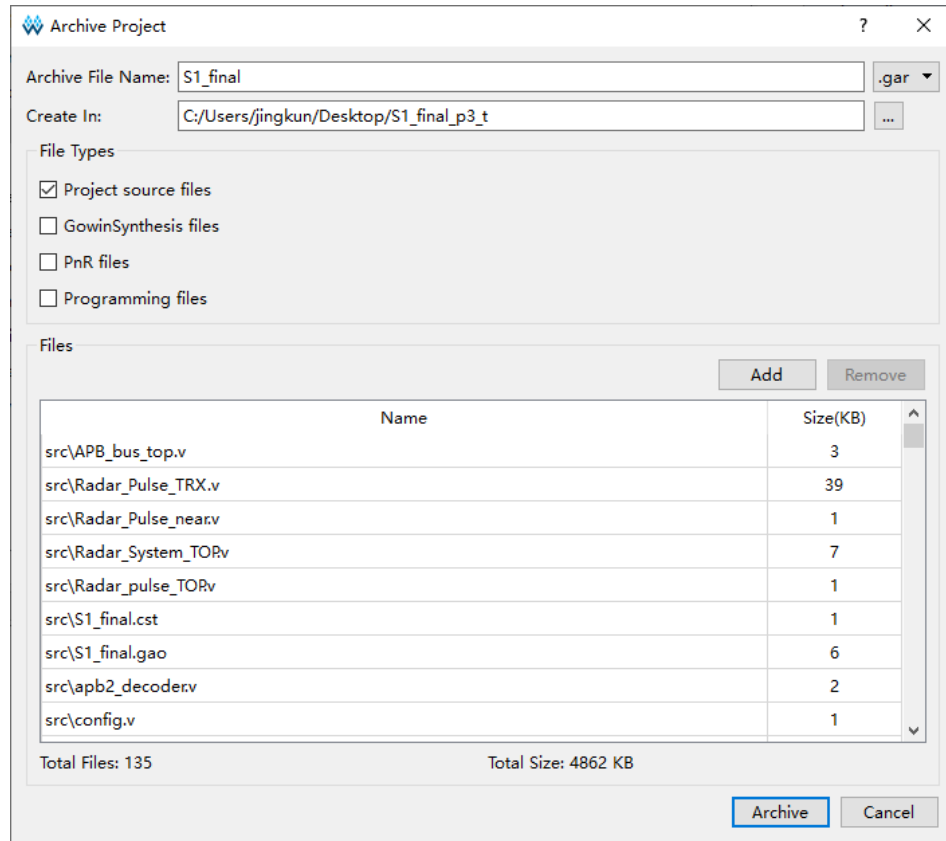
4.5 Archive and Restore a Project

Gowin Software can archive project and restore archived project. Use "Archive Project" and "Restore Archived Project" under "Project" in the menu bar to archive or restore archived project.

4.5.1 Archive a Project

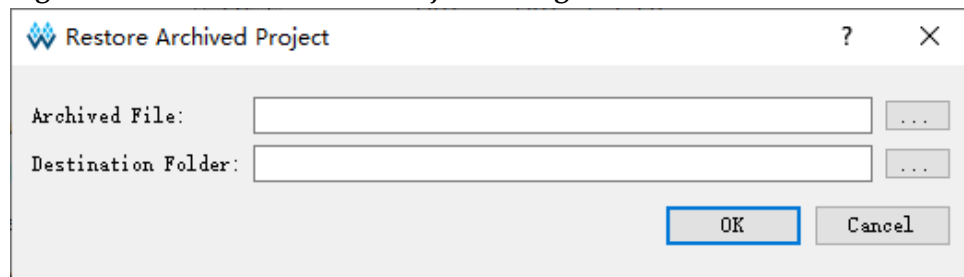
A dialog box will pop up when you click "Project > Archive Project", as shown in Figure 4-31.

- Archive File Name is the archived file name. The default name is the same as the current archived project name with extension .gar.
- Create In is the path for the archived file, and the default is the current project path.
- The File Types include Project source files (checked by default), GowinSynthesis files, PnR files and Programming files.
 - Project source files: Includes all the files under the path /src where the project is located.
 - GowinSynthesis files: Includes project files (*.prj), netlist files (*.vg), synthesis reports (*_syn.rpt.html), resource statistics files (*_syn_rsc.xml) generated synthesis under the path /impl/gwsynthesis where the project is located.
 - PnR files: Includes the files generated by PnR under the path /impl/pnr where the project is located.
 - Programming files: Includes the bitstream file *.fs, *.bin and *.binx generated by PnR under the path /impl/pnr where the project is located.
- When a file type is checked, the source file, path and size of the current project are displayed below.
- Add and Remove can be used to add and remove archived files.
- After clicking Archive, a prompt box will pop up if the files in the project are not saved.
- After archiving, a prompt will pop up, indicating the success or failure of the archiving.
- When the archiving is completed, two files will be generated under the "Create In" path: the archived project *.gar and the archived file *.garlog. The file with .gar suffix compresses and stores all the archived files. The log file with *.garlog suffix is used for checking which files are archived and whether the archiving is successful.

Figure 4-31 Archive Project Dialog Box

4.5.2 Restore Archived Project

Restore Archived Project dialog will pop up when you clicks Project in the menu bar, as shown in Figure 4-32 .

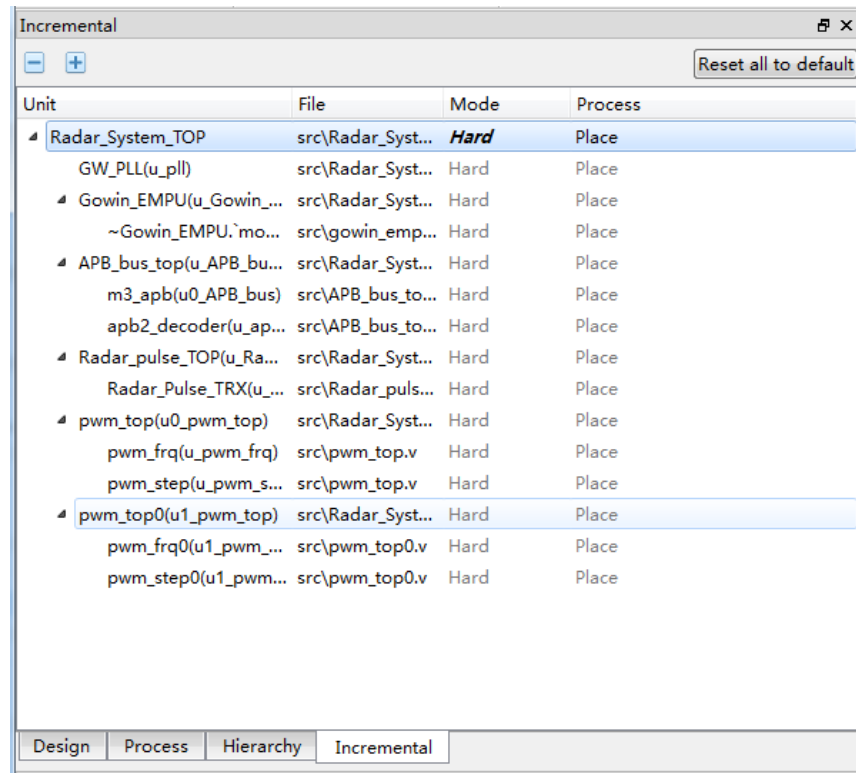
Figure 4-32 Restore Archived Project Dialog Box

Click the button on the right side of Archived File to select the archived file to restore. After selecting, "Destination Folder" is automatically updated to the path where the archive file is. Click "OK" and a dialog box will pop up.

4.6 Set Incremental

Gowin Software incremental currently can retain the previous placement to reduce runtime. Click "Project > Set Incremental" to open GUI, as shown in Figure 4-33.

Figure 4-33 Set Incremental View



The "Unit" displays the module hierarchy of the design file. The "File" displays the files defined by the module. The "Mode" displays incremental mode, and the "Process" specifies a valid process. Clicking "-" and "+" in the upper left corner can collapse and expand all levels in the design. Click "Reset all to default" in the upper right corner to reset all configurations to the default.

The incremental mode can be configured by double-clicking and currently the following three modes are supported.


- Unset: Unset an unspecified incremental.
- Ignore: Ignore the previous synthesis and PnR and re-run.
- Hard: Use the previous placement result.

The Process column currently only supports Place, which means that the synthesis and place remain, and only set route incremental.

The default incremental mode is Ignore. When Unset or Ignore is selected, the Process column will be empty. When Hard is selected, the Process column displays Place. Currently, only the Mode setting for the top module is supported, and the corresponding value of the sub module will be updated synchronously with the configuration of the top module.

4.7 Exit Software

There are two ways to exit Gowin Software.

1. Select "File > Exit" from the File menu.
2. Click the " " icon on the upper right of the IDE.

Note!

- If files are not saved, IDE will prompt you to save the files first.
- Save, Save All, and Save As...are only available for text editing.
- Project configuration modification and project files addition and deletion will not be saved to project configuration files in time; they will be saved automatically when you close the software.
- If the software is running, you cannot exit software by clicking.

5 Tools Integrated in Gowin Software

5.1 Physical Constraints Editor

Gowin FloorPlanner is designed in-house by Gowin, and it supports reading and editing the attributes and locations of I/O, Primitive, Block (BSRAM and DSP), and Group, etc. It also supports the generation of new placement and constraints files according to your configuration. These files define the I/O attributes, primitives and locations, etc. Gowin FloorPlanner, supporting Gowin all FPGA products, provides an editing way to improve design efficiency, and it also supports timing optimization.

FloorPlanner can be started using two methods.

1. If no FPGA project is created, you can select "Tools > FloorPlanner" directly from the menu bar. You will need to add netlist files and devices information by selecting "File > New".
2. If an FPGA project is already created, run "Synthesize", and then double-click "FloorPlanner" directly in the Process View. The Floorplanner will then load the project files directly. The FloorPlanner includes Summary, Netlist, Chip Array, Package View, as shown in Figure 5-1 and Figure 5-2.

Note!

- For more details, see SUG935, Gowin Design Physical Constraints Guide
- The FloorPlanner also supports timing optimization.

Figure 5-1 Chip Array View

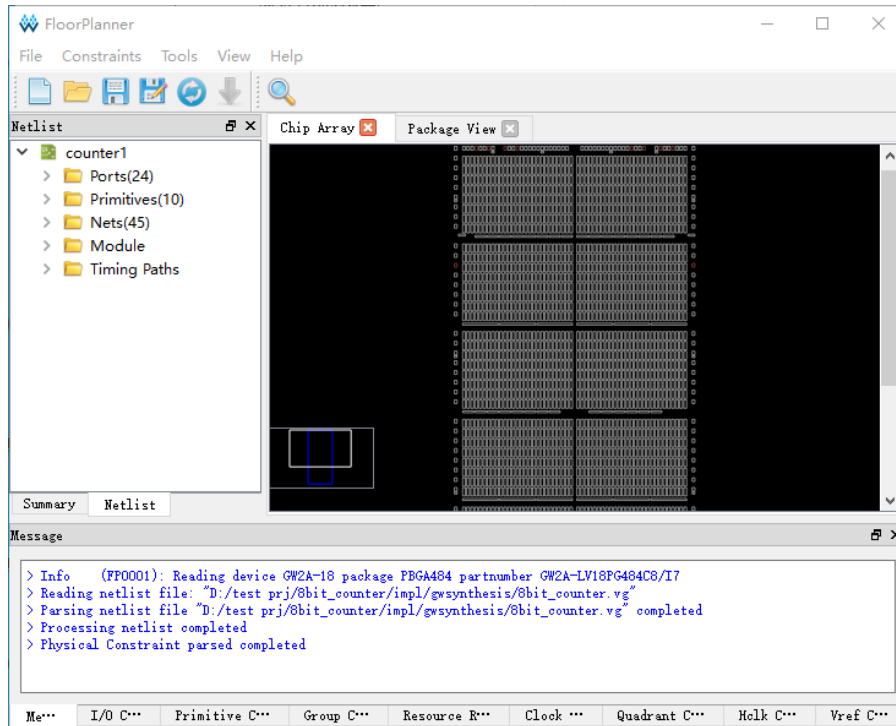
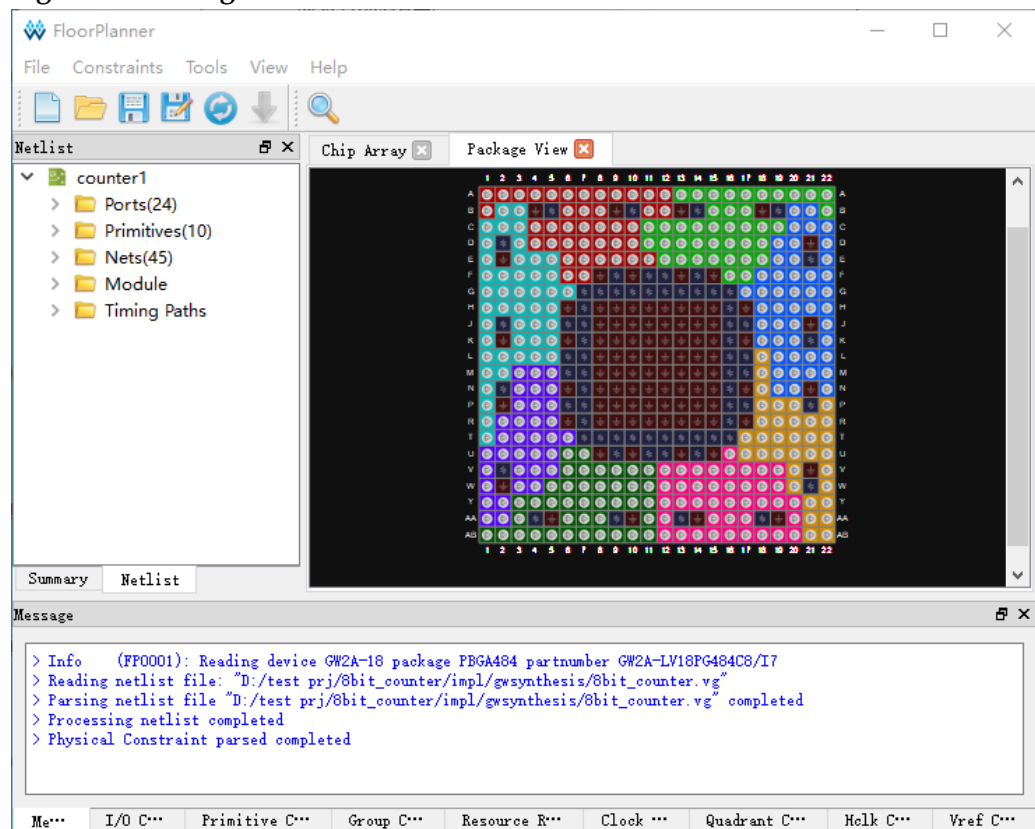


Figure 5-2 Package View



5.2 Timing Constraint Editor

The Gowin Timing Constraints Editor is designed in-house by Gowin, and supports multiple timing constraints commands, including clock constraints, I/O constraints, path constraints, and clock report editing. The Timing Constraints Editor allows an easy and quick timing constraint editing for Gowin all FPGA products.

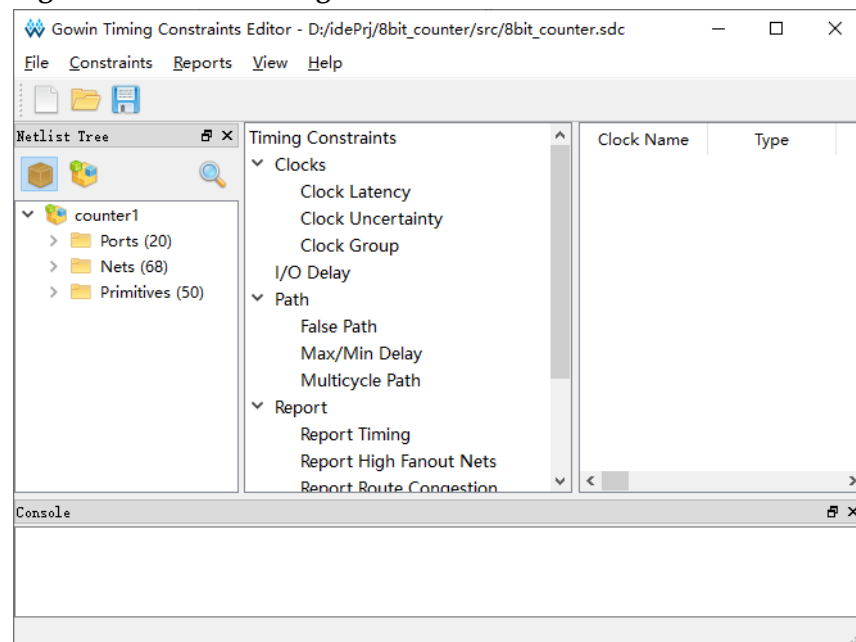
Timing Constraints Editor can be started using two methods:

1. If no FPGA project is created, you can select "Tools > Timing Constraints Editor" from the menu bar. Add netlist files by selecting "File > New".
2. If an FPGA project is already created, Run "Synthesize", double-click "Timing Constraints Editor", and the Timing Constraints Editor will load project files directly, as shown in Figure 5-3.

Note!

For the details, see [SUG940](#), Gowin Design Timing Constraint User Guide.

Figure 5-3 Create Timing Constraints



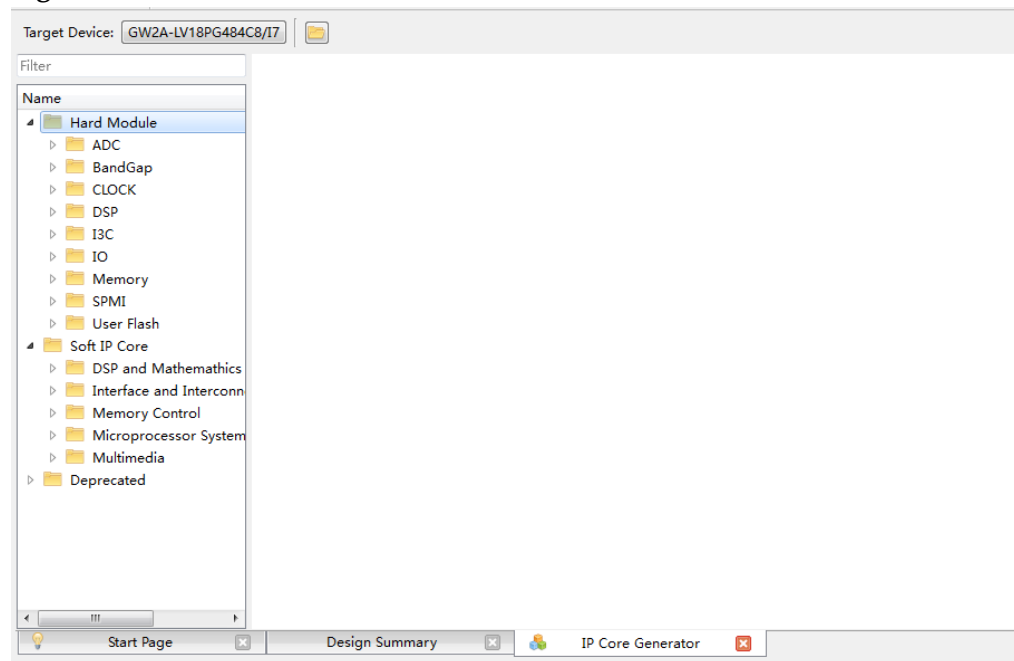
5.3 IP Core Generator

The IP Core Generator in Gowin Software is mainly used to generate hard and soft IPs, which you can call to implement the required functions. As shown in Figure 5-4, its main functions are as follows.

- Supports Soft IP core, Hard module information preview
- Supports customized Soft IP core and Hard module.
- Supports Hard module instance generation.
- Can save configuration automatically.
- Supports IP generation code language selection.

- Some Soft IP can generate incentive file automatically.
- Can display available IPs by selecting device.

Figure 5-4 IP Core Generator



Start the IP Core Generator by selecting "IP Core Generator" from the Tools menu. For the details, you can see following manuals.

- For the details of ADC, BANDGAP, I3C and SPMI, you can see [SUG283](#), Gowin Primitives User Guide.
- For the details of CLOCK, you can see [UG286](#), Gowin Clock User Guide.
- For the details of DSP, you can see [UG287](#), Gowin Digital Signal Processing User Guide.
- For the details of IO Logic, you can see [UG289](#), Gowin Programmable IO (GPIO) User Guide.
- For the details of BSRAM & SSRAM, you can see [UG285](#), Gowin BSRAM & SSRAM User Guide.
- For the details of User Flash, you can see [UG295](#), Gowin User Flash User Guide.
- For the soft IPs reference design, you can click this [link](#).

Note!

The grayed out Hard Module or Soft IP Core is not supported by the current device.

5.4 Gowin Analyzer Oscilloscope

The Gowin Analyzer Oscilloscope (GAO) is a digital signal analyzer that is designed in-house by Gowin. It helps you to analyze signal timing in design more easily, and quickly perform system analysis and fault locating, thereby improving design efficiency.

GAO supports RTL-level signal capture and netlist-level signal capture after synthesis, and provides standard version (Standard) and simplified version (Lite). Standard GAO can support up to 16 AOs, each of which can be configured with one or more trigger ports, supporting multi-level static or dynamic trigger expressions. Lite GAO is easy to configure, and you do not need to set trigger conditions, and it also can capture the initial value of the signal, which is convenient for you to analyze the state of power-on. After signal capture, the waveform can be exported, supporting *.csv, *.vcd and *.prn file formats. *.csv and *.prn files can be directly used in matlab and other third-party simulation tools, and *.vcd file can be directly used in ModelSim.

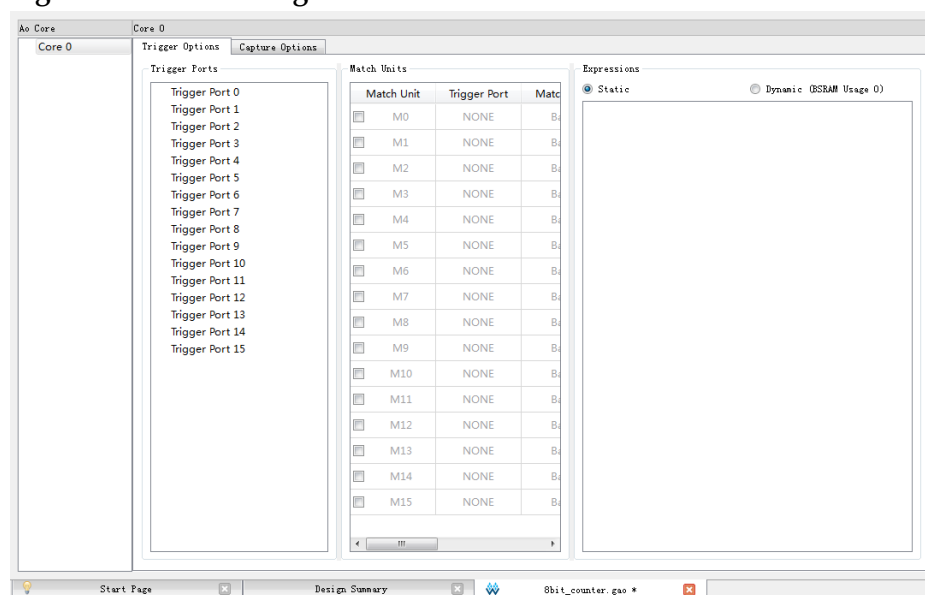
Note!

Matlab and ModelSim tools require a third-party license.

The GAO includes the Gowin GAO configuration and the Gowin Analyzer Oscilloscope. Gowin GAO configuration is mainly used to insert position information into the design, which is predominantly based on the sampling clock, trigger unit, and trigger expression; Gowin Analyzer Oscilloscope connects software and target hardware through the JTAG interface, and visually displays the data of the sampled signal set by GAO Config File with the waveform.

Before starting GAO configuration, create the GAO config file in the Project View to open the GAO configuration view, taking standard version as an example, as shown in Figure 5-5.

Figure 5-5 GAO Config File View

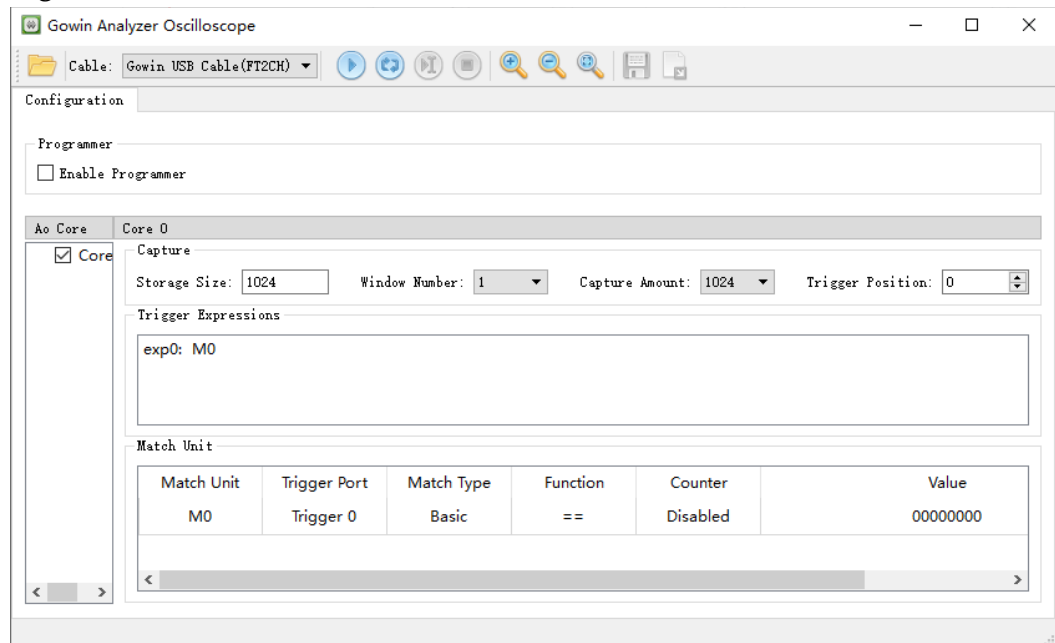


After the configuration file is created, select "Tools > Gowin Analyzer Oscilloscope" from the menu bar to open the Gowin Analyzer Oscilloscope, as shown in Figure 5-6.

Note!

For the details, see [SUG114](#), Gowin Analyzer Oscilloscope User Guide.

Figure 5-6 GAO View



5.5 Gowin Power Analyzer

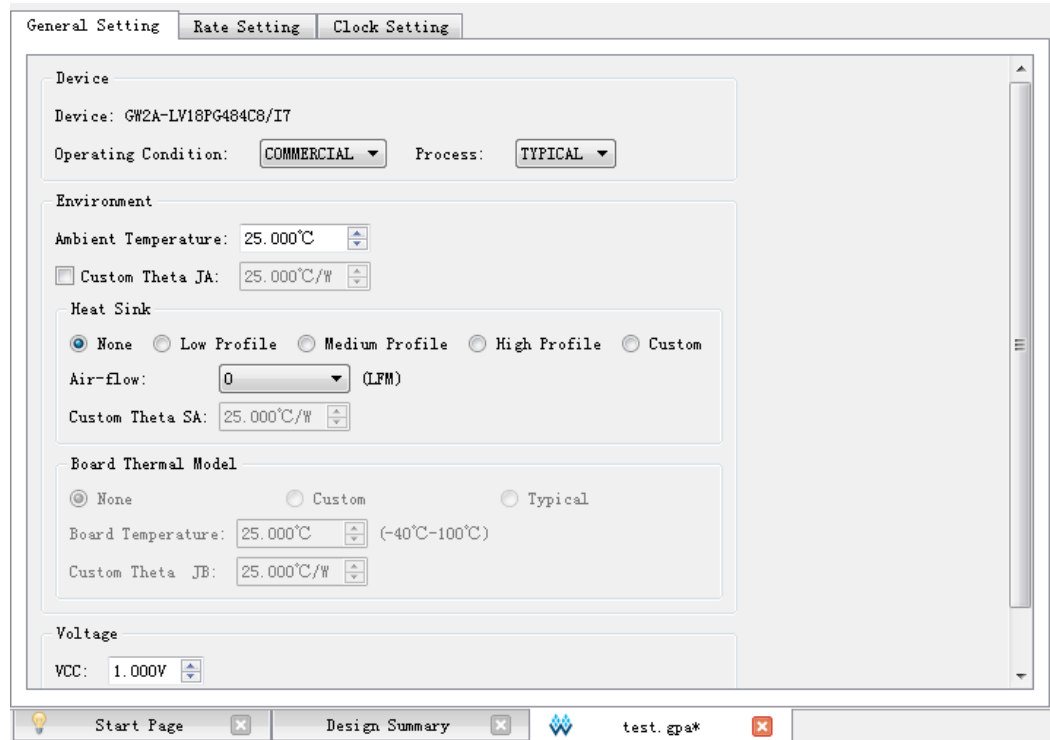
Gowin Power Analyzer (GPA) helps to analyze the power consumption of your design and provides many configuration options. You can configure the parameters according to the actual design. GPA automatically estimates the power consumption and generates a power consumption analysis report according to the parameters.

Based on the new configuration file (.gpa), follow the below steps to start the GPA.

1. In the Design area, select "File> New..." to open a "New" dialog box.
2. Select "GPA Config File" and type a Name in the pop-up dialog box.
3. Click "OK", and the new GPA config file will be displayed in the Project Design View.
4. Double click on the file name to open the GPA Config view, as shown in Figure 5-7.

Note!

For the details, see [SUG282](#), Gowin Power Analysis User Guide.

Figure 5-7 GPA Config File View

5.6 Block Memory Initialization File Editor

The Memory Initialization File is an ASCII file with an .mi suffix. You can generate the corresponding Initialization File according to your design to specify the initial value for the memory of each address. The Memory Initialization File editor can be used to open and edit the existed .mi file.

Each line in the Memory Initialization File correlates with one memory. The number of lines is the number of memories and also the memory address depth. The number of columns represents each memory bit; that is, the memory data width. The address decreases from top to bottom with the most significant bit first for each line.

Gowin block memory initialization file is based on .mi file. For the details, see [UG285](#), Gowin BSRAM & SSRAM User Guide. The steps are as follows:

1. In the Design area, select "File> New..." to open a "New" dialog box.
2. Select "Memory Initialization File", as shown in Figure 5-8. Click "OK" and type the initialization file name in the pop-up "New File" dialog box, and then click "OK". The Initialization File Configuration View is as shown in Figure 5-9.
3. Start the file initialization view as shown in Figure 5-10. Type the initial value on the left side and configure the initialization file format and depth/width and view on the right side.
4. On the right side, configure the depth and width for the initialization file and the format for the address and initial values in the left table.

- The depth and width values should be same as the Block Memory or Shadow Memory address depth and data width set in the IP Core Generator. If the address depth and data width in the initialization file are greater than the values set in the IP Core Generator, the IP Core Generator will prompt an error message. If the depth and width values are less than the BSRAM address depth and data width set in the IP Core Generator, the value of the unassigned address will be initialized to 0 by default. Click "Update" after configuration.
 - The display format of the addresses and values on the left in the table can be configured as binary, hexadecimal, and address-hexadecimal, etc.
5. Type the initial value and set the view in the left table.
 - Right-click the table header to configure the number of columns, which can be configured as 1, 8, or 16, as shown in Figure 5-11.
 - Double-click and type the initial value, or right-click to set the value. "Fill with 0" means the initial value is 0, "Fill with 1" means each bit of the initial value is 1, and "Custom Fill" means you can type the value according to your needs; you can also set initial values in batches, as shown in Figure 5-12.
 6. Save the file.

Figure 5-8 New Dialog Box

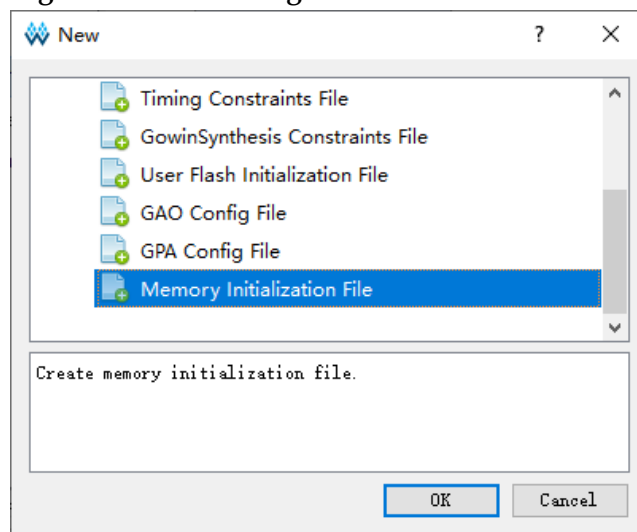


Figure 5-9 New File Dialog Box

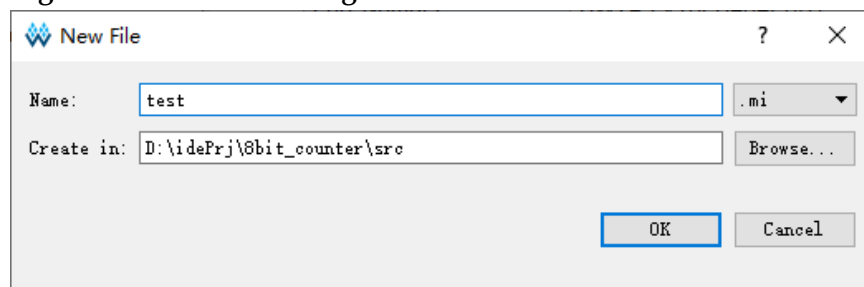


Figure 5-10 Initialization File Configuration View

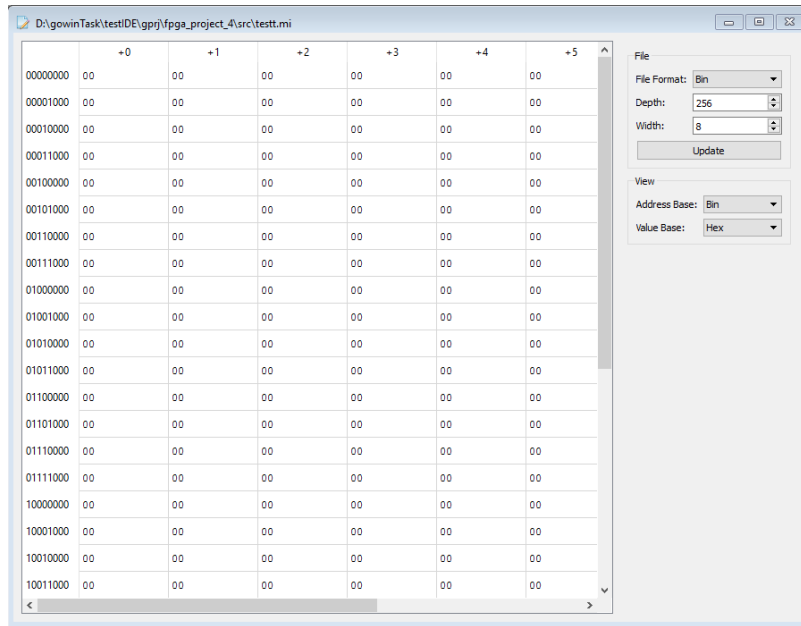


Figure 5-11 Column Setting

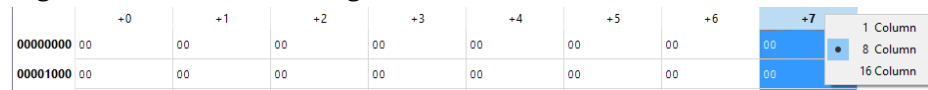
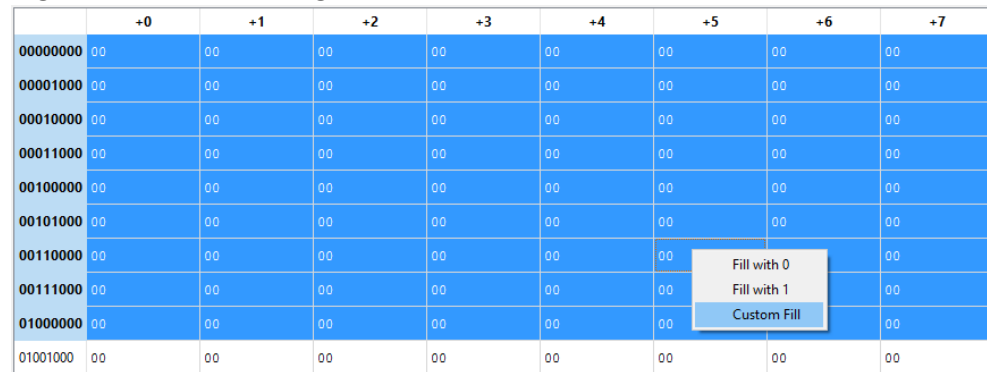


Figure 5-12 Batch Setting



5.7 User Flash Initialization File Editor

User Flash Initialization file is an ASCII file with an .fi suffix. You can generate the corresponding Initialization File according to your design to specify the initial value for the User Flash of each address. The User Flash Initialization File editor can be used to open and edit the existed .fi file.

The name of User Flash initialization file is *.fi(file_name.fi). Each line in the Memory Initialization File correlates with one memory. The number of lines is the number of memories that needs to be initialized. The contents in the header bracket represent the ordinate address and the abscissa address respectively, separated by a semicolon. The contents after the brackets in each line represent the data initialized by the memory, and the

data supports binary and hexadecimal, MSB first. The following are examples of the .fi file format.

5.7.1 Bin File

```
Bin file is a text file that consists of the 0 and 1 binary numbers.
//Copyright (C)2014-2021 Gowin Semiconductor Corporation.
//All rights reserved.
//File Title: User Flash Initialization File
//GOWIN Version: V1.9.8.01
//Part Number: GW1N-LV4LQ144C6/I5
//Device-package: GW1N-4-LQFP144
//Flash Type: FLASH256K
//File Format: Bin
//Created Time: 2021-10-11 17:24:22
[0:0] 000000010001000000001000000000000
[2:1] 00000010011101000000001001110100
[4:2] 000100010000000000001000000000001
```

5.7.2 Hex File

The Hex file is similar to the Bin file. It consists of hexadecimal numbers 0~F.

```
//Copyright (C)2014-2021 Gowin Semiconductor Corporation.
//All rights reserved.
//File Title: User Flash Initialization File
//GOWIN Version: V1.9.8.01
//Part Number: GW1N-LV4LQ144C6/I5
//Device-package: GW1N-4-LQFP144
//Flash Type: FLASH256K
//File Format: Hex
//Created Time: 2021-10-12 08:48:03
[0:0] 01101000
[2:1] 02740274
[4:2] 11001001
[5:1] 564a2bc3
[8:1] eadbe012
```

Based on the new configuration file (. fi), and you can follow the below steps to use the initialization file editor.

1. In the Design area, select "File> New..." to open a "New" dialog box.
2. Select "User Flash Initialization File", as shown in Figure 5-13. Click "OK" and type the initialization file name in the pop-up "New File" dialog box, and then click "OK", as shown in Figure 5-14. The devices supported by User Flash Initialization File Editor are the same as the devices supported by User Flash Primitives. If the device you selected does not support User Flash, "Current device do not support flash" will pop up at the bottom of "New File" Dialog box after you click "OK".

Figure 5-13 New Dialog Box

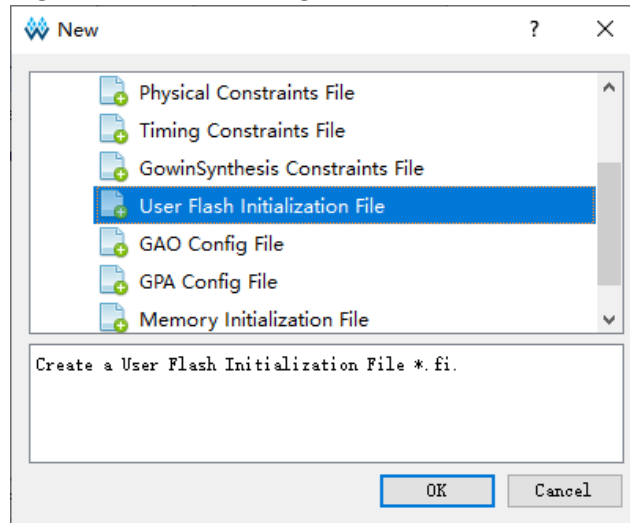
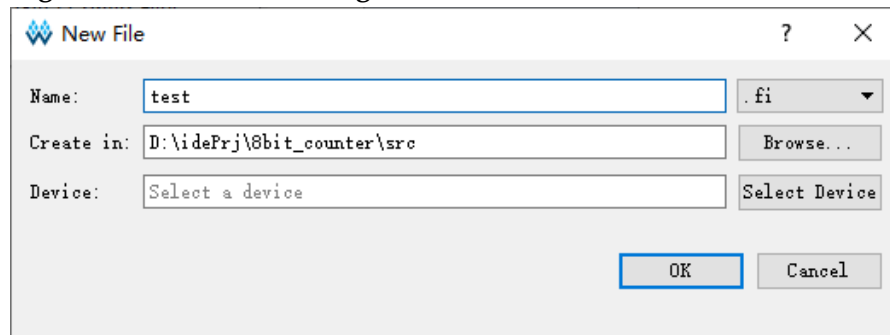
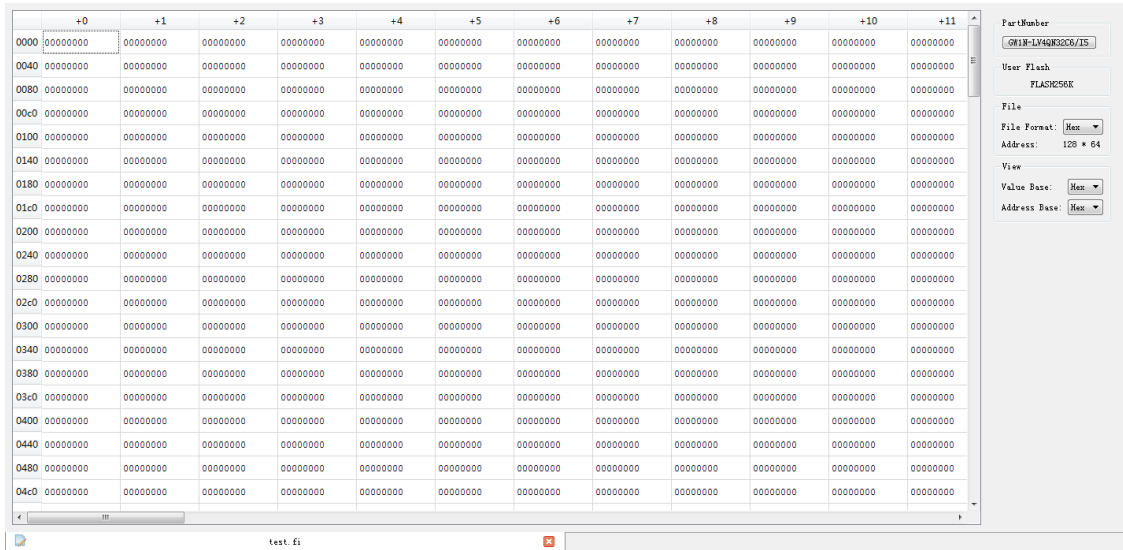


Figure 5-14 New File Dialog Box



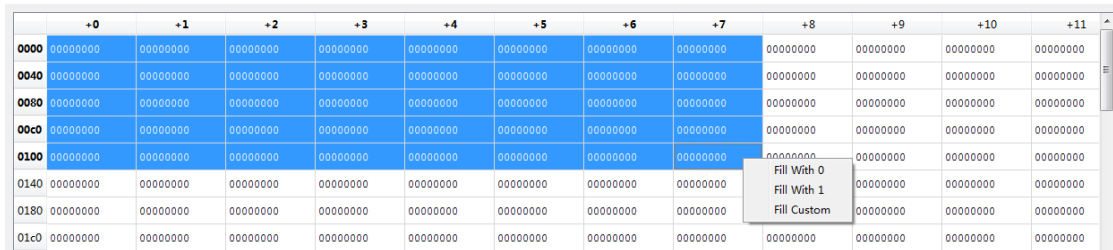
3. Start the file initialization view as shown in Figure 5-15. Enter the initial value on the left side and configure the initialization file format and view on the right side; Part Number and User Flash also displayed on the right.

Figure 5-15 Initialization File Configuration View



4. On the right side, configure Part Number, file format, address and value.
 - Click "Part Number", then "Select Device" dialog box will pop up; you can select the other part number.
 - The format of address and value can be configured as binary, octal, decimal, hexadecimal, etc.
5. Type the initial value and set the view. Double-click and type the initial value, or right-click to set the value. "Fill with 0" means the initial value is 0, "Fill with 1" means each bit of the initial value is 1, and "Custom" means you can type the value according to your needs; you can also set initial values in batches, as shown in Figure 5-16.

Figure 5-16 Batch Setting



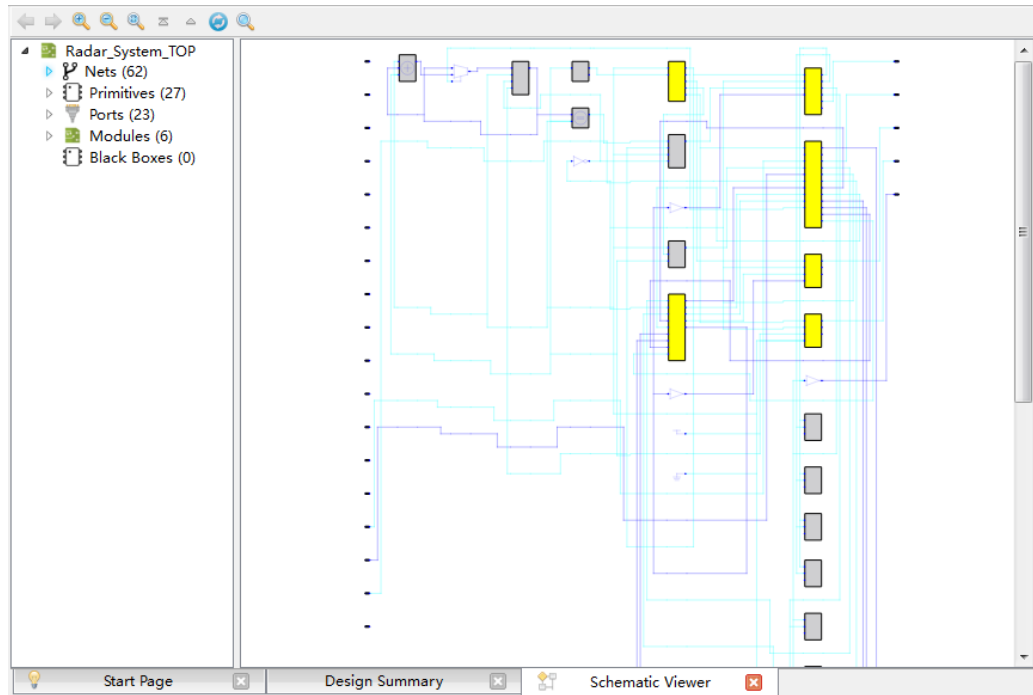
6. Save the file.










5.8 Schematic Viewer

You can understand the design logic by Schematic Viewer, which is helpful to the later modification. Schematic Viewer uses common component symbols to build circuits, including adders, multipliers, registers, and gates, non-gates, and inverters, etc.

You can click "Tools > Schematic Viewer" to open GUI, as shown in Figure 5-17.

Figure 5-17 Schematic Viewer



Schematic Viewer displays backward "", forward "", zoom in "", zoom out "", zoom "", top view "", upper level view "", reload "", and search "". The design hierarchy is displayed on the left side, including modules, ports, nets, primitives, and black boxes.

Note!

For the details, you can see [SUG755](#), Gowin HDL Schematic Viewer User Guide.

6 Description of Output Files

In the process of FPGA design, in addition to bitstream file, Gowin Software can also generate reports for reference. They are synthesis, place & route, ports, timing and power reports. In addition, you can right-click Place & Route to modify the configuration to generate pins constraints, timing simulation files, etc.

6.1 Synthesis Report

GowinSynthesis® will generate synthesis reports and netlist files after synthesis.

The report named *_syn.rpt.html is generated, including Synthesis Message, Design Details, Resource, and Timing, as shown in Figure 6-1.

Figure 6-1 GowinSynthesis Report

Synthesis Details					
<ul style="list-style-type: none"> • Synthesis Messages • Synthesis Details • Resource <ul style="list-style-type: none"> • Resource Usage Summary • Resource Utilization Summary • Timing <ul style="list-style-type: none"> • Clock Summary • Max Frequency Summary • Detail Timing Paths Informations 	<table border="1"> <thead> <tr> <th>Top Level Module</th> <th>counter1</th> </tr> </thead> <tbody> <tr> <td>Synthesis Process</td> <td> Running parser: CPU time = 0h 0m 0.109s, Elapsed time = 0h 0m 0.121s, Peak memory usage = 74.734MB Running netlist conversion: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 0MB Running device independent optimization: Optimizing Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Optimizing Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Optimizing Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Running inference: Inferring Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 3: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Running technical mapping: Tech-Mapping Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 3: CPU time = 0h 0m 0.046s, Elapsed time = 0h 0m 0.095s, Peak memory usage = 87.988MB Tech-Mapping Phase 4: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 87.988MB </td> </tr> </tbody> </table>	Top Level Module	counter1	Synthesis Process	Running parser: CPU time = 0h 0m 0.109s, Elapsed time = 0h 0m 0.121s, Peak memory usage = 74.734MB Running netlist conversion: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 0MB Running device independent optimization: Optimizing Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Optimizing Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Optimizing Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Running inference: Inferring Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 3: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Running technical mapping: Tech-Mapping Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 3: CPU time = 0h 0m 0.046s, Elapsed time = 0h 0m 0.095s, Peak memory usage = 87.988MB Tech-Mapping Phase 4: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 87.988MB
Top Level Module	counter1				
Synthesis Process	Running parser: CPU time = 0h 0m 0.109s, Elapsed time = 0h 0m 0.121s, Peak memory usage = 74.734MB Running netlist conversion: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 0MB Running device independent optimization: Optimizing Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Optimizing Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Optimizing Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Running inference: Inferring Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Inferring Phase 3: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Running technical mapping: Tech-Mapping Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 1: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 2: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 74.734MB Tech-Mapping Phase 3: CPU time = 0h 0m 0.046s, Elapsed time = 0h 0m 0.095s, Peak memory usage = 87.988MB Tech-Mapping Phase 4: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s, Peak memory usage = 87.988MB				

The details are as follows.

- Synthesis Message: Includes design file, GowinSynthesis version, running time, etc.

- Design Details: Includes top module of the design file, the synthesis running time and CPU running time, as well as the memory peak at each stage, and total CPU running time as well as memory peak.
- Resource: Includes resource statistics and device utilization statistics.
- Timing: Includes Clock Summary, Max Frequency Summary, Detail Timing Paths Informations.

6.2 Place & Route Report

The Place & Route Report describes the resource, memory consumption, time consumption, etc. occupied by the user design, with the suffix .rpt.html, and you can check *.rpt.html file for further details.

Double-click "Place & Route Report" in the Process View to open the Place & Route report, as shown in Figure 6-2.

Figure 6-2 Place & Route Report

The screenshot displays the Place & Route Report interface. On the left, there is a navigation menu with the following items:

- PnR Messages
- PnR Details
- Resource
 - Resource Usage Summary
 - I/O Bank Usage Summary
 - Global Clock Usage Summary
 - Global Clock Signals
 - Pinout by Port Name
 - All Package Pins

The main content area is divided into two sections:

PnR Details

Place & Route Process	Running placement: Placement Phase 0: CPU time = 0h 0m 0.004s, Elapsed time = 0h Placement Phase 1: CPU time = 0h 0m 0.263s, Elapsed time = 0h Placement Phase 2: CPU time = 0h 0m 0.002s, Elapsed time = 0h Placement Phase 3: CPU time = 0h 0m 0.8s, Elapsed time = 0h 0r Total Placement: CPU time = 0h 0m 1s, Elapsed time = 0h 0m 1s Running routing: Routing Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0s Routing Phase 1: CPU time = 0h 0m 0.189s, Elapsed time = 0h 0m Routing Phase 2: CPU time = 0h 0m 0.082s, Elapsed time = 0h 0m Total Routing: CPU time = 0h 0m 0.271s, Elapsed time = 0h 0m 0. Generate output files: CPU time = 0h 0m 2s, Elapsed time = 0h 0m 2s
Total Time and Memory Usage	CPU time = 0h 0m 3s, Elapsed time = 0h 0m 3s, Peak memory usag

Resource

Resource Usage Summary:

Resource	Usage	Utilization
Logic	10/20736	1%
--LUT,ALU,ROM16	10(3 LUT, 7 ALU, 0 ROM16)	-
--SSRAM(RAM16)	0	-
Register	8/16683	1%
--Logic Register as Latch	0/15552	0%

The details are as follows.

- PnR Messages: Includes report name, path and name of design, physical constraints file, timing constraints file, software version, device information, report creation time and declaration.
- PnR Details:
 - The time used in each stage of place and the total time of place, including the time of GAO place if there is GAO in the project.
 - The time used in each stage of route and the total time of route, including the time of GAO route if there is GAO in the project.
 - The time used to generate the output file.
- Resource:
 - Resource Usage Summary: Device resources utilization in user design.

- I/O BANK0 Usage Summary: I/O BANK0 in user design
- Global Clock Usage Summary: Global clock used
- Global Clock Signals: Clock signals used in the user design
- Pinout by Port Name: Pinout in the user design
- All Package Pins: Details of all the pins in the device package

If the project has a GAO, it also includes the GAO Resource Usage Summary.

6.3 Ports and Pins Report

The Ports and Pins Report is the ports and pins files after placement. It includes ports type, attributes, and locations, etc. The generated file is saved with the .pin.html suffix, and you can view .html file for details.

Double-click "Ports & Pins Report" in the Process View to open the report , as shown in Figure 6-3.

Figure 6-3 Ports & Pins Report

Pin Details

- Pin Messages
- Pin Details
 - Pinout by Port Name
 - All Package Pins

Pinout by Port Name:

Port Name	Diff Pair	Loc./Bank	Constraint	Dir.	Site	IO Type	Drive	Pull Mode	PCI
clk		L1/7	N	in	IOL25[A]	LVC MOS18	OFF	DOWN	OFF
cout[0]		M2/7	N	out	IOL25[B]	LVC MOS18	8	NONE	OFF
cout[1]		F6/8	N	out	IOL3[A]	LVC MOS18	8	NONE	OFF
cout[2]		G7/8	N	out	IOL3[B]	LVC MOS18	8	NONE	OFF
cout[3]		D3/8	N	out	IOL2[A]	LVC MOS18	8	NONE	OFF
cout[4]		D4/8	N	out	IOL2[B]	LVC MOS18	8	NONE	OFF
cout[5]		A2/0	N	out	IOT2[B]	LVC MOS18	8	NONE	OFF
cout[6]		E6/0	N	out	IOT3[A]	LVC MOS18	8	NONE	OFF
cout[7]		F5/8	N	out	IOL4[B]	LVC MOS18	8	NONE	OFF

All Package Pins:

Loc./Bank	Signal	Dir.	Site	IO Type	Drive	Pull Mode	PCI Clamp	Hysteresis	Open Drain
B1/0	-	out	IOT2[A]	LVC MOS18	8	NONE	OFF	OFF	ON
A2/0	cout[5]	out	IOT2[B]	LVC MOS18	8	NONE	OFF	OFF	OFF
E6/0	cout[6]	out	IOT3[A]	LVC MOS18	8	NONE	OFF	OFF	OFF
F7/0	-	out	IOT3[B]	LVC MOS18	8	NONE	OFF	OFF	ON
B2/0	-	out	IOT4[A]	LVC MOS18	8	NONE	OFF	OFF	ON
A3/0	-	out	IOT4[B]	LVC MOS18	8	NONE	OFF	OFF	ON

The details are as follows:

- Pin Messages: Includes report name, path and name of design, physical constraints file, timing constraints file, software version, device information, report creation time and declaration.
- Pin Details:
 - Pinout by Port Name: Pinout in the user design
 - All Package Pins: Details of all the pins in the device package

6.4 Timing Report

The timing report performs a thorough analysis of the timing model in the circuit netlist, calculates the timing path delays in the circuit, and determines whether they are met the requirements. The Timing report includes setup check, holdup check, restoring and removal time check, Min. clock pulse check, max. fanout path, Place & Route congestion report, etc. by default, and provides the Max. frequency report.

Double-click "Timing Analysis Report" in the Process View to open the timing analysis report for the project, as shown in Figure 6-4.

Note!

For the details, see [SUG940](#), Gowin Design Timing Constraints User Guide.

Figure 6-4 Timing Report

The screenshot shows the Timing Report interface. On the left is a navigation tree with the following items:

- Timing Messages
 - Timing Summaries
 - STA Tool Run Summary
 - Clock Summary
 - Max Frequency Summary
 - Total Negative Slack Summary
 - Timing Details
 - Path Slacks Table
 - Setup Paths Table
 - Hold Paths Table
 - Recovery Paths Table
 - Removal Paths Table
 - Minimum Pulse Width Table
 - Timing Report By Analysis Type
 - Setup Analysis Report
 - Hold Analysis Report
 - Recovery Analysis Report
 - Removal Analysis Report
 - Minimum Pulse Width Report
 - High Fanout Nets Report

The main content area is titled "Timing Summaries" and contains the following sections:

STA Tool Run Summary:

Setup Delay Model	Slow 1.14V 85C
Hold Delay Model	Fast 1.26V 0C
Numbers of Paths Analyzed	8
Numbers of Endpoints Analyzed	8
Numbers of Falling Endpoints	2
Numbers of Setup Violated Endpoints	0
Numbers of Hold Violated Endpoints	0

Clock Summary:

Clock Name	Type	Period	Frequency(MHz)	Rise	Fall	Source	Master	Objects
clk0	Base	20.000	50.000	0.000	10.000			clk0_ibuf/1
clk1	Base	20.000	50.000	0.000	10.000			clk1_ibuf/1

Max Frequency Summary:

NO.	Clock Name	Constraint	Actual Fmax	Logic Level	Entity
1	clk0	50.000(MHz)	437.197(MHz)	1	TOP
2	clk1	50.000(MHz)	525.803(MHz)	1	TOP

6.5 Power Analysis Report

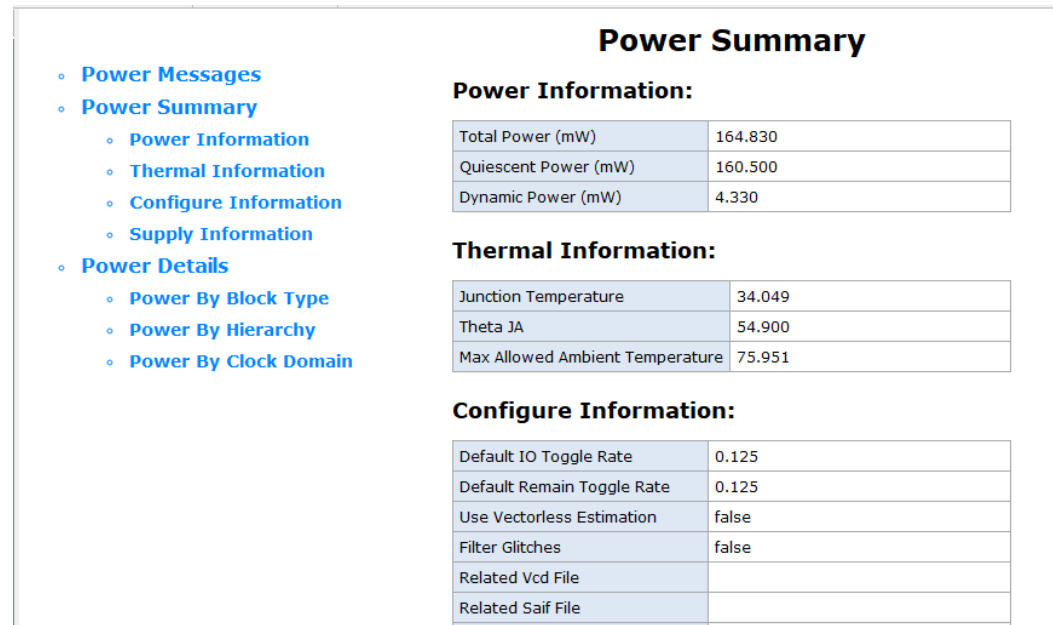
The Power Analysis Report mainly includes the power consumption estimation for your design. It is designed to help you evaluate the basic power consumption of your design.

Double-click "Power Analysis Report" in the Process View to open the analysis report, as shown in Figure 6-5.

Note!

For the details, see [SUG282](#), Gowin Power Analyzer User Guide

Figure 6-5 Power Analysis Report



7 Simulation Files

Gowin Software provides input files for simulation. Simulation includes function simulation and timing simulation. Function simulation, also known as pre simulation, is to verify whether the circuit meets the design requirements, and it is characterized by not considering the circuit gate delay and net delay.

Timing simulation, also known as post simulation or post PnR simulation, is the process of verifying whether a circuit can meet the design under certain timing conditions and whether there are timing violations, taking into account the effects of the circuit path delay and gate delay after the circuit has been mapped to a specific process environment.

7.1 Function Simulation Files

Function simulation includes user RTL design and post- synthesis netlist. The files required: user design RTL file before synthesis, netlist file after synthesis (*.vg), stimulus file (testbench) *tb.v and functional simulation library file prim_sim.v.

Note!

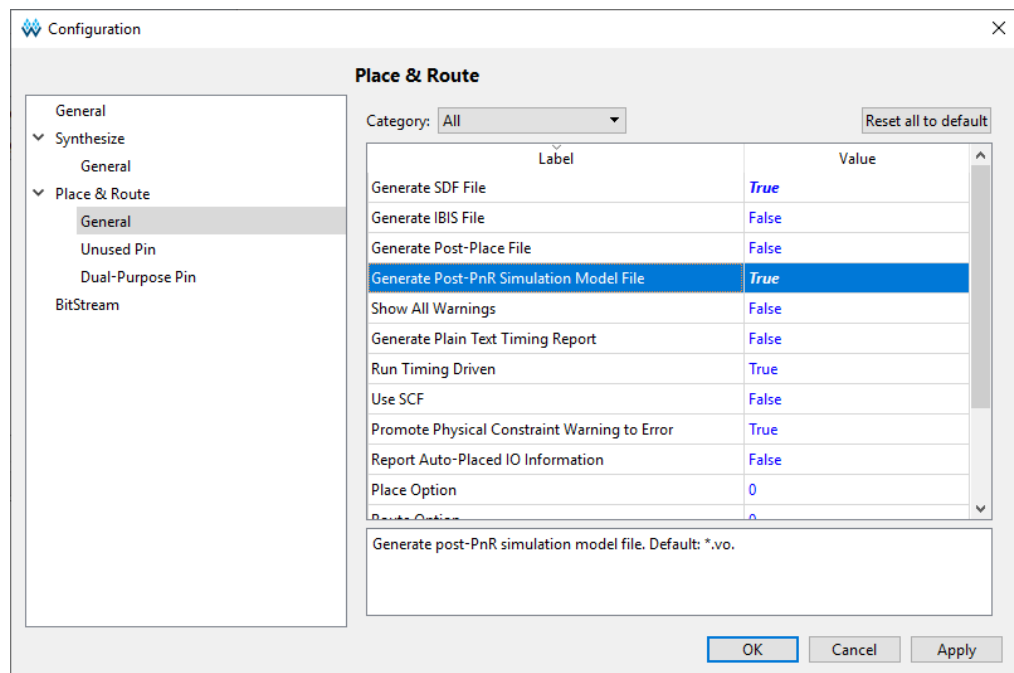
- The directory where the simulation library files are located: installPath\IDE\simlib.
- Since the generated IP is ciphertext, when there is an IP in the design, you need to use the vo file after IP generation as the function simulation file. The vo file is in the IP directory generated by src in the current project src\ipName\ipName.vo.

7.2 Timing Simulation Files

The files required: timing simulation logic netlist file *.vo, delay file *.sdf, stimulus file *tb.v, and the timing simulation library prim_tsim.v.

The *.vo and *.sdf can be generated in the running project. The specific steps are as follows.

1. After creating/opening the project, the Value of "Generate SDF File" and "Generate Post-PNR Simulation Model File" is set to True in the Place & Route option, then click "OK", as shown in Figure 7-1.

Figure 7-1 Configuration

2. Run Place & Route, and you can find the vo and sdf files under the project path of impl/pnr/.

8 Tcl Commands

Gowin Software supports command line mode. In the following description, the content in <> must be specified, and the content in [] is optional.

8.1 Start Command Line Mode

8.1.1 gw_sh.exe

Syntax

Command: Take Windows system as an example, start x.x\IDE\bin\gw_sh.exe under the installation directory.

Parameter:

[script file]

Parameter is null: Enter the command line console mode directly.

script file: Execute a specified script file, optional.

Application Example:

```
# Start Command Line mode
gw_sh.exe
#Execute script file
gw_sh.exe script_file
```

8.2 Command Description

8.2.1 add_file

```
add_file [-type] [- disable] [ -h/-help] <file...>
```

Add design file, and the file path separator can be written in two forms: / or \\ in Windows and Linux.

Parameter:

<File...> : The file to be added. You can specify more than one design file to add and the files are separated by spaces.

Options:

- -type add_file command automatically determines the file type based on the file suffix, or it can be used to specify the file type. The supported file types are verilog, vhdl, netlist, cst, sdc, fdc, gao, gpa, gsc.
- -disable: Disable the added file. The disabled file is added to the file list and is not used in the flow implementation. Relevant command: Set_file_enable
- -h, --help: Help information

For example:

```
add_file abc.v
add_file -type vhdl 1.vhd 2.vhdl 3.vhd
add_file D:/gowin_project/top.v
add_file D:\\gowin_project\\top.v
```

8.2.2 rm_file

```
rm_file [-h/-help ] <files...>
```

Remove file, and the file path separator can be written in two forms: / or \\ in Windows and Linux.

Parameter:

<File...> : The file to be removed. You can specify more than one design file to remove and the files are by spaces.

Option:

-h, --help: Help information

Example:

```
rm_file a.v
rm_file a.v b.v c.v
rm_file D:/gowin_project/top.v
rm_file D:\\gowin_project\\top.v
```

8.2.3 set_device

```
set_device [-name] [-h/-help ] <part number>
```

Set part number.

Parameter:

Device part number, such as GW1N-UV4LQ144C6/I5.

Options:

- -name <name>: Specify the name of the device, such as GW1N-4.
- -h, --help: Help information

Example:

```
set_device GW1N-LV1CS30C6/I5
set_device -name GW1N-4 GW1N-UV4LQ144C6/I5
```

8.2.4 set_file_prop

```
set_file_prop [-lib] [-h/-help] <file...>
```

Set file property, and the file path separator can be written in two forms: / or \\ in Windows and Linux.

Parameter:

<File...> : The file to be set. You can specify more than one file and the files are separated by spaces.

Options:

- -lib <name>: Set library name It is only valid for VHDL file.
- -h, --help: Help information

Example:

```
set_file_prop -lib work top .vhd
set_file_prop -lib work D:/gowin_project/top.vhd
set_file_prop -lib work D:\\gowin_project\\top.vhd
```

8.2.5 run

```
run [-h/-help] <syn/pnr/all>
```

Run the whole process or a process.

Parameter:

<process>: Specify the process name, such as syn and pnr. It can also specify all, indicating running the whole process.

Options:

-h, --help: Help information

Example:

```
run pnr
run all
```

8.2.6 set_file_enable

```
set_file_enable [-h/-help] <file> <true|false>
```

Enable the file or not, and the file path separator can be written in two forms: / or \\ in Windows and Linux.

Parameter:

- <file> : The file to be set.
- <true|false> true means the file can be used; false means it cannot be used.

Options:

-h, --help: Help information

Example:

```
set_file_enable top.v false
set_file_enable D:/gowin_project/top.v
set_file_enable D:\\gowin_project\\top.v
```

8.2.7 saveto

saveto [-all_options] [-h/-help] <file>

Save the current project to tcl script. The file path separator can be written in two forms: / or \\ in Windows and Linux.

Parameter:

<file> : The file to be exported.

Options:

- -all_options saveto: Save only the modified, which is different from the default value. You can save all information by -all_options.
- -h, --help: Help information

Example:

```
saveto project.tcl
saveto -all_options project.tcl
saveto -all_options D:/gowin_project/project.tcl
saveto -all_options D:\\gowin_project\\project.tcl
```

8.2.8 set_option

set_option [options]

Set options

Options:

- -output_base_name <name>

Specify the output files. This option specifies the base name of the file, and different processes use the appropriate extension based on the type of output file. For example, if -output_base_name abc, the netlist file generated by gowinsynthesis is named abc.vg.
- -synthesis_tool <tool>

Specify GowinSynthesis[®] as the synthesis tool.
- -top_module <name>

Specify Top Module/Entity
- -include_path <path or path list>

Specify include path When multiple include paths are specified, they need to be separated by a semicolon and the path is contained by a pair of braces {}, such as -include_path {/path1;/path2;/path3}.

Support relative path and absolute path, and the relative path means the current running path of the program.

- `-inc <incremental.cfg >`

Specify incremental.cfg.

Synthesis Configuration

- `-verilog_std <v1995|v2001|sysv2017>`

Specify Verilog: Verilog 95 / Verilog 2001 / System Verilog2017, and the default is Verilog 2001.

- `-vhdl_std <vhdl1993|vhdl2008>`

Specify VHDL: VHDL1993 / VHDL 2008, and the default is VHDL1993.

- `-dsp_balance <0|1>`

Specify whether to run DSP Balance automatically when synthesizing, and the default is 0.

0: No

1: Yes

- `-print_all_synthesis_warning <0|1>`

Specify whether to print all synthesis warnings, and the default value is 0.

0: No

1: Yes

- `-disable_io_insertion <0|1>`

Enable or disable I/O insertion, and the default is 0.

0: No

1: Yes

- `-looplimit <value>`

Set the loop limit value of the default editor in RTL, and the default value is 2000.

- `-maxfan <value>`

Set fanout for an input port, net, or register output, and the default is 10000.

- `-rw_check_on_ram <0|1>`

Enable this option to automatically insert bypass logic to prevent simulation mismatches for read during write.

0: No

1: Yes

Place & Route Configuration

- `-gen_sdf <0|1>`

Specify whether Place & Route to generate an SDF file, 0 by default.

0: No

1: Yes

- -gen_io_cst <0|1>

Specify whether Place & Route to generate port physical constraints file named as *.io.cst, and the default value is 0.

0: No

1: Yes

- -gen_ibis <0|1>

Specify whether Place & Route to generate the input/output buffer file named as *.ibs, and the default is 0.

0: No

1: Yes

- -gen_posp <0|1>

Specify whether Place & Route to generate place file with *.posp suffix, and the default is 0.

0: No

1: Yes

- -gen_text_timing_rpt <0|1>

Specify whether Place & Route to generate plain text timing report with suffix *.tr, and the default is 0.

0: No

1: Yes

- -gen_sim_netlist <0|1>

Specify whether Place & Route to generate simulation file with suffix *.vo., and the default is 0.

0: No

1: Yes

- -show_init_in_vo <0|1>

Add the default initial value to the instance of the generated PnR timing simulation model file, and the default is 0.

0: No

1: Yes

- -show_all_warn <0|1>

Output all warnings when Place & Route running, and the default is 0.

0: No

1: Yes

- `-timing_driven <0|1>`

Timing driven optimization of the placement and routing is performed, and the default is 1.

 - 0: No
 - 1: Yes
- `-use_scf <0|1>`

The *.scf file generated by Synplify Pro is used as an additional timing constraint file and defaults to 0.

 - 0: No
 - 1: Yes
- `-cst_warn_to_error <0|1>`

Change the Physical Constraint Warning to Error when Place & Route running, and the default is 1.

 - 0: No
 - 1: Yes
- `-rpt_auto_place_io_info <0|1>`

Report auto-placed IO location, and the default is 0.

 - 0: No
 - 1: Yes
- `-place_option <0|1>`

Place algorithm option, and the default is 0.

 - 0: Use default algorithm.
 - 1: Use algorithm 1.
- `-route_option <0|1|2>`

Route algorithm option, and the default is 0.

 - 0: Use default algorithm.
 - 1: Use algorithm 1
 - 2: Use algorithm 2
- `-ireg_in_iob <0|1>`

Enable this option, Place & Route will place the registers connected to the input Buffer to IOB, and the default is 1.

 - 0: Disable
 - 1: Enable
- `-oreg_in_iob <0|1>`

Enable this option, Place & Route will place the registers connected to the Output/Tristate Buffer to IOB, and the default is 1.

 - 0: Disable

1: Enable

- `-ioreg_in_iob <0|1>`

Enable this option, Place & Route will place the registers connected to the in/out Buffer to IOB, and the default is 1.

0: Disable

1: Enable

Note!

For more details, refer to [4.3.3 Place & Route](#) in this manual.

Dual-purpose Pins Configuration

- `-use_jtag_as_gpio <0|1>`

Use relevant pins of JTAG as regular IO pins. These relevant pins are TCK, TMS, TDI, and TDO, and the default is 0.

0: JTAG pin

1: General IO

- `-use_sspi_as_gpio <0|1>`

Use relevant pins of SSPI as regular IO pins. These relevant pins are SCLK, CLKHOLD_N, SI, SO, SSPI_CS_N, and the default is 0.

0: SSPI pin

1: General IO

- `-use_mspi_as_gpio <0|1>`

Use relevant pins of MSPI as regular IO pins. These relevant pins are MCLK, MCS_N, MI, MO, and the default is 0.

0: MSPI pin

1: General IO

- `-use_ready_as_gpio <0|1>`

Use READY as regular IO, and the default is 0.

0: READY pin

1: General IO

- `-use_done_as_gpio <0|1>`

Use DONE as regular IO, and the default is 0.

0: DONE pin

1: General IO

- `-use_reconfig_as_gpio <0|1>`

Use RECONFIG_N as regular IO, and the default is 0.

0: RECONFIG_N pin

1: General IO

- `-use_i2c_as_gpio <0|1>`

Use relevant pins of I2CI as regular IO pins. These relevant pins are SCL and SDA, and the default is 0.

0: I2C pin

1: General IO

BitStream Configuration

- `-bit_format <txt|bin>`
Specify the bitstream file format.
- `-bit_crc_check <0|1>`
Enable CRC check
0: Disable
1: Enable
- `-bit_compress <0|1>`
Compress the generated bitstream file
0: Disable
1: Enable
- `-bit_encrypt <0|1>`
Encrypt the bitstream file, only GW2A series supported.
0: Disable
1: Enable
- `-bit_encrypt_key <key>`
Use with "-bit_encrypt", and it allows you to customize the encrypted key.
- `-bit_security <0|1>`
Enable security bit
0: Disable
1: Enable
- `-bit_incl_bsrain_init <0|1>`
Print BSRAM Initial Value to Bitstream file
0: Disable
1: Enable
- `-bg_programming <off | jtag | i2c | internal | i2c_jtag_ssipi_qsspi>`
Background programming, programming Flash without interrupting the current FPGA running.
Off: Background programming off
Jtag: Background programming using JTAG mode
I2C: Background programming using I2C mode

Internal: Background programming using I2C internal logic

i2c_jtag_ssipi_qsspi: Background programming using I2C/JTAG/SSPI/QSSPI

- -hotboot <0|1>

0: Disable

1: Enable

- -i2c_slave_addr <value>

I2C Slave Address(Hex): 00~7F

- -secure_mode <0|1>

Enable secure mode. Use JTAG pin as GPIO, and device can be programmed only once.

0: Disable

1: Enable

- -loading_rate <value>

In AutoBoot mode and MSPI mode, the rate of loading bitstream data from Flash to SRAM is 2.500MHz by default.

- -spi_flash_addr <value>

Specify SPI Flash address

- -program_done_bypass <0|1>

After this option is configured, when the Done Final internal signal takes effect, the external Done Pin remains low so that new bitstream can be forwarded after the bitstream is loaded. The default is 0.

0: Disable

1: Enable

- -power_on_reset <0|1>

Power on reset enable

0: Disable

1: Enable

- -wakeup_mode <0|1>

Wake up mode enable

0: Disable

1: Enable

- -user_code <default|value>

You can customize user code.

Note!

For more details, refer to 4.3.3 BitStream in this manual.

Unused Pin Configuration

-unused_pin <default|open_drain>

Set IO types and attributes for unused pins (except dual-purpose pins).

Note!

For more details of Unused Pin option, refer to [4.3.3 Unused Pin](#) in this manual.

