Triple Channel PWM Controller with Integrated Driver for IMVP8 Mobile CPU Core Power Supply

General Description

The RT3601BC is an IMVP8 compliant CPU power controller which includes three voltage rails : a single phase synchronous Buck controller, the main VR, a 2/1 phase synchronous Buck controller, the auxiliary VR, and a single phase synchronous Buck controller, the VCCSA VR. The RT3601BC adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3601BC also features a quick response mechanism for optimized AVP performance during load transient. The RT3601BC supports mode transition function with various operating states. A serial VID (SVID) interface is built in the RT3601BC to communicate with Intel IMVP8 compliant CPU. The RT3601BC supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT3601BC varies with VID, load and input voltage to further enhance the efficiency even in CCM. Moreover, the G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT3601BC integrates a high accuracy ADC for platform setting functions, such as quick response trigger level. Besides, the setting function also supposes this two rails address exchange. The RT3601BC provides VR ready output signals. It also features complete fault protection functions including over-voltage (OV), negative voltage (NV), over-current (OC) and under-voltage lockout (UVLO). The RT3601BC is available in the WQFN-52L 6x6 small foot print package.

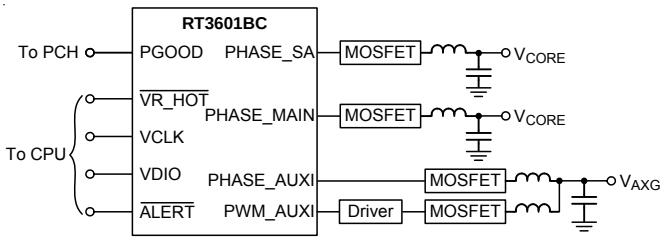
Features

- **Intel IMVP8 Serial VID Interface Compatible Power Management States**
- **Single Phase (Main VR) + 2/1 Phase (Auxiliary VR) + Single Phase (VCCSA VR) PWM Controller**
- **1 Embedded MOSFET Driver at the Main VR, 1 Embedded MOSFET Driver at the Auxiliary VR, and Embedded MOSFET Driver at the VCCSA VR**
- **G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Accurate Current Balance**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition for Multiple or Single Phase Operation**
- **Fast Transient Response**
- **VR Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **OVP, OCP, NVP, UVLO**
- **Slew Rate Setting/Address Flip Function**
- **DVID Enhancement**

Applications

- IMVP8 Intel Core Supply
- Notebook/ Desktop Computer/ Servers Multi-phase CPU Core Supply
- AVP Step-Down Converter

Simplified Application Circuit



Ordering Information

RT3601BC□□

Package Type
QW : WQFN-52L 6x6 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

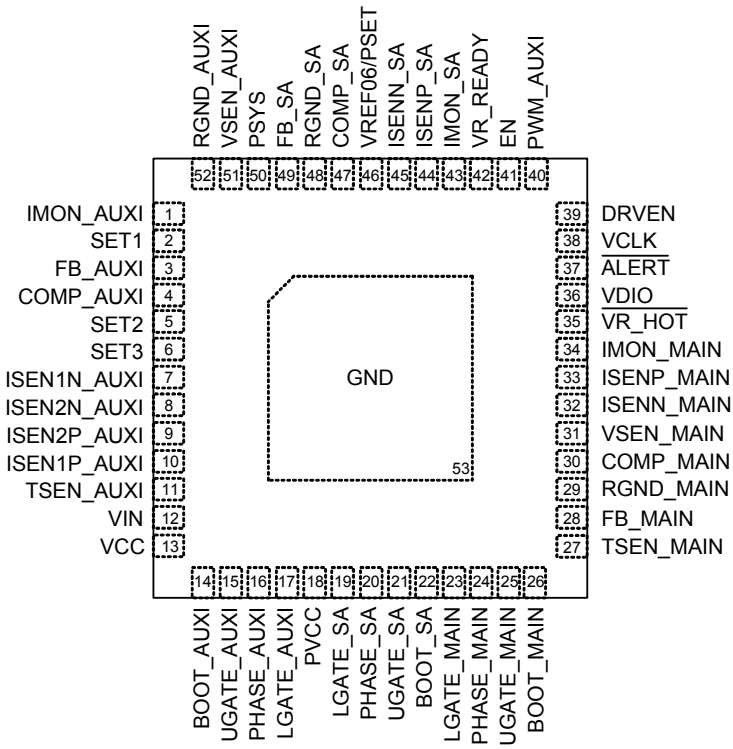
Marking Information

RT3601BCGQW : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WQFN-52L 6x6

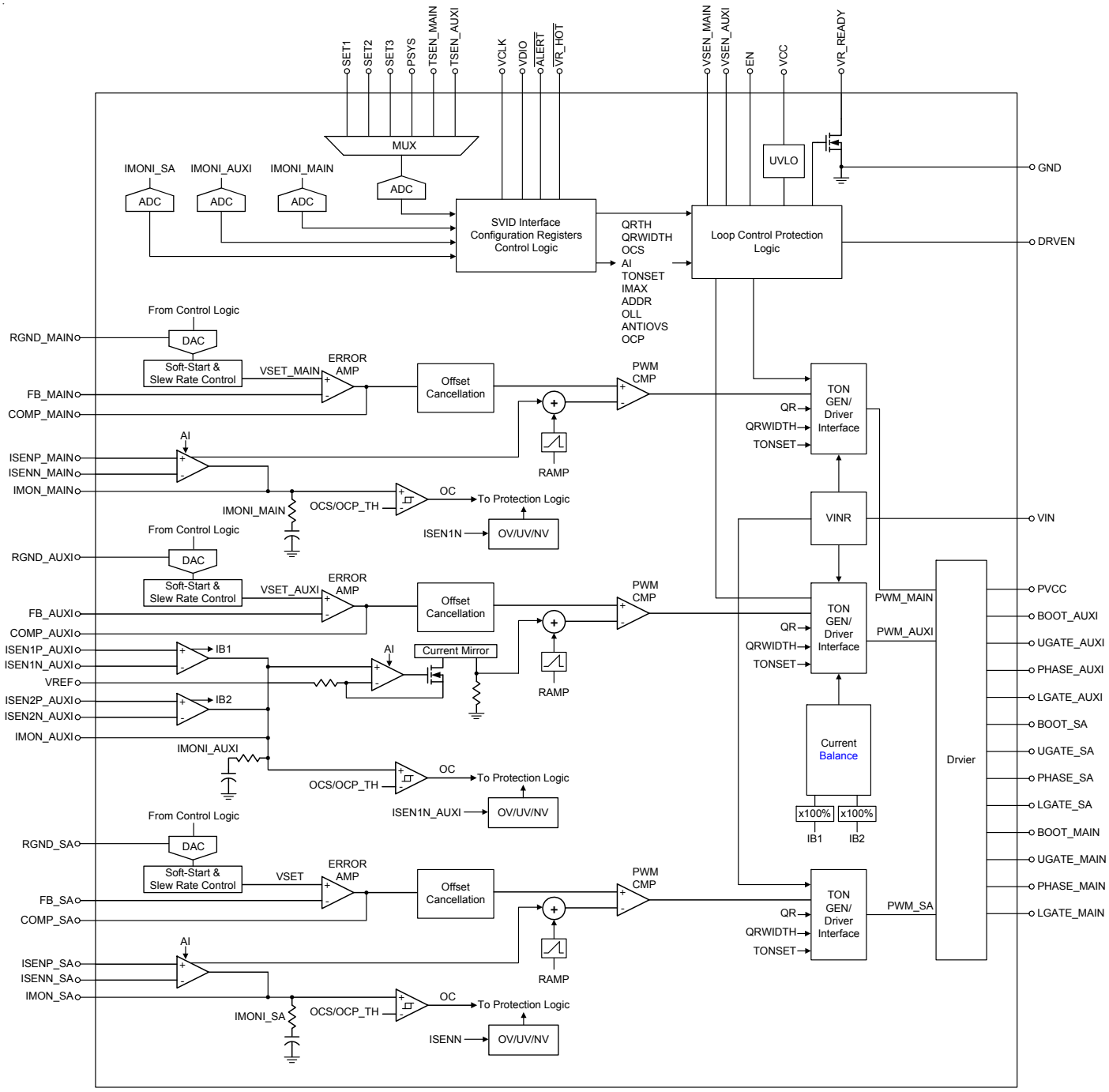
Functional Pin Description

Pin No	Pin Name	Pin Function
1	IMON_AUXI	Auxiliary Rail VR Current Monitor Output. This pin outputs a voltage proportional to the output current.
2	SET1	Platform Setting. Platform can use this pin to set switching frequency, ki gain, QRTH and QR width and for Main VR.
3	FB_AUXI	Negative Input of the Error Amplifier. This pin is for Auxiliary rail VR output voltage feedback to controller.
4	COMP_AUXI	Auxiliary Rail VR Compensation. This pin is error amplifier output pin.
5	SET2	Platform Setting. Platform can use this pin to set switching frequency, ki gain, QRTH and QR width for Auxiliary VR.
6	SET3	Platform Setting. Platform can use this pin to set switching frequency, ki gain zero load-line, QRTH and QR width for VCCSA rail. And it can be set Enable/Disable anti-overshoot function for each rail.
7, 8	ISEN[1:2]N_AUXI	Negative Current Sense Inputs of Multi-Phase Auxiliary Rail VR Channel 1 and 2.
10, 9	ISEN[1:2]P_AUXI	Positive Current Sense Inputs of Multi-Phase Auxiliary Rail VR Channel 1 and 2.
11	TSEN_AUXI	Thermal Sense Input for VR.
12	VIN	VIN Input Pin. Connect a low pass filter to this pin to set on-time.
13	VCC	Controller Power Supply. Connect this pin to 5V and place a decoupling capacitor 2.2μF at least. The decoupling capacitor is as close PWM controller as possible.

Pin No	Pin Name	Pin Function
14	BOOT_AUXI	Bootstrap Supply for High-Side Gate MOSFET Driver for Auxiliary rail VR.
15	UGATE_AUXI	High-Side Driver Output for Auxiliary rail VR. Connect the pin to the gate of high-side MOSFET.
16	PHASE_AUXI	Switch Node of High-Side Driver for Auxiliary rail VR. Connect the pin to high-side MOSFE source together with the low-side MOSFET drain and inductor.
17	LGATE_AUXI	Low-Side Driver Output for Auxiliary rail VR. This pin drives the gate of low-side MOSFET.
18	PVCC	Driver Power Supply Input. Connect this pin to GND by a minimum 2.2μF ceramic Capacitor.
19	LGATE_SA	Low-Side Driver Output for VCCSA VR. This pin drives the gate of low-side MOSFET.
20	PHASE_SA	Switch Node of High-Side Driver for VCCSA VR. Connect the pin to high-side MOSFE source together with the low-side MOSFET drain and inductor.
21	UGATE_SA	High-Side Driver Output for VCCSA VR. Connect the pin to the gate of high-side MOSFET.
22	BOOT_SA	Bootstrap Supply for High-Side Gate MOSFET Driver for VCCSA VR.
23	LGATE_MAIN	Low-Side Driver Output for MAIN rail VR. This pin drives the gate of low-side MOSFET.
24	PHASE_MAIN	Switch Node of High-Side Driver for MAIN rail VR. Connect the pin to high-side MOSFE source together with the low-side MOSFET drain and inductor.
25	UGATE_MAIN	High-Side Driver Output for MAIN rail VR. Connect the pin to the gate of high-side MOSFET.
26	BOOT_MAIN	Bootstrap Supply for High-Side Gate MOSFET Driver for MAIN rail VR.
27	TSEN_MAIN	Thermal Sense Input for Main Rail VR.
28	FB_MAIN	Negative Input of the Error Amplifier. This pin is for main rail VR output voltage feedback to controller.
29	RGND_MAIN	Return Ground for Main Rail VR. This pin is the negative node of the differential remote voltage sensing.
30	COMP_MAIN	Main Rail VR Compensation. This pin is error amplifier output pin.
31	VSEN_MAIN	Main VR Voltage Sense Input. This pin is connected to the terminal of Main VR output voltage.
32	ISENN_MAIN	Negative Current Sense Input of Single-Phase Main Rail.
33	ISENP_MAIN	Positive Current Sense Input of Single-Phase Main Rail.
34	IMON_MAIN	Main Rail VR Current Monitor Output. This pin outputs a voltage proportional to the output current.
35	$\overline{\text{VR\_HOT}}$	Thermal Monitor Output, this Pin is Active Low.
36	VDIO	VR and CPU Data Transmission Interface.
37	$\overline{\text{ALERT}}$	SVID Alert. (Active low)
38	VCLK	Synchronous Clock from the CPU.
39	DRVEN	External Driver Enable Control. Connecting to driver enable pin.

Pin No	Pin Name	Pin Function
40	PWM_AUXI	PWM Outputs for Auxiliary VR.
41	EN	VR Enable Control Input.
42	VR_READY	VR Ready Indicator.
43	IMON_SA	VCCSA Rail VR Current Monitor Output. This pin outputs a voltage proportional to the output current.
44	ISENP_SA	Positive Current Sense Input of Single-Phase VCCSA Rail VR.
45	ISENN_SA	Negative Current Sense Input of Single-Phase VCCSA Rail VR.
46	VREF06/PSET	Fixed 0.6V Output Reference Voltage. This voltage is used to offset the output voltage of IMON pin. Between this pin and GND must be placed a exact 0.47μF decoupling capacitor.
47	COMP_SA	VCCSA Rail VR Compensation. This pin is error amplifier output pin.
48	RGND_SA	Return Ground for VCCSA Rail VR. This pin is the negative node of the differential remote voltage sensing.
49	FB_SA	Negative Input of the Error Amplifier. This pin is for VCCSA rail VR output voltage feedback to controller.
50	PSYS	System Input Power Monitor.
51	VSEN_AUXI	AUXI VR Voltage Sense Input. This pin is connected to the terminal of AUXI VR output voltage.
52	RGND_AUXI	Return Ground for Auxiliary Rail VR. This pin is the negative node of the differential remote voltage sensing.
53 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

The RT3601BC adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning).

The G-NAVP™ controller is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches COMP signal, the RT3601BC generates an on-time width to achieve PWM modulation.

TON GEN/Driver Interface PWMx

Generate the sequentially according to the phase control signal from the Loop Control/Protection Logic. Pulse width is determined by current balance result and pin setting. Once quick response mechanism is triggered, VR will allow all PWM to turn on at the same time. PWM status is also controlled by Protection Logic. Different protections may cause different PWM status (Both High-Z or LG turn-on).

SVID Interface/Configuration Registers/Control Logic

The interface receives the SVID signal from CPU and sends the relative signals to Loop Control/Protection Logic for loop control to execute the action by CPU. The registers save the pin setting data from ADC output. The Control Logic controls the ADC timing, generates the digital code of the VID for VSEN voltage.

Loop Control/Protection Logic

It controls the power on sequence, the protection behavior, and the operational phase number.

MUX and ADC

The MUX supports the inputs from SET1, SET2, SET3, IMON_MAIN, IMON_AUXI, TSEN_MAIN and TSEN_AUXI. The ADC converts these analog signals to digital codes for reporting or performance adjustment.

Current Balance

Each phase current sense signal is sent to the current balance circuit which adjusts the on-time of each phase to optimize current sharing.

Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

UVLO

Detect the VCC voltage and issue POR signal as they are high enough.

DAC

Generate an analog signal according to the digital code generated by Control Logic.

Soft-Start & Slew Rate Control

Control the Dynamic VID slew rate of VSEN according to the SetVID fast or SetVID slow.

Error Amp

Error amplifier generates COMP_MAIN/COMP_AUXI/COMP_SA signal by the difference between output of Main/Auxiliary/SA rail and FB_MAIN/FB_AUXI/FB_SA.

PWM CMP

The PWM comparator compares COMP signal and current feedback signal to generate a signal for TON trigger.

IMON Filter

IMON Filter is used for average sum current signal by analog RC filter.

Table 1. IMVP8 VID Code Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	0	0	0	0	0	1	01	0.25
0	0	0	0	0	0	1	0	02	0.255
0	0	0	0	0	0	1	1	03	0.26
0	0	0	0	0	1	0	0	04	0.265
0	0	0	0	0	1	0	1	05	0.27
0	0	0	0	0	1	1	0	06	0.275
0	0	0	0	0	1	1	1	07	0.28
0	0	0	0	1	0	0	0	08	0.285
0	0	0	0	1	0	0	1	09	0.29
0	0	0	0	1	0	1	0	0A	0.295
0	0	0	0	1	0	1	1	0B	0.3
0	0	0	0	1	1	0	0	0C	0.305
0	0	0	0	1	1	0	1	0D	0.31
0	0	0	0	1	1	1	0	0E	0.315
0	0	0	0	1	1	1	1	0F	0.32
0	0	0	1	0	0	0	0	10	0.325
0	0	0	1	0	0	0	1	11	0.33
0	0	0	1	0	0	1	0	12	0.335
0	0	0	1	0	0	1	1	13	0.34
0	0	0	1	0	1	0	0	14	0.345
0	0	0	1	0	1	0	1	15	0.35
0	0	0	1	0	1	1	0	16	0.355
0	0	0	1	0	1	1	1	17	0.36
0	0	0	1	1	0	0	0	18	0.365
0	0	0	1	1	0	0	1	19	0.37
0	0	0	1	1	0	1	0	1A	0.375
0	0	0	1	1	0	1	1	1B	0.38
0	0	0	1	1	1	0	0	1C	0.385
0	0	0	1	1	1	0	1	1D	0.39
0	0	0	1	1	1	1	0	1E	0.395
0	0	0	1	1	1	1	1	1F	0.4
0	0	1	0	0	0	0	0	20	0.405
0	0	1	0	0	0	0	1	21	0.41
0	0	1	0	0	0	1	0	22	0.415
0	0	1	0	0	0	1	1	23	0.42
0	0	1	0	0	1	0	0	24	0.425

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	1	0	0	1	0	1	25	0.43
0	0	1	0	0	1	1	0	26	0.435
0	0	1	0	0	1	1	1	27	0.44
0	0	1	0	1	0	0	0	28	0.445
0	0	1	0	1	0	0	1	29	0.45
0	0	1	0	1	0	1	0	2A	0.455
0	0	1	0	1	0	1	1	2B	0.46
0	0	1	0	1	1	0	0	2C	0.465
0	0	1	0	1	1	0	1	2D	0.47
0	0	1	0	1	1	1	0	2E	0.475
0	0	1	0	1	1	1	1	2F	0.48
0	0	1	1	0	0	0	0	30	0.485
0	0	1	1	0	0	0	1	31	0.49
0	0	1	1	0	0	1	0	32	0.495
0	0	1	1	0	0	1	1	33	0.5
0	0	1	1	0	1	0	0	34	0.505
0	0	1	1	0	1	0	1	35	0.51
0	0	1	1	0	1	1	0	36	0.515
0	0	1	1	0	1	1	1	37	0.52
0	0	1	1	1	0	0	0	38	0.525
0	0	1	1	1	0	0	1	39	0.53
0	0	1	1	1	0	1	0	3A	0.535
0	0	1	1	1	0	1	1	3B	0.54
0	0	1	1	1	1	0	0	3C	0.545
0	0	1	1	1	1	0	1	3D	0.55
0	0	1	1	1	1	1	0	3E	0.555
0	0	1	1	1	1	1	1	3F	0.56
0	1	0	0	0	0	0	0	40	0.565
0	1	0	0	0	0	0	1	41	0.57
0	1	0	0	0	0	1	0	42	0.575
0	1	0	0	0	0	1	1	43	0.58
0	1	0	0	0	1	0	0	44	0.585
0	1	0	0	0	1	0	1	45	0.59
0	1	0	0	0	1	1	0	46	0.595
0	1	0	0	0	1	1	1	47	0.6
0	1	0	0	1	0	0	0	48	0.605
0	1	0	0	1	0	0	1	49	0.61

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	0	0	1	0	1	0	4A	0.615
0	1	0	0	1	0	1	1	4B	0.62
0	1	0	0	1	1	0	0	4C	0.625
0	1	0	0	1	1	0	1	4D	0.63
0	1	0	0	1	1	1	0	4E	0.635
0	1	0	0	1	1	1	1	4F	0.64
0	1	0	1	0	0	0	0	50	0.645
0	1	0	1	0	0	0	1	51	0.65
0	1	0	1	0	0	1	0	52	0.655
0	1	0	1	0	0	1	1	53	0.66
0	1	0	1	0	1	0	0	54	0.665
0	1	0	1	0	1	0	1	55	0.67
0	1	0	1	0	1	1	0	56	0.675
0	1	0	1	0	1	1	1	57	0.68
0	1	0	1	1	0	0	0	58	0.685
0	1	0	1	1	0	0	1	59	0.69
0	1	0	1	1	0	1	0	5A	0.695
0	1	0	1	1	0	1	1	5B	0.7
0	1	0	1	1	1	0	0	5C	0.705
0	1	0	1	1	1	0	1	5D	0.71
0	1	0	1	1	1	1	0	5E	0.715
0	1	0	1	1	1	1	1	5F	0.72
0	1	1	0	0	0	0	0	60	0.725
0	1	1	0	0	0	0	1	61	0.73
0	1	1	0	0	0	1	0	62	0.735
0	1	1	0	0	0	1	1	63	0.74
0	1	1	0	0	1	0	0	64	0.745
0	1	1	0	0	1	0	1	65	0.75
0	1	1	0	0	1	1	0	66	0.755
0	1	1	0	0	1	1	1	67	0.76
0	1	1	0	1	0	0	0	68	0.765
0	1	1	0	1	0	0	1	69	0.77
0	1	1	0	1	0	1	0	6A	0.775
0	1	1	0	1	0	1	1	6B	0.78
0	1	1	0	1	1	0	0	6C	0.785
0	1	1	0	1	1	0	1	6D	0.79
0	1	1	0	1	1	1	0	6E	0.795

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	1	0	1	1	1	1	6F	0.8
0	1	1	1	0	0	0	0	70	0.805
0	1	1	1	0	0	0	1	71	0.81
0	1	1	1	0	0	1	0	72	0.815
0	1	1	1	0	0	1	1	73	0.82
0	1	1	1	0	1	0	0	74	0.825
0	1	1	1	0	1	0	1	75	0.83
0	1	1	1	0	1	1	0	76	0.835
0	1	1	1	0	1	1	1	77	0.84
0	1	1	1	1	0	0	0	78	0.845
0	1	1	1	1	0	0	1	79	0.85
0	1	1	1	1	0	1	0	7A	0.855
0	1	1	1	1	0	1	1	7B	0.86
0	1	1	1	1	1	0	0	7C	0.865
0	1	1	1	1	1	0	1	7D	0.87
0	1	1	1	1	1	1	0	7E	0.875
0	1	1	1	1	1	1	1	7F	0.88
1	0	0	0	0	0	0	0	80	0.885
1	0	0	0	0	0	0	1	81	0.89
1	0	0	0	0	0	1	0	82	0.895
1	0	0	0	0	0	1	1	83	0.9
1	0	0	0	0	1	0	0	84	0.905
1	0	0	0	0	1	0	1	85	0.91
1	0	0	0	0	1	1	0	86	0.915
1	0	0	0	0	1	1	1	87	0.92
1	0	0	0	1	0	0	0	88	0.925
1	0	0	0	1	0	0	1	89	0.93
1	0	0	0	1	0	1	0	8A	0.935
1	0	0	0	1	0	1	1	8B	0.94
1	0	0	0	1	1	0	0	8C	0.945
1	0	0	0	1	1	0	1	8D	0.95
1	0	0	0	1	1	1	0	8E	0.955
1	0	0	0	1	1	1	1	8F	0.96
1	0	0	1	0	0	0	0	90	0.965
1	0	0	1	0	0	0	1	91	0.97
1	0	0	1	0	0	1	0	92	0.975
1	0	0	1	0	0	1	1	93	0.98

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	0	0	1	0	1	0	0	94	0.985
1	0	0	1	0	1	0	1	95	0.99
1	0	0	1	0	1	1	0	96	0.995
1	0	0	1	0	1	1	1	97	1
1	0	0	1	1	0	0	0	98	1.005
1	0	0	1	1	0	0	1	99	1.01
1	0	0	1	1	0	1	0	9A	1.015
1	0	0	1	1	0	1	1	9B	1.02
1	0	0	1	1	1	0	0	9C	1.025
1	0	0	1	1	1	0	1	9D	1.03
1	0	0	1	1	1	1	0	9E	1.035
1	0	0	1	1	1	1	1	9F	1.04
1	0	1	0	0	0	0	0	A0	1.045
1	0	1	0	0	0	0	1	A1	1.05
1	0	1	0	0	0	1	0	A2	1.055
1	0	1	0	0	0	1	1	A3	1.06
1	0	1	0	0	1	0	0	A4	1.065
1	0	1	0	0	1	0	1	A5	1.07
1	0	1	0	0	1	1	0	A6	1.075
1	0	1	0	0	1	1	1	A7	1.08
1	0	1	0	1	0	0	0	A8	1.085
1	0	1	0	1	0	0	1	A9	1.09
1	0	1	0	1	0	1	0	AA	1.095
1	0	1	0	1	0	1	1	AB	1.1
1	0	1	0	1	1	0	0	AC	1.105
1	0	1	0	1	1	0	1	AD	1.11
1	0	1	0	1	1	1	0	AE	1.115
1	0	1	0	1	1	1	1	AF	1.12
1	0	1	1	0	0	0	0	B0	1.125
1	0	1	1	0	0	0	1	B1	1.13
1	0	1	1	0	0	1	0	B2	1.135
1	0	1	1	0	0	1	1	B3	1.14
1	0	1	1	0	1	0	0	B4	1.145
1	0	1	1	0	1	0	1	B5	1.15
1	0	1	1	0	1	1	0	B6	1.155
1	0	1	1	0	1	1	1	B7	1.16
1	0	1	1	1	0	0	0	B8	1.165

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	0	1	1	1	0	0	1	B9	1.17
1	0	1	1	1	0	1	0	BA	1.175
1	0	1	1	1	0	1	1	BB	1.18
1	0	1	1	1	1	0	0	BC	1.185
1	0	1	1	1	1	0	1	BD	1.19
1	0	1	1	1	1	1	0	BE	1.195
1	0	1	1	1	1	1	1	BF	1.2
1	1	0	0	0	0	0	0	C0	1.205
1	1	0	0	0	0	0	1	C1	1.21
1	1	0	0	0	0	1	0	C2	1.215
1	1	0	0	0	0	1	1	C3	1.22
1	1	0	0	0	1	0	0	C4	1.225
1	1	0	0	0	1	0	1	C5	1.23
1	1	0	0	0	1	1	0	C6	1.235
1	1	0	0	0	1	1	1	C7	1.24
1	1	0	0	1	0	0	0	C8	1.245
1	1	0	0	1	0	0	1	C9	1.25
1	1	0	0	1	0	1	0	CA	1.255
1	1	0	0	1	0	1	1	CB	1.26
1	1	0	0	1	1	0	0	CC	1.265
1	1	0	0	1	1	0	1	CD	1.27
1	1	0	0	1	1	1	0	CE	1.275
1	1	0	0	1	1	1	1	CF	1.28
1	1	0	1	0	0	0	0	D0	1.285
1	1	0	1	0	0	0	1	D1	1.29
1	1	0	1	0	0	1	0	D2	1.295
1	1	0	1	0	0	1	1	D3	1.3
1	1	0	1	0	1	0	0	D4	1.305
1	1	0	1	0	1	0	1	D5	1.31
1	1	0	1	0	1	1	0	D6	1.315
1	1	0	1	0	1	1	1	D7	1.32
1	1	0	1	1	0	0	0	D8	1.325
1	1	0	1	1	0	0	1	D9	1.33
1	1	0	1	1	0	1	0	DA	1.335
1	1	0	1	1	0	1	1	DB	1.34
1	1	0	1	1	1	0	0	DC	1.345
1	1	0	1	1	1	0	1	DD	1.35

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	1	0	1	1	1	1	0	DE	1.355
1	1	0	1	1	1	1	1	DF	1.36
1	1	1	0	0	0	0	0	E0	1.365
1	1	1	0	0	0	0	1	E1	1.37
1	1	1	0	0	0	1	0	E2	1.375
1	1	1	0	0	0	1	1	E3	1.38
1	1	1	0	0	1	0	0	E4	1.385
1	1	1	0	0	1	0	1	E5	1.39
1	1	1	0	0	1	1	0	E6	1.395
1	1	1	0	0	1	1	1	E7	1.4
1	1	1	0	1	0	0	0	E8	1.405
1	1	1	0	1	0	0	1	E9	1.41
1	1	1	0	1	0	1	0	EA	1.415
1	1	1	0	1	0	1	1	EB	1.42
1	1	1	0	1	1	0	0	EC	1.425
1	1	1	0	1	1	0	1	ED	1.43
1	1	1	0	1	1	1	0	EE	1.435
1	1	1	0	1	1	1	1	EF	1.44
1	1	1	1	0	0	0	0	F0	1.445
1	1	1	1	0	0	0	1	F1	1.45
1	1	1	1	0	0	1	0	F2	1.455
1	1	1	1	0	0	1	1	F3	1.46
1	1	1	1	0	1	0	0	F4	1.465
1	1	1	1	0	1	0	1	F5	1.47
1	1	1	1	0	1	1	0	F6	1.475
1	1	1	1	0	1	1	1	F7	1.48
1	1	1	1	1	0	0	0	F8	1.485
1	1	1	1	1	0	0	1	F9	1.49
1	1	1	1	1	0	1	0	FA	1.495
1	1	1	1	1	0	1	1	FB	1.5
1	1	1	1	1	1	0	0	FC	1.505
1	1	1	1	1	1	0	1	FD	1.51
1	1	1	1	1	1	1	0	FE	1.515
1	1	1	1	1	1	1	1	FF	1.52

Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- VIN to GND ---------- –0.3V to 28
- Other Pins ---------- –0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-52L 6x6 ---------- 3.77W
- Package Thermal Resistance (Note 2)
  WQFN-52L 6x6, θ_{JA} ---------- 26.5°C/W
  WQFN-52L 6x6, θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Supply Voltage, PVCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{VCC}	EN = 1.05V, No Switching	--	9	15	mA
Supply Current at PS3	I_{VCC_PS4}	EN = 1.05V, No Switching	--	0.2	--	
Shutdown Current	I_{SHDN}	EN = 0V	--	--	10	μA
Driver Supply Voltage	V_{PVCC}		4.5	--	5.5	V
Reference and DAC						
DAC Accuracy	V_{FB}	VDAC = 0.75V – 1.52V	–0.5%	0	0.5%	% of VID
		VDAC = 0.5V – 0.745V	–8	0	8	mV
		VDAC = 0.25V – 0.495V	–10	0	10	
Slew Rate						
Dynamic VID Slew Rate	SR	Set VID Fast	30	37.5	--	mV/μs
		Set VID Slow, set slow = 1/2 Fast	15	18.75	--	
EA Amplifier						
DC Gain	ADC	R_L = 47kΩ	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	--	5	--	MHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset	V_{EAOFS}		–3	--	3	mV
Slew Rate	SREA	C_{LOAD} = 10pF (Gain= –4, R_F = 47kΩ, V_{OUT} =0.5V to -3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.3	--	3.6	V
Max Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	5	--	mA
Current Sensing Amplifier						
Input Offset Voltage	V_{OSCS}		–0.4	--	0.4	mV
Impedance at Positive Input	RISENxP		1	--	--	MΩ
Current Mirror Gain	AMIRROR	IIMON/ISENxN	0.97	1	1.03	A/A
Input Range	V_{ISEN_IN}	V_{DAC} = 1.1V, ISENP_x – ISENN_x	–40	--	40	mV
TON Setting						
On-Time Setting	T_{ON}	V_{IN} = 10V, V_{DAC} = 1V, Freq. = 400k	--	250	--	ns
Minimum Off time	T_{OFF}	VDAC = 1	--	150	--	ns
Protections						
Under-Voltage Lockout Threshold	V_{UVLO}	Falling edge	3.9	4.1	4.3	V
	ΔV_{UVLO}	Rising edge hysteresis	--	150	--	mV
Over-Voltage Protection Threshold	V_{OV}	Respect to VID voltage	VID + 300	VID + 350	VID + 400	mV
		Lower limit to 1V	950	1000	1050	mV
Under-Voltage Protection Threshold	V_{UV}	Respect to VID voltage	–400	–350	–300	mV
						mV
Negative Voltage Protection Threshold	V_{NV}		–100	–50	--	mV
VRON and VR_READY						
VRON Threshold	V_{IH}	Respect to 1V, 70%	0.7	--	--	V
	V_{IL}	Respect to 1V, 30%	--	--	0.3	V
Leakage Current of VRON			–1	--	1	μA
PGOOD Pull Low Voltage	V_{PGOOD}	I_{VR_Ready} = 10mA	--	--	0.13	V
Serial VID and $\overline{\text{VR\_HOT}}$						
VCLK, VDIO	V_{IH}	Respect to INTEL Spec. with 50mV hysteresis	0.65	--	--	V
	V_{IL}		--	--	0.45	
Leakage Current of VCLK, VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR\_HOT}}$	I_{LEAK_IN}		–1	--	1	μA
VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR\_HOT}}$ Pull Low Voltage		I_{VDIO} = 10mA	--	--	0.13	V
		$I_{\overline{ALERT}}$ = 10mA				
		$I_{\overline{VR\_HOT}}$ = 10mA				

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VREF						
VREF06	V_{REF}		0.595	0.6	0.605	V
ADC						
Digital IMON Set	V_{IMON}	$V_{IMON} - V_{IMON\_INI}$ = 0.8V, Auxiliary rail, 2 phase application	--	255	--	Decimal
		$V_{IMON} - V_{IMON\_INI}$ = 0.4V, Main rail	--	255	--	
Update Period	T_{IMON}		--	125	--	μs
TSEN Threshold for Tmp_Zone[7] Transition	V_{TSEN}	100°C	--	1.092	--	V
TSEN Threshold for Tmp_Zone[6] Transition		97°C	--	1.132	--	
TSEN Threshold for Tmp_Zone[5] Transition		94°C	--	1.176	--	
TSEN Threshold for Tmp_Zone[4] Transition		91°C	--	1.226	--	
TSEN Threshold for Tmp_Zone[3] Transition		88°C	--	1.283	--	
TSEN Threshold for Tmp_Zone[2] Transition		85°C	--	1.346	--	
TSEN Threshold for Tmp_Zone[1] Transition		82°C	--	1.418	--	
TSEN Threshold for Tmp_Zone[0] Transition		75°C	--	1.624	--	
Update Period	T_{tsen}		--	100	--	μs
Switching Timing						
UGATEx Rising Time	t_{UGATEr}	3nF load	--	25	--	ns
UGATEx Falling Time	t_{UGATEf}	3nF load	--	12	--	ns
LGATEx Rising Time	t_{LGATEr}	3nF load	--	24	--	ns
LGATEx Falling Time	t_{LGATEf}	3nF load	--	10	--	ns
Propagation Delay	$t_{UGATEpgh}$	$V_{BOOTx} - V_{PHASEx}$ = 12V See Timing Diagram	--	60	--	ns
	$t_{UGATEpdl}$		--	22	--	
	$t_{LGATEpdh}$	See Timing Diagram	--	30	--	
	$t_{LGATEpdl}$		--	8	--	
Output						
UGATEx Drive Source	$R_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 12V, I_{Source} = 100mA	--	1.7	--	Ω
UGATEx Drive Sink	$R_{UGATEsk}$	$V_{BOOT} - V_{PHASE}$ = 12V, I_{Sink} = 100mA	--	1.4	--	Ω
LGATEx Drive Source	$R_{LGATEsr}$	I_{Source} = 100mA	--	1.6	--	Ω
LGATEx Drive Sink	$R_{LGATEsk}$	I_{Sink} = 100mA	--	1.1	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ITSEN						
TSEN Source Current	I_{TSEN}	TSEN = 1.6V	79.2	80	80.8	μA

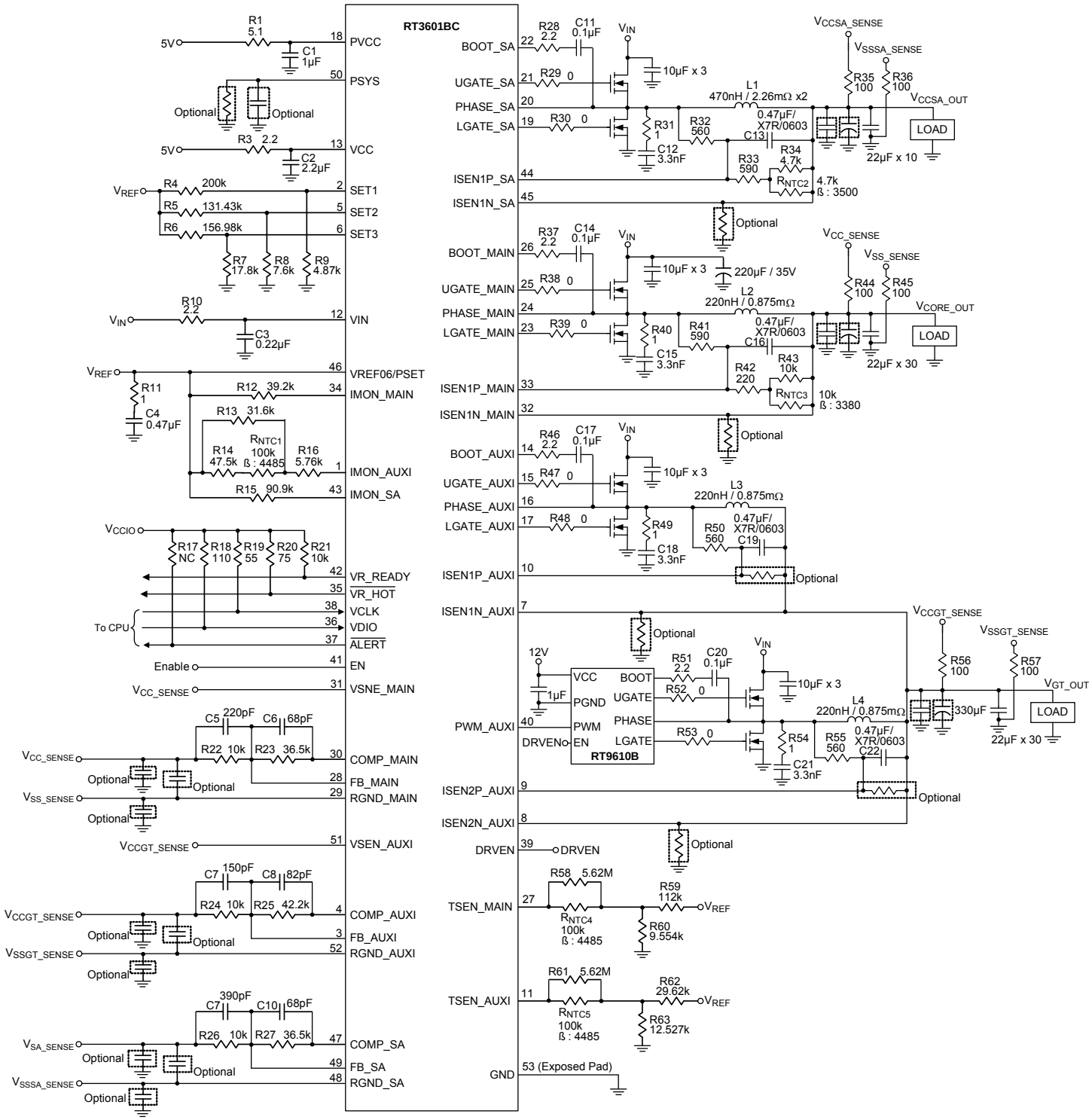
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



Applications information

The RT3601BC includes three voltage rails : a single phase synchronous Buck controller, the main VR, a 2/1 multiphase synchronous Buck controller, the auxiliary VR, and a single phase synchronous Buck controller, the VCCSA VR, designed to meet Intel IMVP8 compatible CPUs specification with a serial SVID control interface. The controller uses an ADC to implement all kinds of settings to save total pin number for easy use and increasing PCB space utilization. The RT3601BC is used in notebooks, desktop computers and servers.

General loop Function

G-NAVP™ Control Mode

The RT3601BC adopts the G-NAVP™ controller, which is a current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches comp signal, the RT3601BC generates an on-time width to achieve PWM modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms in continuous conduct mode (CCM).

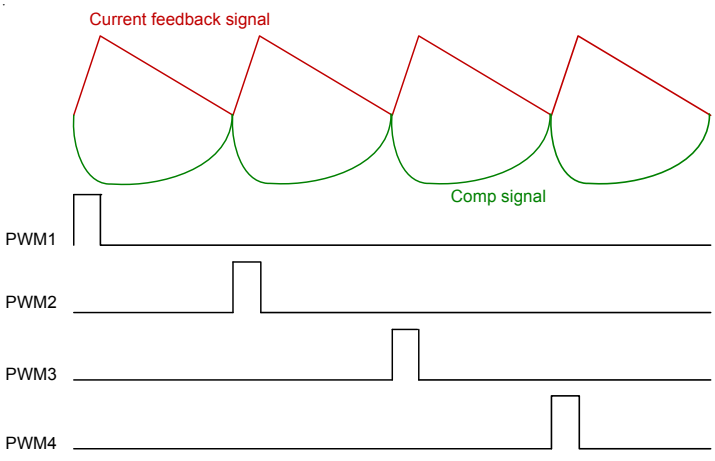


Figure 1 (a). G-NAVP™ Behavior Waveforms in CCM in Steady State

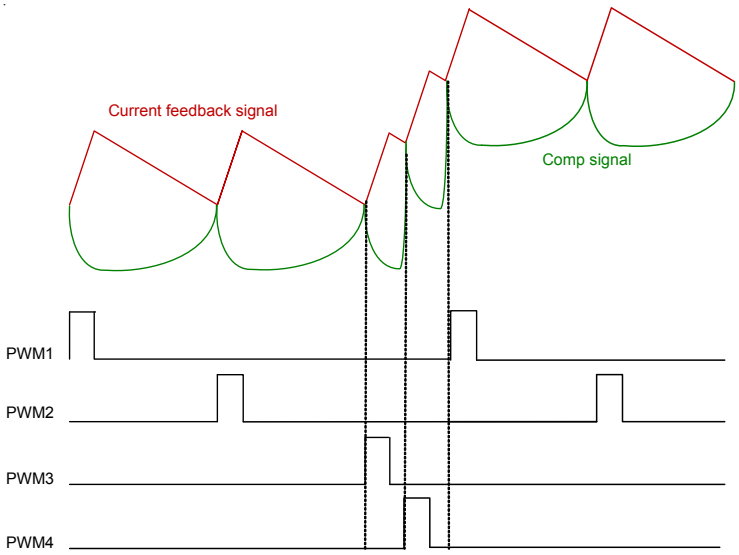


Figure 1 (b). G-NAVP™ Behavior Waveforms in CCM in Load Transient.

Diode Emulation Mode (DEM)

As well-known, the dominate power loss is switching related loss during light load, hence VR needs to be operated in asynchronous mode (or called discontinuous conduct mode, DCM) to reduce switching related loss since switching frequency is dependent on loading in the asynchronous mode. The RT3601BC can operate in diode emulation mode (DEM) to improve light load efficiency. In DEM operation, the behavior of low-side MOSFET(s) needs to work like a diode, that is, the low-side MOSFET(s) will be turned on when the phase voltage is a negative value, i.e. the inductor current follows from Source to Drain of low-side MOSFET(s). And the low-side MOSFET(s) will be turned off when phase voltage is a positive value, i.e. reversed current is not allowed. Figure 2 shows the control behavior in DEM. Figure 3 shows the G-NAVP™ operation in DEM to illustrate the control behaviors. When the load decreases, the discharge time of output capacitors increases during UGATE and LGATE are turned off. Hence, the switching frequency and switching loss will be reduced to improve efficiency in light load condition.

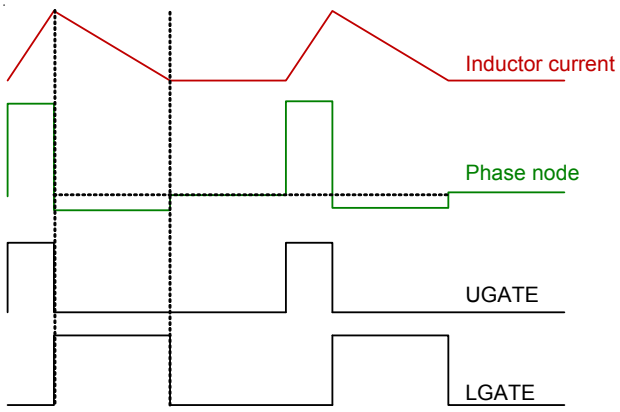


Figure 2. Diode Emulation Mode (DEM) in Steady State

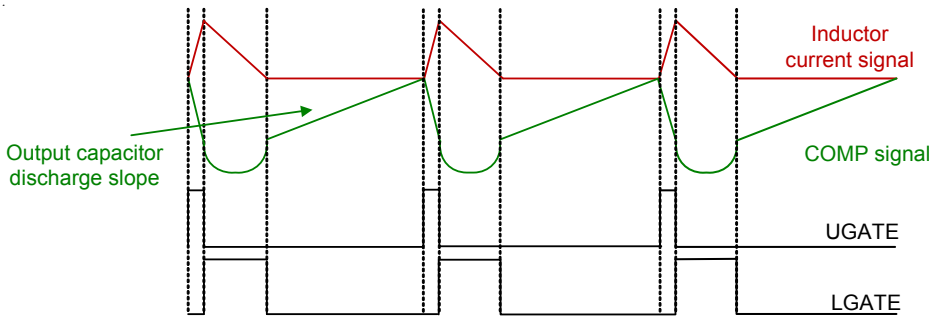


Figure 3. (a)

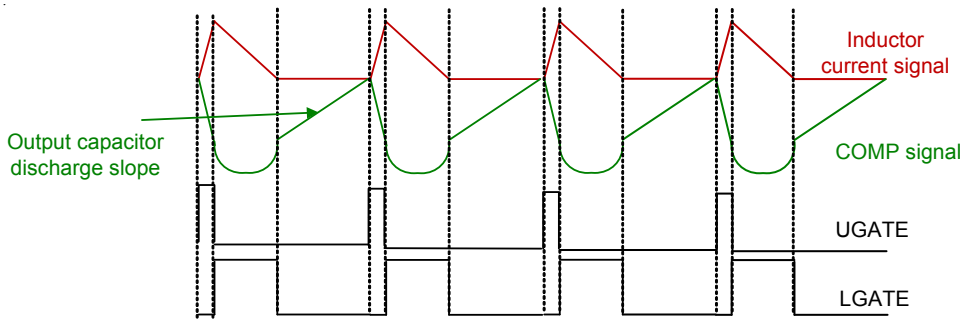


Figure 3. (b)

Figure 3. G-NAVP™ Operation in DEM. (a) : The load is lighter, output capacitor discharge slope is smaller and the switching frequency is lower. (b) : The load is increasing, output capacitor discharge slope is increased and switching frequency is increased, too.

Phase Interleaving Function

The RT3601BC is a multiphase controller, which has a phase interleaving function, 90 degree phase shift for 4-phase operation, 120 degree phase shift for 3-phase operation and 180 degree phase shift for 2-phase operation which can help reduce output voltage ripple and EMI problem.

Multi-Function Pin Setting Mechanism

For reducing total pin number of package, SET [1:3], TSEN_Main and TSEN_AUXI pins adopt the multi-function pin setting mechanism in the RT3601BC. Figure 4 illustrates this operating mechanism for SET [1:3]. The voltage at VREF pin will be pulled up to 3.2V after power ready (POR). First, external voltage divider is used to set the Function1, and then internal current source 80μA is used to set the Function2. The setting voltage of Function1 and Function2 can be represented as

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{Function2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

All function setting will be done within 500μs after power ready (POR), and the voltage at VREF pin will be fixed to 0.6V after all function setting over.

If $V_{Function1}$ and $V_{Function2}$ are determined, R1 and R2 can be calculated as follows :

$$R1 = \frac{3.2V \times V_{Function2}}{80\mu A \times V_{Function1}}$$

$$R2 = \frac{R1 \times V_{Function1}}{3.2V - V_{Function1}}$$

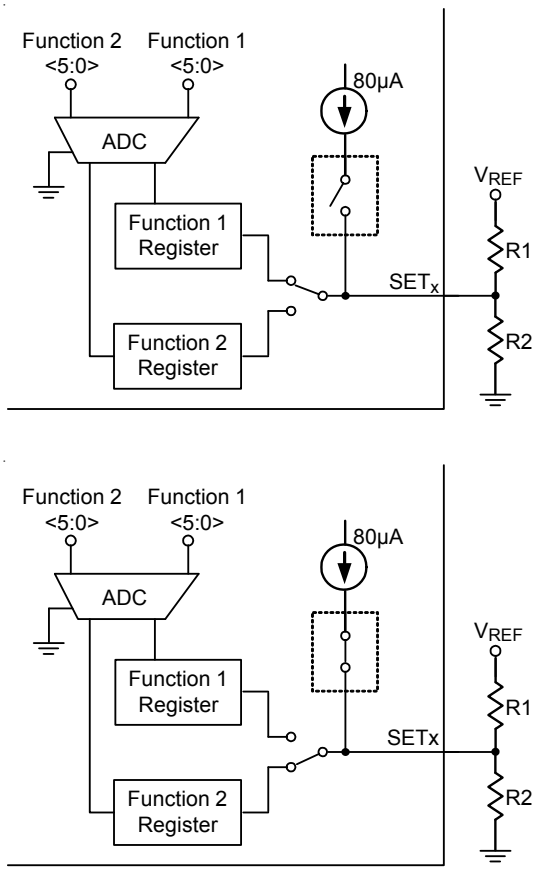


Figure 4. Multi-Function Pin Setting Mechanism for SET [1:3]

Connecting a R3 resistor from SETx pin or SETAx pin to the middle node of voltage divider can help to fine tune the set voltage of Function 2, which does not affect the set voltage of Function1. The Figure 5 shows the setting method and the set voltage of Function 1 and Function2 can be represented as :

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{Function2} = 80\mu A \times \left(R3 + \frac{R1 \times R2}{R1+R2} \right)$$

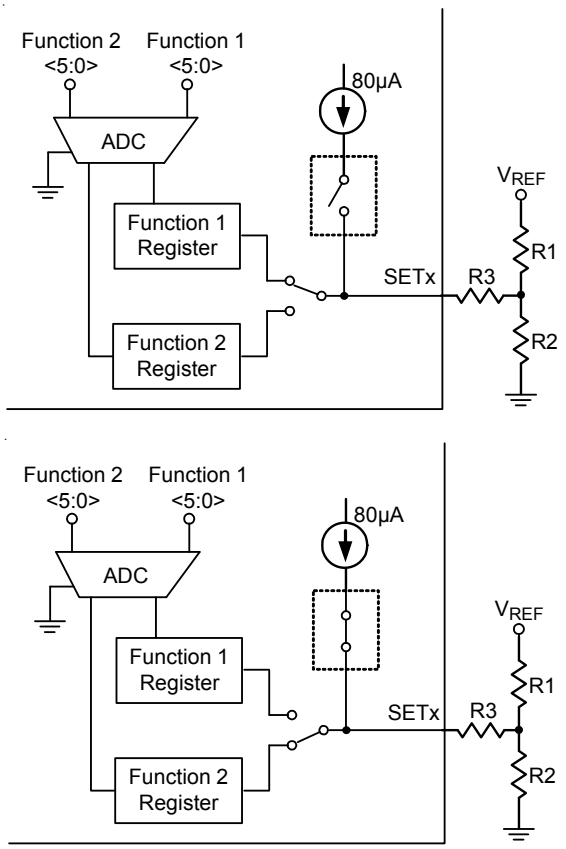


Figure 5. Multi-Function Pin Setting Mechanism with a R3 Resistor to Fine Tune the Set Voltage of Function2

Figure 6 shows operating mechanism for TSEN_Main and TSEN_AUXI pins. There is only voltage divider Function to program VR. The internal current source is used to thermal sensing. The Function for program VR can be represented as

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

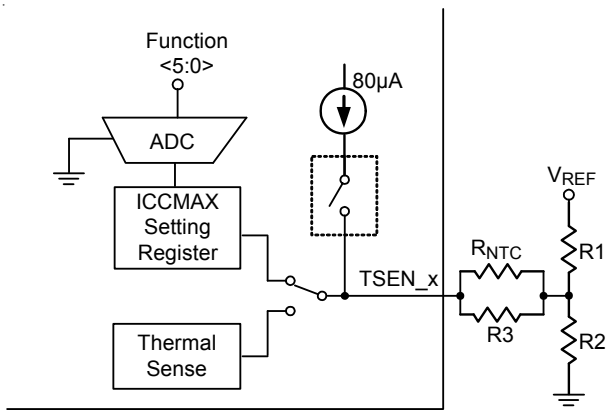


Figure 6. Multi-Function Pin Setting Mechanism for TSEN_ Main and TSEN_ AUXI

By the way, Function1 of SET1, SET2 and SET3 pins are used to program T_{ON} factor and ki gain for each VR rail (Main, AUXI and SA). Function2 of SET1, and SET2 pins are used to program QR threshold and QR width for Main and AUXI VR rails, respectively. Function2 of SET3 pin is used to setting enable/disable anti-overshoot function and tri-state delay time for each rail. SET3 pin also can be set enable/disable zero load-line function for SA rail. TSEN_Main and TSEN_AUXI pins are used to setting DVID threshold and ICCMAX for each VR rail. In addition, Richtek provide a Microsoft Excel-based spreadsheet to help design SETx, TSEN_Main and TSEN_AUXI resistor network.

TSEN_Main, TSEN_AUXI and $\overline{\text{VR\_HOT}}$

The $\overline{\text{VR\_HOT}}$ signal is an open-drain signal which is used for VR thermal protection. When the sensed voltage in each TSEN pin is less than 1.092, the $\overline{\text{VR\_HOT}}$ signal will be pulled-low to notify CPU that the thermal protection needs to work. According to Intel VR definition, $\overline{\text{VR\_HOT}}$ signal needs acting if VR power chain temperature exceeds 100°C. Placing an NTC thermistor at the hottest area in the VR power chain and its connection is shown in Figure 7, to design the TSEN network so that V_{TSEN} = 1.092V at 100°C. The resistance accuracy of TSEN network is recommended to be 1% or higher.

$$V_{TSEN\_X} = 80\mu A \times (R_{NTC} // R3) + (R1 // R2)$$

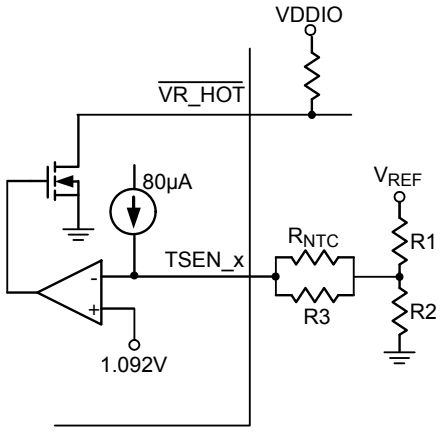


Figure 7. $\overline{\text{VR\_HOT}}$ Circuit

Power Ready (POR) Detection

During start-up, the RT3601BC detects the voltage at the voltage input pins : V_{CC} and EN. When V_{CC}> 4.45V, the RT3601BC recognizes the power state of system to be ready (POR = high) and waits for enable command at the EN pin. After POR = high and V_{EN} > 0.7V, the RT3601BC enters start-up sequence. If V_{CC} drops below low threshold (POR = low), the RT3601BC enters power down sequence and all functions will be disabled. Normally, connecting system voltage V_{TT} (1.05V) to the EN pin is recommended. 2ms (max) after the chip has been enabled, the SVID circuitry will be ready. All the protection latches (OVP, OCP, UVP) will be cleared only by V_{CC}. The condition of VEN = low will not clear these latches. Figure 8 and Figure 9 show the POR detection and the timing chart for POR process, respectively.

Under-Voltage Lockout (UVLO)

During normal operation, if the voltage at the VCC pin drops below POR threshold 4.14V (min), the VR triggers UVLO. The UVLO protection forces all high-side MOSFETs and low-side MOSFETs off by shutting down internal PWM logic drivers.

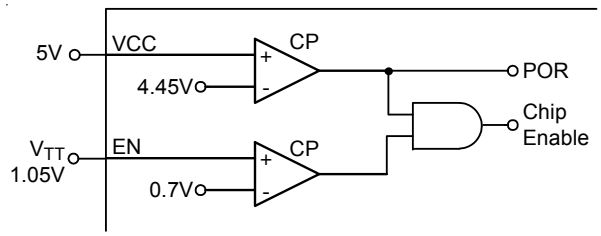


Figure 8. POR Detection

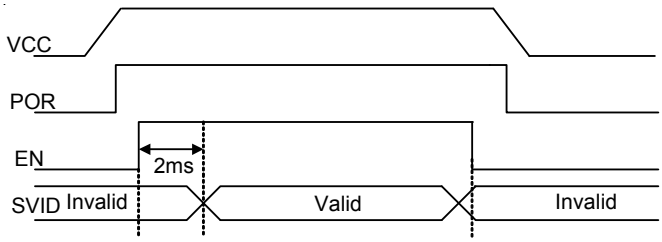


Figure 9. Timing Chart for POR Process

Phase Disable (Before POR)

The number of active phases is determined by the internal circuitry that monitors the ISENxN voltages during startup. Normally, the AUXI rail operates as a 2-phase PWM controller. Pulling ISEN2N to VCC programs a 1-phase operation. Before POR, VR detects whether the voltage of ISEN2N is higher than "VCC – 1V" to decide how many phases should be active. Phase selection is only active during POR. When POR = high, the number of active phases is determined and latched. The unused ISENxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

Switching Frequency Setting

The RT3601BC is one kind of constant on-time control. The patented CCRCOT (Constant Current Ripple COT) technology can generate an adaptive on-time with input voltage and VID code to obtain a constant current ripple, so that the output voltage ripple can be controlled nearly like a constant as different input and output voltages change.

The Ton equation can be classified as below two regions.

$$V_{DAC} \geq 0.7$$

$$T_{ON} = \frac{1.2\mu \times V_{DAC}}{k_{TON} \times (V_{IN} - V_{DAC})} + 15n$$

$$V_{DAC} < 0.7$$

$$T_{ON} = \frac{0.84\mu}{k_{TON} \times (V_{IN} - V_{DAC})} + 15n$$

where k_{TON} is a coefficient which can be selected by SET[1:3] pins for each VR rail. Table 2 and Table 3 show the k_{TON} coefficient and ki gain setting for each VR rail on the SET[1:3] pins.

Table 2. SET[1 and 3] Pins Setting for k_{TON} and ki gain

$V_{SET[1\ and\ 3]\_V} = V_{REF} \times \frac{R2}{R1+R2}$				TONSET_X	AI_X	
Min	**Typical**	**Max**	**Unit**		**Main**	**SA**
60.073314	75.073314	90.073314	mV	0.6	20	NA
110.12219	125.12219	140.12219	mV		NA	40
160.17107	175.17107	190.17107	mV		80	NA
260.26882	275.26882	290.26882	mV	0.8	20	NA
310.31769	325.31769	340.31769	mV		NA	40
360.36657	375.36657	390.36657	mV		80	NA
460.46432	475.46432	490.46432	mV	1.1	20	NA
510.5132	525.5132	540.5132	mV		NA	40
560.56207	575.56207	590.56207	mV		80	NA
660.65982	675.65982	690.65982	mV	1.4	20	NA
710.7087	725.7087	740.7087	mV		NA	40
760.75758	775.75758	790.75758	mV		80	NA
860.85533	875.85533	890.85533	mV	1.7	20	NA
910.9042	925.9042	940.9042	mV		NA	40
960.95308	975.95308	990.95308	mV		80	NA
1061.0508	1076.0508	1091.0508	mV	2	20	NA
1111.0997	1126.0997	1141.0997	mV		NA	40
1161.1486	1176.1486	1191.1486	mV		80	NA
1261.2463	1276.2463	1291.2463	mV	2.3	20	NA
1311.2952	1326.2952	1341.2952	mV		NA	40
1361.3441	1376.3441	1391.3441	mV		80	NA
1461.4418	1476.4418	1491.4418	mV	0.4	20	NA
1511.4907	1526.4907	1541.4907	mV		NA	40
1561.5396	1576.5396	1591.5396	mV		80	NA

*NA represent not applicable.

Table 3. SET2 Pin Setting for k_{TON} and ki gain

$V_{SET2\_V} = V_{REF} \times \frac{R2}{R1+R2}$				TONSET_X	AI_X
Min	**Typical**	**Max**	**Unit**		**AUXI**
110.12219	125.12219	140.12219	mV	0.6	1
160.17107	175.17107	190.17107	mV		2
310.31769	325.31769	340.31769	mV	0.8	1
360.36657	375.36657	390.36657	mV		2
510.5132	525.5132	540.5132	mV	1.1	1
560.56207	575.56207	590.56207	mV		2
710.7087	725.7087	740.7087	mV	1.4	1
760.75758	775.75758	790.75758	mV		2
910.9042	925.9042	940.9042	mV	1.7	1
960.95308	975.95308	990.95308	mV		2
1111.0997	1126.0997	1141.0997	mV	2	1
1161.1486	1176.1486	1191.1486	mV		2
1311.2952	1326.2952	1341.2952	mV	2.3	1
1361.3441	1376.3441	1391.3441	mV		2
1511.4907	1526.4907	1541.4907	mV	0.4	1
1561.5396	1576.5396	1591.5396	mV		2

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$F_{SW(MAX)} = \frac{VID1 + \frac{IccTDC}{N}\cdot\left(DCR + \frac{R_{ON\_LS,max}}{n_{LS}} - N\cdot R_{LL}\right)}{\left[V_{IN(MAX)} + \frac{IccTDC}{N}\cdot\left(\frac{R_{ON\_LS,max}}{n_{LS}} - \frac{R_{ON\_HS,max}}{n_{HS}}\right)\right]\cdot\left(T_{ON} - T_D + T_{ON,VAR}\right) + \frac{IccTDC}{N}\cdot\left(\frac{R_{ON\_LS,max}}{n_{LS}}\right)\cdot T_D}$$

where $F_{SW(MAX)}$ is the maximum switching frequency, VID1 is the typical VID of application, $V_{IN(MAX)}$ is the maximum application input voltage, IccTDC is the thermal design current of application, N is the phase number. The $R_{ON\_HS,max}$ is the maximum equivalent high-side $R_{DS(ON)}$, and n_{HS} is the number of high-side MOSFETs ; $R_{ON\_LS,max}$ is the maximum equivalent low-side $R_{DS(ON)}$, and n_{LS} is the number of low-side MOSFETs. T_D is the summation of the high-side MOSFET delay time and the rising time, $T_{ON,\ VAR}$ is the T_{ON} variation value. DCR is the inductor DCR, and R_{LL} is the loadline setting. In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the R_{TON} for RT3601BC.

When load increases, on-time keeps constant. The off-time width will be reduced so that loading can load more power from input terminal to regulate output voltage. Hence, the loading current usually increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related loss increases, vice versa.

Current Sense

In the RT3601BC, the current signal is used for load-line setting and over-current protection (OCP). The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in Figure 10. If RC network time constant matches inductor time constant L_x/DCR_x, an expected load transient waveform can be designed. If R_xC_x network time constant is larger than inductor time constant L_x/DCR_x, V_{CORE} waveform has a sluggish droop during load transient. If R_xC_x network is smaller than inductor time constant L_x/DCR_x, a worst V_{CORE} waveform will sag to create an undershooting to fail the specification. Figure 11 shows the variety R_xC_x constant corresponding to the output waveforms.

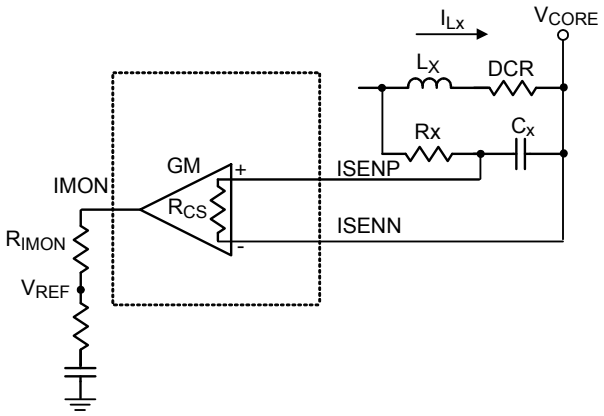


Figure 10. Lossless Current Sense Method for Single Phase

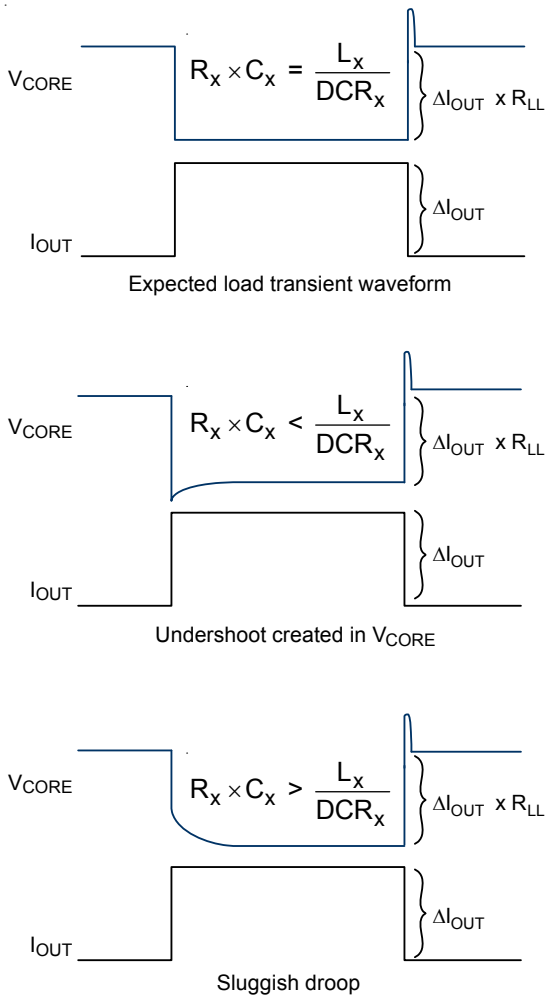


Figure 11. All Kind of R_xC_x Constants

For dual phase current sense is demonstrated as Figure 12. It is similar to single phase method and it also can be extended to N phase application. In RT3601BC design, the resistance of R_{CS} is equal to 2.15kΩ.

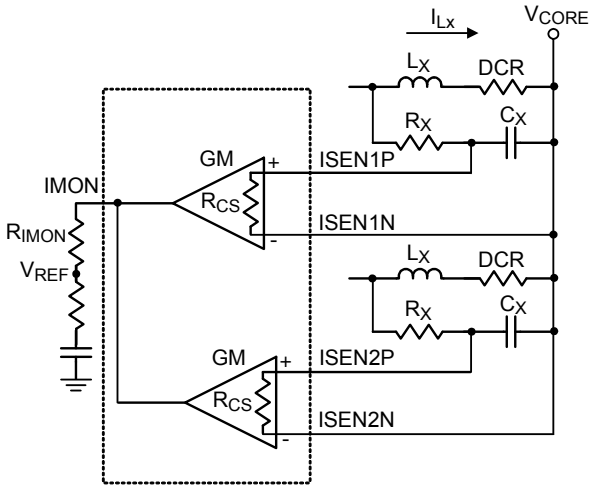


Figure 12. Lossless Current Sense Method for Dual Phase

Thermal Compensation for Current Sense

Since the copper wire of inductor has a positive temperature coefficient. And hence, temperature compensation is necessary for the lossless inductor current sense. For single phase thermal compensation, Figure 13. shows a not only simple but also effective way to compensate temperature variation. An NTC thermistor is put in the current sensing network and it can be used to compensate DCR variation due to temperature is changed.

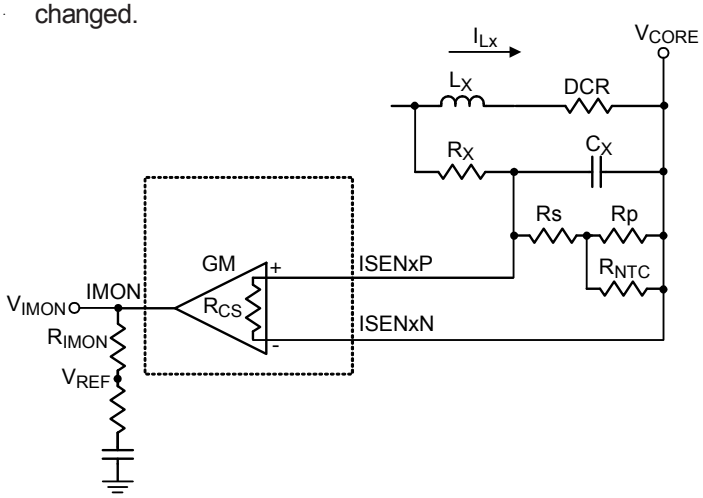


Figure 13. Thermal Compensation method for Single Phase

The current sense network equation is as follows :

$$\Delta V_{IMON} = V_{IMON} - V_{REF} = \frac{I_{LX} \times DCR \times \frac{R_S + (R_P // R_{NTC})}{R_X + (R_S + R_P // R_{NTC})}}{R_{CS}} \times R_{IMON}$$

Usually, R_P is set equal to R_{NTC} (25°C). R_S is selected to linearize the NTC's temperature characteristic. For a given NTC, design is to get R_X and R_S to compensate the temperature variation of the sense resistor.

Let

$$R_{EQU} = R_S + (R_P // R_{NTC})$$

According to current sense network, the corresponding equation is represented as follows :

$$\frac{L_X}{DCR} = C_X \times \frac{R_{EQU} \times R_X}{R_{EQU} + R_X}$$

Next, let

$$m = \frac{L_X}{DCR \times C_X}$$

Then

$$m \times \left(R_X + R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right) = R_X \times \left(R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right)$$

Step1 : Given the two system temperature T_R and T_H at which are compensated.

Step2 : Two equations can be listed as

$$m(T_R) \times \left(R_X + R_S + \frac{R_{NTC}(T_R) \times R_P}{R_{NTC}(T_R) + R_P} \right) = R_X \times \left(R_S + \frac{R_{NTC}(T_R) \times R_P}{R_{NTC}(T_R) + R_P} \right)$$

$$m(T_H) \times \left(R_X + R_S + \frac{R_{NTC}(T_H) \times R_P}{R_{NTC}(T_H) + R_P} \right) = R_X \times \left(R_S + \frac{R_{NTC}(T_H) \times R_P}{R_{NTC}(T_H) + R_P} \right)$$

Step3 : Usually R_P is set to equal to $R_{NTC}(T_R)$. And hence, there are two equations and two unknowns, R_X and R_S can be found out.

Above thermal compensation method needs a NTC resistor in each phase. In order to reduce the NTC amount for multi-phase application, another thermal compensation method is presented. This method can be applied to multi-phase application and it only needs one NTC resistor. So, the NTC resistor cost can be saved by using this method. Figure 14 shows the thermal compensation method for dual phase.

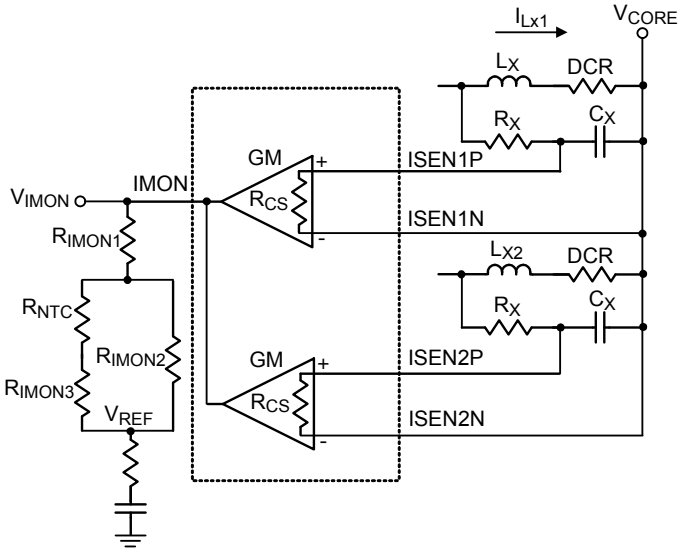


Figure 14. Thermal Compensation method for dual Phase

The current sense network equation is as follows :

$$V_{IMON} - V_{ref} = \frac{\sum_{X=1}^{2} I_{LX} \times DCR}{R_{CS}} \times \{R_{IMON1} + [R_{IMON2} // (R_{IMON3} + R_{NTC})]\}$$

Please note that V_{IMON} is equal to 1V for single phase application and V_{IMON} is equal to 1.4V for dual phase application under ICCMAX condition.

A resistor network with NTC thermistor compensation connecting between IMON pin and VREF pin is used to compensate the positive temperature coefficient of inductor DC. The design flow is as follows :

Step1: Given the three temperature T_L, T_R and T_H, at which are compensated.

Step 2 : Three equations can be listed as

$$\frac{DCR(T_L)}{R_{CS}} = \sum_{i=1}^{2} I_{Li} \times R_{IMON}(T_L) = 0.4$$

$$\frac{DCR(T_R)}{R_{CS}} = \sum_{i=1}^{2} I_{Li} \times R_{IMON}(T_R) = 0.4$$

$$\frac{DCR(T_H)}{R_{CS}} = \sum_{i=1}^{2} I_{Li} \times R_{IMON}(T_H) = 0.4$$

Where :

(1) The relationship between DCR and temperature is as follows :

$$DCR(T) = DCR(25°C) \times [1 + 0.00393(T-25)]$$

(2) $R_{IMON}(T)$ is the equivalent resistor of the resistor network with a NTC thermistor

$$R_{IMON}(T) = R_{IMON1} + \{R_{IMON2} // [R_{IMON3} + R_{NTC}(T)]\}$$

And the relationship between NTC and temperature is as follows :

$$R_{NTC}(T) = R_{NTC}(25°C) \times e^{\beta(\frac{1}{T+273} - \frac{1}{298})}$$

β is in the NTC thermistor datasheet.

Step 3 : Three equation and three unknowns, R_{IMON1}, R_{IMON2} and R_{IMON3} can be calculated out unique solution.

$$R_{IMON1} = K_{TR} - \frac{R_{IMON2} \times (R_{NTCTR} + R_{IMON3})}{R_{IMON2} + R_{NTCTR} + R_{IMON3}}$$

$$R_{IMON2} = \sqrt{[K_{R3}^2 + K_{R3}(R_{NTCTL} + R_{NTCTR}) + R_{NTCTL}R_{NTCTR}]\alpha_{TL}}$$

$$R_{IMON3} = -R_{IMON2} + K_{R3}$$

Where :

$$\alpha_{TH} = \frac{K_{TH} - K_{TR}}{R_{NTCTH} - R_{NTCTR}}$$

$$\alpha_{TL} = \frac{K_{TL} - K_{TR}}{R_{NTCTL} - R_{NTCTR}}$$

$$K_{R3} = \frac{(\alpha_{TH}/\alpha_{TL})R_{NTCTH} - R_{NTCTL}}{1 - (\alpha_{TH}/\alpha_{TL})}$$

$$K_{TL} = \frac{0.4}{\frac{DCR(T_L)}{R_{CS}} \times I_{CCMAX}}$$

$$K_{TR} = \frac{0.4}{\frac{DCR(T_R)}{R_{CS}} \times I_{CCMAX}}$$

$$K_{TH} = \frac{0.4}{\frac{DCR(T_H)}{R_{CS}} \times I_{CCMAX}}$$

Current Monitor, IMON

For each VR rail, the RT3601BC includes a current monitor (IMON) function which can be used to detect over-current protection and maximum processor current ICCMAX, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMON and VREF pins.

Load-Line (Droop) Setting

The G-NAVP™ topology can set load-line (droop) via the current loop and voltage loop, the load-line is a slope between load current I_{CC} and output voltage Vsen as shown in Figure 15. Figure 16 shows the voltage control and current loop for Main and SA rails. By using both loops, the load-line (droop) can be set easily. The load-line set equation for Main and SA is :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{k_i}{2} \times \frac{DCR}{R_{CS}} \times R_{OUT}}{\frac{R_2}{R_1}} = \frac{\frac{k_i}{2} \times DCR}{\frac{R_2}{R_1}} \ (m\Omega)$$

where $R_{OUT} = R_{CS}$

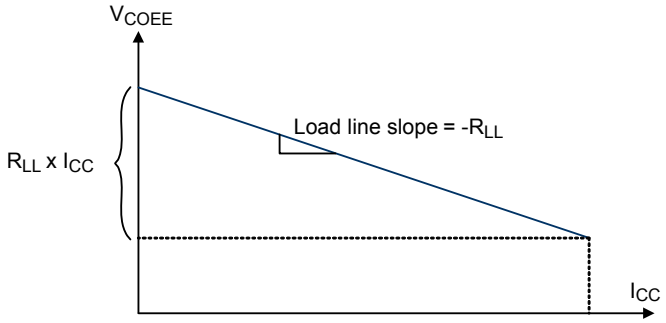


Figure 15. Load-Line (Droop)

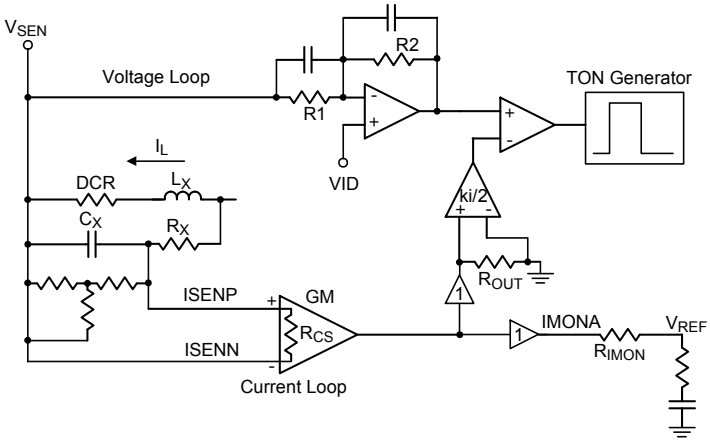


Figure 16. Voltage Loop and Current Loop for Main and SA Rails

Figure 17 shows the voltage control and current loop for AUXI rail. By using both loops, the load-line (droop) can be set easily. The load-line set equation for AUXI is :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{k_i}{2} \times \frac{DCR}{R_{CS}} \times R_{IMON}}{\frac{R_2}{R_1}}$$

Where R_{CS} = 2.15kΩ

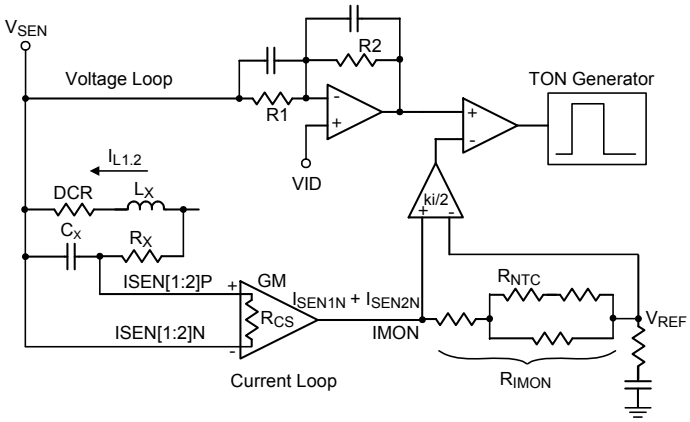


Figure 17. Voltage Loop and Current Loop for AUXI

The ki gain can be selected by SET [1:3] pins for individual rail.

Compensator Design

The compensator of RT3601BC doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP™ topology to achieve constant output impedance design for Intel IMVP8 ACLL specification. The one pole one zero compensator is shown as Figure 18. The transfer function of compensator should be design as following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range :

$$G_{CON}(S) \approx \frac{A_I}{R_{LL}} \frac{1 + \frac{s}{\omega \times fsw}}{1 + \frac{s}{\omega ESR}}$$

where A_I is current loop gain, R_{LL} is load-line, f_{SW} is switching frequency and ω_{ESR} is a pole that should be located at 1/(C_{OUT} x ESR). Then, the C1 and C2 should be designed as follows :

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \qquad C2 = \frac{C_{OUT} \times ESR}{R2}$$

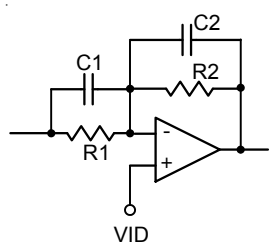


Figure 18. Type I compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts for Main and AUXI rails. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE} and connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier as shown in Figure 19. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

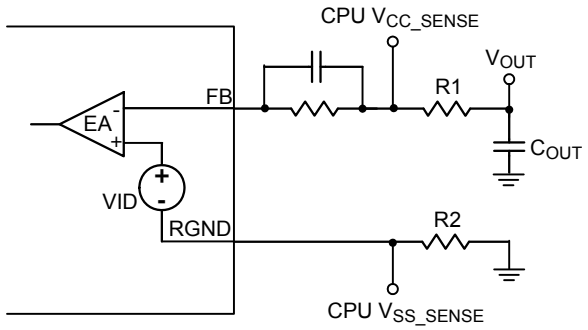


Figure 19. Remote Sensing Circuit

Maximum Processor Current Setting, IMAX

The maximum processor current IMAX for each VR rail can be set by TSEN_Main and TSEN_ AUXI pins. Each VR IMAX register is set by an external voltage divider with the multi-function mechanism. Table 4 and Table 5 show the each VR IMAX setting on TSEN_Main and TSEN_ AUXI pins.

Table 4. TSEN_Main Setting for DVIDTH_SA, IMAX_AUXI and IMAX_SA

$V_{TSEN\_Main} = V_{REF} \times \frac{R2}{R1+R2}$				DVIDTH_SA (mV)	IMAX_AUXI (A)	IMAX_SA (A)
Min	Typical	Max	Unit			
35.0489	50.0489	65.0489	mV	15	28 (SPIKE-OCP = 3X)	6 (SPIKE-OCP = 6X)
135.147	150.147	165.147	mV			8 (SPIKE-OCP = 6X)
235.244	250.244	265.244	mV		36 (SPIKE-OCP = 3X)	6 (SPIKE-OCP = 6X)
335.342	350.342	365.342	mV			8 (SPIKE-OCP = 6X)
435.44	450.44	465.44	mV		60 (SPIKE-OCP = 2X)	6 (SPIKE-OCP = 6X)
535.538	550.538	565.538	mV			8 (SPIKE-OCP = 6X)
635.635	650.635	665.635	mV		68 (SPIKE-OCP = 2X)	6 (SPIKE-OCP = 6X)
735.733	750.733	765.733	mV			8 (SPIKE-OCP = 6X)
835.831	850.831	865.831	mV	30	28 (SPIKE-OCP = 3X)	6 (SPIKE-OCP = 6X)
935.929	950.929	965.929	mV			8 (SPIKE-OCP = 6X)
1036.03	1051.03	1066.03	mV		36 (SPIKE-OCP = 3X)	6 (SPIKE-OCP = 6X)
1136.12	1151.12	1166.12	mV			8 (SPIKE-OCP = 6X)
1236.22	1251.22	1266.22	mV		60 (SPIKE-OCP = 2X)	6 (SPIKE-OCP = 6X)
1336.32	1351.32	1366.32	mV			8 (SPIKE-OCP = 6X)
1436.42	1451.42	1466.42	mV		68 (SPIKE-OCP = 2X)	6 (SPIKE-OCP = 6X)
1536.52	1551.52	1566.52	mV			8 (SPIKE-OCP = 6X)
1636.61	1651.61	1666.61	mV	60	28 (SPIKE-OCP = 3X)	6 (SPIKE-OCP = 6X)
1736.71	1751.71	1766.71	mV			8 (SPIKE-OCP = 6X)
1836.81	1851.81	1866.81	mV		36 (SPIKE-OCP = 3X)	6 (SPIKE-OCP = 6X)
1936.91	1951.91	1966.91	mV			8 (SPIKE-OCP = 6X)
2037	2052	2067	mV		60 (SPIKE-OCP = 2X)	6 (SPIKE-OCP = 6X)
2137.1	2152.1	2167.1	mV			8 (SPIKE-OCP = 6X)
2237.2	2252.2	2267.2	mV		68 (SPIKE-OCP = 2X)	6 (SPIKE-OCP = 6X)
2337.3	2352.3	2367.3	mV			8 (SPIKE-OCP = 6X)
2437.39	2452.39	2467.39	mV	90	28 (SPIKE-OCP = 3X)	6 (SPIKE-OCP = 6X)
2537.49	2552.49	2567.49	mV			8 (SPIKE-OCP = 6X)
2637.59	2652.59	2667.59	mV		36 (SPIKE-OCP = 3X)	6 (SPIKE-OCP = 6X)
2737.69	2752.69	2767.69	mV			8 (SPIKE-OCP = 6X)
2837.79	2852.79	2867.79	mV		60 (SPIKE-OCP = 2X)	6 (SPIKE-OCP = 6X)
2937.88	2952.88	2967.88	mV			8 (SPIKE-OCP = 6X)
3037.98	3052.98	3067.98	mV		68 (SPIKE-OCP = 2X)	6 (SPIKE-OCP = 6X)
3138.08	3153.08	3168.08	mV			8 (SPIKE-OCP = 6X)

Table 5. TSEN_AUXI Setting for DVIDTH_AUXI, DVIDTH_Main and IMAX_Main

$V_{TSEN\_AUXI} = V_{REF} \times \frac{R2}{R1+R2}$				DVIDTH_AUXI (mV)	DVIDTH_Main (mV)	IMAX_Main (A)
Min	Typical	Max	Unit			
35.0489	50.0489	65.0489	mV	15	15	29 (SPIKE-OCP = 3X)
135.147	150.147	165.147	mV			35 (SPIKE-OCP = 2X)
235.244	250.244	265.244	mV		30	29 (SPIKE-OCP = 3X)
335.342	350.342	365.342	mV			35 (SPIKE-OCP = 2X)
435.44	450.44	465.44	mV		60	29 (SPIKE-OCP = 3X)
535.538	550.538	565.538	mV			35 (SPIKE-OCP = 2X)
635.635	650.635	665.635	mV		90	29 (SPIKE-OCP = 3X)
735.733	750.733	765.733	mV			35 (SPIKE-OCP = 2X)
835.831	850.831	865.831	mV	30	15	29 (SPIKE-OCP = 3X)
935.929	950.929	965.929	mV			35 (SPIKE-OCP = 2X)
1036.03	1051.03	1066.03	mV		30	29 (SPIKE-OCP = 3X)
1136.12	1151.12	1166.12	mV			35 (SPIKE-OCP = 2X)
1236.22	1251.22	1266.22	mV		60	29 (SPIKE-OCP = 3X)
1336.32	1351.32	1366.32	mV			35 (SPIKE-OCP = 2X)
1436.42	1451.42	1466.42	mV		90	29 (SPIKE-OCP = 3X)
1536.52	1551.52	1566.52	mV			35 (SPIKE-OCP = 2X)
1636.61	1651.61	1666.61	mV	60	15	29 (SPIKE-OCP = 3X)
1736.71	1751.71	1766.71	mV			35 (SPIKE-OCP = 2X)
1836.81	1851.81	1866.81	mV		30	29 (SPIKE-OCP = 3X)
1936.91	1951.91	1966.91	mV			35 (SPIKE-OCP = 2X)
2037	2052	2067	mV		60	29 (SPIKE-OCP = 3X)
2137.1	2152.1	2167.1	mV			35 (SPIKE-OCP = 2X)
2237.2	2252.2	2267.2	mV		90	29 (SPIKE-OCP = 3X)
2337.3	2352.3	2367.3	mV			35 (SPIKE-OCP = 2X)
2437.39	2452.39	2467.39	mV	90	15	29 (SPIKE-OCP = 3X)
2537.49	2552.49	2567.49	mV			35 (SPIKE-OCP = 2X)
2637.59	2652.59	2667.59	mV		30	29 (SPIKE-OCP = 3X)
2737.69	2752.69	2767.69	mV			35 (SPIKE-OCP = 2X)
2837.79	2852.79	2867.79	mV		60	29 (SPIKE-OCP = 3X)
2937.88	2952.88	2967.88	mV			35 (SPIKE-OCP = 2X)
3037.98	3052.98	3067.98	mV		90	29 (SPIKE-OCP = 3X)
3138.08	3153.08	3168.08	mV			35 (SPIKE-OCP = 2X)

Dynamic VID (DVID) Compensation

When VID transition event occurs, a charge current will be generated in the loop to cause DVID performance is deteriorated by this induced charge current, the phenomenon is called droop effect. The droop effect is shown in Figure 20. When VID up transition occurs, the output capacitor will be charged by inductor current. Since current signal is sensed in inductor, an induced charge current will appear in control loop. The induced charge current will produce a voltage drop in R1 to cause output voltage to have a droop effect. Due to this, VID transition performance will be deteriorated.

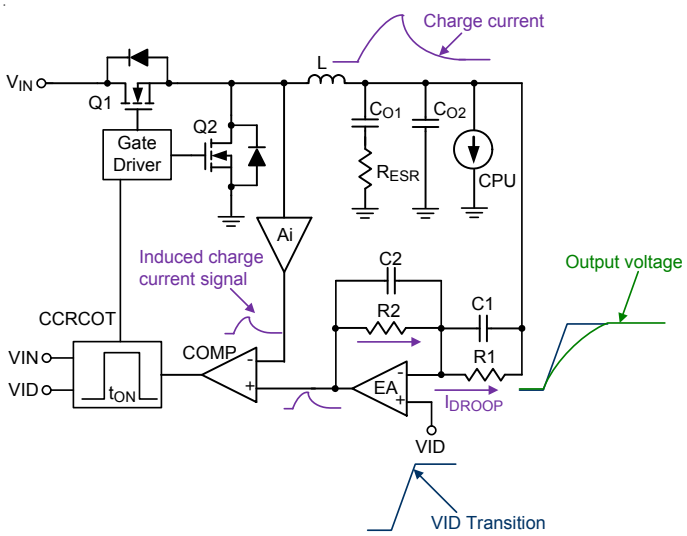


Figure 20. Droop Effect in VID transition

The RT3601BC provides a DVID compensation function. By the DVID compensation to cancel the real induced charge current signal and the virtual charge current signal is defined in Figure 21. Figure 22 shows the operation of cancelling droop effect. A virtual charge current signal is established first and then VID signal plus virtual charge current signal to be generated on the FB pin. Hence, an induced charge current signal flows to R1 and is cancelled to reduce droop effect.

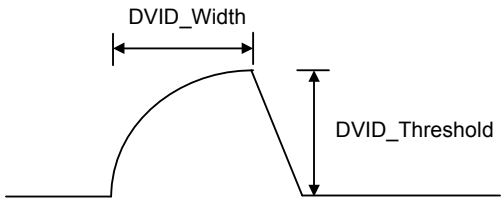


Figure 21. Definition of Virtual Charge Current Signal

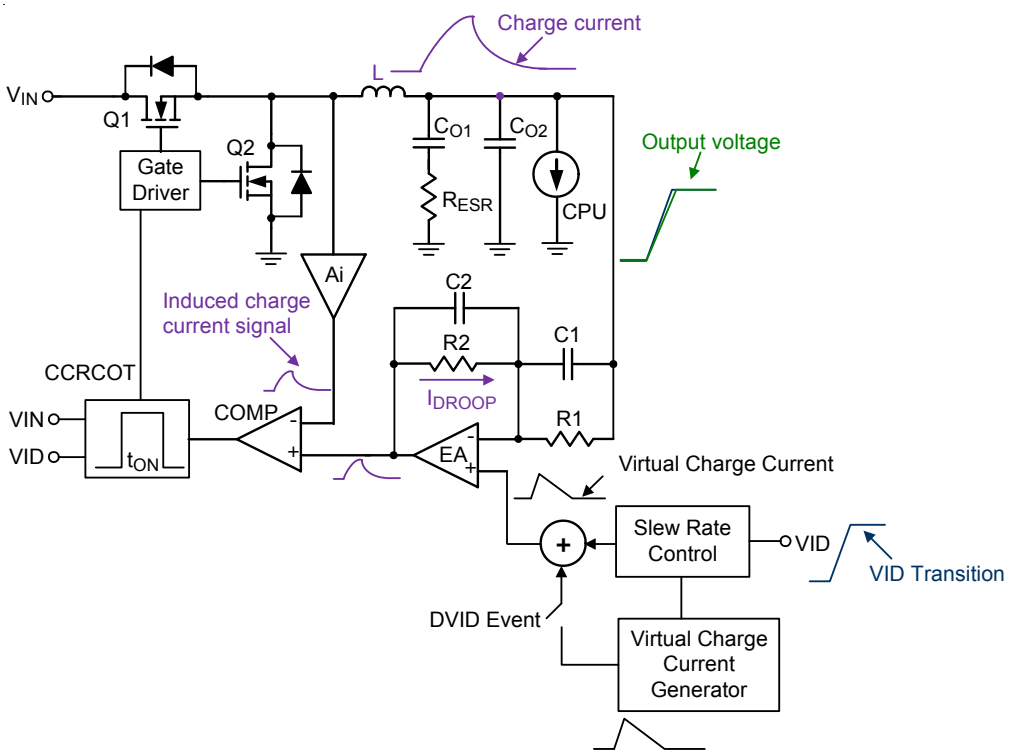


Figure 22. DVID Compensation

Table 4 and Table 5 show the each VR DVID threshold setting on TSEN_Main and TSEN_ AUXI pins. The each VR DVID width is equal to 2µs. For example, VR IMAXs are 34A, 6A and 40A for Main rail, SA rail and AUXI rail, respectively. And DIVDTHs are all set as 15mV for each rail. The V_{TSEN_Main} and V_{TSEN_AUXI} need to be set as 0.25V and 0.15V, respectively. Please note that a high accuracy resistor is needed for this setting, <1% error tolerance is recommended.

Ramp Compensation

The G-NAVP™ topology is one type of ripple based control that has fast transient response and can lower BOM cost. However, ripple based control usually has no good noise immunity. The RT3601BC provides the ramp compensation to increase noise immunity and reduce jitter at the switching node. Figure 23 shows the ramp compensation.

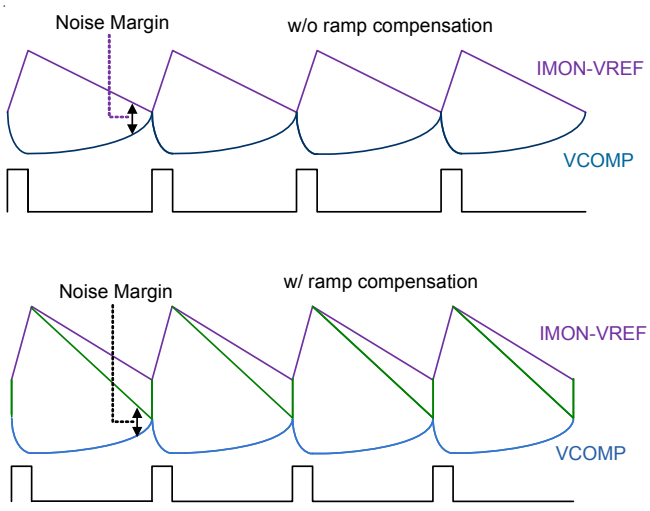


Figure 23. Ramp Compensation

Quick Response (QR) Mechanism

When the transient load step-up becomes quite large, it is difficult for loop response to meet the energy transfer. Hence, that output voltage generate undershoot to fail specification. The RT3601BC has Quick Response (QR) mechanism being able to improve this issue. It adopts a nonlinear control mechanism which can disable interleaving function and simultaneously turn on all UGATE one pulse at instantaneous step-up transient load to restrain the output voltage drooping. Figure 24 shows the QR behavior.

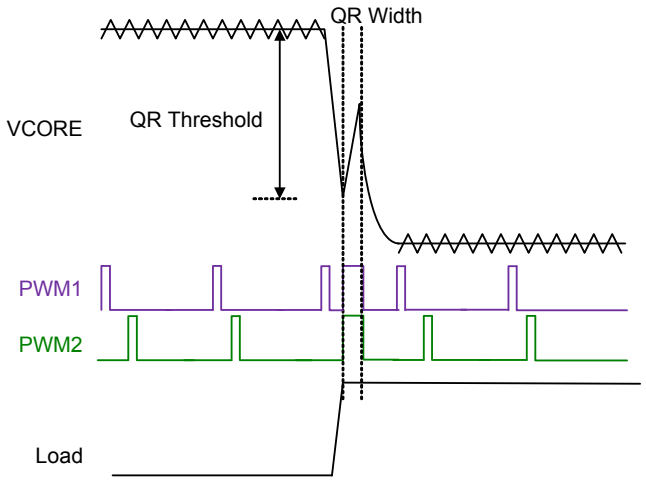


Figure 24. Quick Response Mechanism

The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at the VSEN pin which is shown in Figure 25. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 24. A proper QR mechanism set can meet different applications. The SET1 and SET2 pins can set QR threshold and QR width by internal current source 80μA with multi-function pin setting mechanism for Main and AUXI VR rails. Table 6 shows the QR_TH and QR_WIDTH for Main and AXUI VR rails on the SET[1:2] pins.

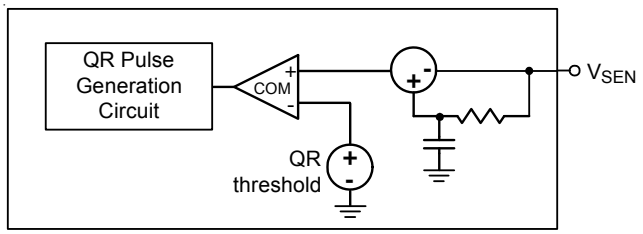


Figure 25. Simplified QR Trigger schematic

Table 6. SET[1:2] pins setting for QR Threshold and QR Width

$V_{SET[1:2]\_I} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$				QRTH_X (mV)		QRWIDTH_X (% of On-Time)
Min	Typical	Max	Unit	PS0	PS1	
10.0244	25.0244	40.0244	mV	Disable	Disable	160%
60.0733	75.0733	90.0733	mV			130%
110.122	125.122	140.122	mV			100%
160.171	175.171	190.171	mV			70%
210.22	225.22	240.22	mV	10	10	160%
260.269	275.269	290.269	mV			130%
310.318	325.318	340.318	mV			100%
360.367	375.367	390.367	mV			70%
410.415	425.415	440.415	mV	15	15	160%
460.464	475.464	490.464	mV			130%
510.513	525.513	540.513	mV			100%
560.562	575.562	590.562	mV			70%
610.611	625.611	640.611	mV	20	20	160%
660.66	675.66	690.66	mV			130%
710.709	725.709	740.709	mV			100%
760.758	775.758	790.758	mV			70%
810.806	825.806	840.806	mV	25	25	160%
860.855	875.855	890.855	mV			130%
910.904	925.904	940.904	mV			100%
960.953	975.953	990.953	mV			70%
1011	1026	1041	mV	30	30	160%
1061.05	1076.05	1091.05	mV			130%
1111.1	1126.1	1141.1	mV			100%
1161.15	1176.15	1191.15	mV			70%
1211.2	1226.2	1241.2	mV	35	35	160%
1261.25	1276.25	1291.25	mV			130%
1311.3	1326.3	1341.3	mV			100%
1361.34	1376.34	1391.34	mV			70%
1411.39	1426.39	1441.39	mV	40	40	160%
1461.44	1476.44	1491.44	mV			130%
1511.49	1526.49	1541.49	mV			100%
1561.54	1576.54	1591.54	mV			70%

For example, 35mV QR threshold and 1.3 x TON QR width are set. According to Table 6, the set voltage should be between 1.261V and 1.291V. Please note that a high accuracy resistor is needed for this setting accuracy, <1% error tolerance is recommended.

Zero Load-Line Setting and Anti-overshoot function

The SET3 pin can be enabled/disabled zero load-line function for SA rail and can be enabled/disabled anti-overshoot function for each VR rail. Table 7 show the zero load-line function for SA rail and anti-overshoot function for each VR rail on the SET3 pin.

When DVID slew rate increases, loop response is difficult to meet energy transfer so that output voltage generates overshoot to fail specification. The RT3601BC has anti-overshoot function being able to help improve this issue. The VR will turn off low-side MOSFET when output voltage ramps up to the target VID (ALERT signal be pulled low). This function also can improve the overshoot during the load transient condition. When anti-overshoot function is triggered, the UGATE and LGATE signal will be masked to reduce the overshoot amplitude.

In order to increase high power density performance, Dr.MOS is popular to use in VR application. Dr.MOS usually has the tri-state delay time, that is to say, PWM output will be hold last state during tri-state delay time. This behavior will cause larger on-time than normal condition at PWM output is high to tri-state. So RT3601BC provide a function to improve this drawback, the SET3 pin can be set enable/disable tri-state delay function. PWM output will be hold-off during tri-state delay time when tri-state function is enabled.

Table 7. SET3 Pin Setting for anti-overshoot and zero load-line

$V_{SET3\_I} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$				ANTIOVS			SA_0LL	Tri-state delay
Min	Typical	Max	Unit	CORE	GT	SA		
10.02443793	25.02443793	40.02443793	mV	Disable	Disable	Disable	Disable	Disable
60.07331378	75.07331378	90.07331378	mV					Enable
110.1221896	125.1221896	140.1221896	mV				Enable	Disable
160.1710655	175.1710655	190.1710655	mV					Enable
210.2199413	225.2199413	240.2199413	mV			Enable	Disable	Disable
260.2688172	275.2688172	290.2688172	mV					Enable
310.3176931	325.3176931	340.3176931	mV				Enable	Disable
360.3665689	375.3665689	390.3665689	mV					Enable
410.4154448	425.4154448	440.4154448	mV		Enable	Disable	Disable	Disable
460.4643206	475.4643206	490.4643206	mV					Enable
510.5131965	525.5131965	540.5131965	mV				Enable	Disable
560.5620723	575.5620723	590.5620723	mV					Enable
610.6109482	625.6109482	640.6109482	mV			Enable	Disable	Disable
660.659824	675.659824	690.659824	mV					Enable
710.7086999	725.7086999	740.7086999	mV				Enable	Disable
760.7575758	775.7575758	790.7575758	mV					Enable

$V_{SET3\_I} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$				ANTIOVS			SA_0LL	Tri-state delay
Min	Typical	Max	Unit	CORE	GT	SA		
810.8064516	825.8064516	840.8064516	mV	Enable	Disable	Disable	Disable	Disable
860.8553275	875.8553275	890.8553275	mV					Enable
910.9042033	925.9042033	940.9042033	mV				Enable	Disable
960.9530792	975.9530792	990.9530792	mV					Enable
1011.001955	1026.001955	1041.001955	mV			Enable	Disable	Disable
1061.050831	1076.050831	1091.050831	mV					Enable
1111.099707	1126.099707	1141.099707	mV				Enable	Disable
1161.148583	1176.148583	1191.148583	mV					Enable
1211.197458	1226.197458	1241.197458	mV		Enable	Disable	Disable	Disable
1261.246334	1276.246334	1291.246334	mV					Enable
1311.29521	1326.29521	1341.29521	mV				Enable	Disable
1361.344086	1376.344086	1391.344086	mV					Enable
1411.392962	1426.392962	1441.392962	mV			Enable	Disable	Disable
1461.441838	1476.441838	1491.441838	mV					Enable
1511.490714	1526.490714	1541.490714	mV				Enable	Disable
1561.539589	1576.539589	1591.539589	mV					Enable

Over-Current Protection

The RT3601BC has dual OCP mechanism. One is named SUM-OCP, the other is called SPIKE-OCP. The over current protection (OCP) forces high-side MOSFET and low-side MOSFET off by shutting down internal PWM logic drivers. RT3601BC provides SUM-OCP which is 160% of IMAX. When output current is higher than the SUM-OCP threshold, SUM-OCP is latched with a 40μs delay time to prevent false trigger. Besides, the SUM-OCP function is masked when dynamic VID transient occurs and after dynamic VID transition, SUM-OCP is masked for 80μs. The other one is SPIKE-OCP which should trip when the output current exceeds SPIKE_OCP threshold during first DVID. SPIKE_OCP threshold is dependent on IMAX level as shown in Table 4 and Table 5. When output current is higher than the SPIKE-OCP threshold, SPIKE-OCP is latched with a 1μs delay time to prevent false trigger.

Output Over-Voltage Protection

An OVP condition is detected when the VSEN pin is 350mV more than VID. When OVP is detected, the high-side gate voltage UGATEx is pulled low and the low-side gate voltage LGATEx is pulled high. OVP is latched with a 0.5μs delay- to prevent false trigger.

Negative Voltage Protection

Since the OVP latch continuously turns on all low-side MOSFETs of the VR, the VR will suffer negative output voltage. When the VSEN detects a voltage below –0.07V after triggering OVP, the VR triggers NVP to turn off all low-side MOSFETs of the VR while the high-side MOSFETs remain off. After triggering NVP, if the output voltage rises above 0V, the OVP latch restarts to turn on all low-side MOSFETs. Therefore, the output voltage may bounce between 0V and –0.07V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered.

Under-Voltage Protection

When the VSEN pin voltage is 350mV less than VID, UVP will be latched. When UVP latched, the both UGATEx and LGATEx are pulled low. A 3µs delay is used in UVP detection circuit to prevent false trigger. Besides, the UVP function is masked when dynamic VID transient occurs and after dynamic VID transition, UVP is masked for 80µs.

Design Step :

RT3601BC Excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. Three main design procedures of RT3601BC design, first step is loop design, second step is pin setting design, and the last step is protection settings. The following design example is to explain RT3601BC design procedure :

Main VR

	V_{Main} Specification
Input Voltage	19V
No. of Phase	1
Normal VID	1.35V
ICCMAX	34
ICC-Dyn	28
Load-Line	2.1mΩ
Fast Slew Rate	37.5mV/µs
MAX Switching Frequency	700kHz

The output filter requirements of VRTB specification are as follows :

Output Inductor : 220nH/0.875mΩ

Output Ceramic Capacitor: 47µF (6pcs)

Output Ceramic Capacitor:10µF (9pcs)

Loop Design :

- On time setting: Using the specification, then can get that T_{ON} is 108ns.

  The k_{TON} parameter can be calculated after the on-time is decided.

$$T_{ON} = \frac{1.7\mu \times V_{DAC}}{k_{TON} \times (V_{IN} - V_{DAC})} + 15n$$

  Choosing the nearest on-time setting k_{TON} = 1.4

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expected load transient waveform R_XC_X time constant needs to match L_X/DCR_X. C_X = 0.47µF, R_{NTC} = 10kΩ and R_P = 10kΩ are set, then

$$R_{EQU} = R_S + (R_P // R_{NTC})$$

$$\frac{L_X}{DCR} = C_X \times \frac{R_{EQU} \times R_X}{R_{EQU} + R_X}$$

  By using the design tool, R_S and R_X can be determined, are equal to 220Ω and 590Ω, respectively.

- IMON resistor network design :

$$R_{IMON} = \frac{\Delta V_{IMON} \times 2.15k}{ICCMAX \times DCR \times \frac{R_{EQU}}{R_X + R_{EQU}}} = 32.17k\Omega$$

- Load-line design : 2.1mΩ droop is requirement, because DCR and ki are decided to 0.875mΩ and 20, respectively. The voltage loop Av gain is also can be determined by following equation :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{k_i}{2} \times DCR}{\frac{R_2}{R_1}}$$

  R_1 = 10kΩ is usually decided and here R2 is chosen to 37.4kΩ.

- Typical compensator design can use the following equations to design C_1 and C_2 values

$$C_1 = \frac{1}{R_1 \times \pi \times F_{SW}} \approx 45.5pF$$

$$C_2 = \frac{C_{OUT} \times ESR}{R_2} \approx 33pF$$

  For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the zero location can be designed close to 1/10 of the switching frequency or less than the 1/10 of switching frequency.

SA VR

	V_{SA} Specification
Input Voltage	19V
No. of Phase	1
Normal VID	1.05V
ICCMAX	6
ICC-Dyn	3
Load-Line	10.3mΩ
Fast Slew Rate	37.5mV/μs
MAX Switching Frequency	800kHz

The output filter requirements of VRTB specification are as follows :

Output Inductor: 820nH/6.7mΩ

Output Ceramic Capacitor: 47μF (4pcs)

Output Ceramic Capacitor:10μF (8pcs)

Loop Design :

- On time setting : Using the specification, then can get that T_{ON} is 96ns.

  The k_{TON} parameter can be calculated after the on-time is decided.

$$T_{ON} = \frac{1.7\mu \times V_{DAC}}{k_{TON} \times (V_{IN} - V_{DAC})} + 15n$$

  Choosing the nearest on-time setting k_{TON} = 1.4

  Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expected load transient waveform R_XC_X time constant needs to match L_X/DCR_X. C_X = 0.47μF, R_{NTC} = 4.7kΩ and Rp = 4.7kΩ are set, then

$$R_{EQU} = R_S + (R_P // R_{NTC})$$

$$\frac{L_X}{DCR} = C_X \times \frac{R_{EQU} \times R_X}{R_{EQU} + R_X}$$

  By using the design tool, R_S and R_X can be determined, are equal to 165Ω and 280Ω, respectively.

- IMON resistor network design :

$$R_{IMON} = \frac{\Delta V_{IMON} \times 2.15k}{ICCMAX \times DCR \times \frac{R_{EQU}}{R_X + R_{EQU}}} = 23.79k\Omega$$

- Load-line design : 10.3mΩ droop is requirement, because DCR and ki are decided to 6.7mΩ and 20, respectively. The voltage loop Av gain is also can be determined by following equation :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{k_i}{2} \times DCR}{\frac{R_2}{R_1}}$$

  R_1 = 10kΩ is usually decided and here R2 is chosen to 58.5kΩ.

  Typical compensator design can use the following equations to design C_1 and C_2 values

$$C_1 = \frac{1}{R_1 \times \pi \times F_{SW}} \approx 45.5pF$$

$$C_2 = \frac{C_{OUT} \times ESR}{R_2} \approx 56pF$$

  For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the zero location can be designed close to 1/10 of the switching frequency or less than the 1/10 of switching frequency.

AVXI VR

	V_{AUXI} Specification
Input Voltage	19V
No. of Phase	1
Normal VID	1.35V
ICCMAX	40
ICC-Dyn	37
Load-Line	3.1mΩ
Fast Slew Rate	37.5mV/μs
MAX Switching Frequency	700kHz

The output filter requirements of VRTB specification are as follows :

Output Inductor: 220nH/0.875mΩ

Output Bulk Capacitor: 330μF/2V.4.5mΩ (1pcs)

Output Ceramic Capacitor: 47μF (6pcs)

Output Ceramic Capacitor: 22μF (7pcs)

Output Ceramic Capacitor:10μF (2pcs)

Loop Design :

- On time setting: Using the specification, then can get that T_{ON} parameter can be calculated after the on-time is decided.

$$T_{ON} = \frac{1.7\mu \times V_{DAC}}{k_{TON} \times (V_{IN} - V_{DAC})} + 15n$$

Choosing the nearest on-time setting k_{TON} = 1.1

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expected load transient waveform R_XC_X time constant needs to match L_X/DCR_X. C_X = 0.47µF is set, then

$$R_X = \frac{L_X}{1\mu F \times DCR_X} = 530\Omega$$

- IMON resistor network design : T_L = 25°C, T_R = 50°C and T_H = 100°C are decided, NTC thermistor = 100kΩ @ 25°C, β = 4485 and ICCMAX = 40A. R_{IMON1} = 22.07kΩ, R_{IMON2} = 41.03kΩ and R_{IMON3} =3 8.3kΩ can be decided. The R_{EQ}(25°C) = 53.71kΩ.

- Load-line design: 3.1mΩ droop is requirement, because DCR and ki are decided to 0.875mΩ and 2, respectively. The voltage loop Av gain is also can be determined by following equation :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{k_i}{2} \times \frac{DCR}{R_{CS}} \times R_{IMON}}{\frac{R_2}{R_1}}$$

R_1 = 10kΩ is usually decided and here R2 is chosen to 64.51kΩ.

- Typical compensator design can use the following equations to design C_1 and C_2 values

$$C_1 = \frac{1}{R_1 \times \pi \times F_{SW}} \approx 45.5pF$$

$$C_2 = \frac{C_{OUT} \times ESR}{R_2} \approx 55pF$$

For intel platform, in order to induce the band width to enhance transient performance to meet intel's criterion, the zero location can be designed close to 1/10 of the switching frequency or less than the 1/10 of switching frequency.

Pin Setting Design :

SET1 resistor network design: From above designs, parameters of k_{TON_Main} and k_{i_Main} are 1.1 and 20, respectively. The Main_QR_TH is set to disable and Main_QR_Width is designed as 0.7 x T_{ON}. By using the information, the two equation can be listed by using multi-function pin setting mechanism :

$$3.2 \times \frac{R_2}{R_1 + R_2} = 675.7mV$$

$$80\mu \times \frac{R_1 \times R_2}{R_1 + R_2} = 175.2mV$$

R_1 = 10.37kΩ and R_2 = 2.78kΩ.

- SET2 resistor network design : From above designs, parameters of k_{TON_AUXI} and k_{i_AUXI} are 1.1 and 2, respectively. The AUXI_QR_TH is set to 15mV and AUXI_QR_Width is designed as 0.7 x T_{ON}. By using the information, the two equation can be listed by using multi-function pin setting mechanism :

$$3.2 \times \frac{R_2}{R_1 + R_2} = 575.56mV$$

$$80\mu \times \frac{R_1 \times R_2}{R_1 + R_2} = 575.56mV$$

R_1 = 40kΩ and R_2 = 8.77kΩ.

- SET3 resistor network design: From above designs, parameters of k_{TON_SA} and k_{i_SA} are 1.4 and 20, respectively. The anti-overshoot function is enabled for Main and AUXI rails. The anti-overshoot function and zero load-line function for SA rail both are disabled. The tri-state delay is disable, too. By using the information, the two equation can be listed by using multi-function pin setting mechanism :

$$3.2 \times \frac{R_2}{R_1 + R_2} = 675.66mV$$

$$80\mu \times \frac{R_1 \times R_2}{R_1 + R_2} = 1276.24mV$$

R_1 = 75.56kΩ and R_2 = 20.22kΩ.

- TSEN_Main resistor network design : The DIVD threshold is 60mV for SA rail. And the IMAXs are designed as 40A and 6A for AUXI rail and SA rail, respectively. By using the information, the equation can be shown as below :

$$3.2 \times \frac{R_2}{R_1 + R_2} = 1.851V$$

- TSEN_AUXI resistor network design : The DIVD thresholds are 15mV and 60mV for Main rail and AUXI rail, respectively. And the IMAX is designed as 34A for

Main rail. By using the information, the equation can be listed by using multi-function pin setting mechanism :

$$3.2\times\frac{R_2}{R_1+R_2}=550mV$$

Protection Settings :

- OVP/UVP protections: When the VSEN pin voltage is 350mV higher than VID, the OVP will be latched. When the VSEN pin voltage is 350mV lower than VID, the UVP will be latched.
- TSEN and $\overline{VR\_HOT}$ design : Using the following equation to calculate related resistances for $\overline{VR\_HOT}$ setting.

$$V_{TSEN}=80\mu\times(R_3//R_{NTC})+(R_1//R_2)$$

Choosing R_1 = 100kΩ and an NTC thermistor $R_{NTC\,(25°C)}$ = 100kΩ and its β = 4485. When temperature is 100°C, the $R_{NTC\,(100°C)}$ = 4.85kΩ. According to TSEN pins for multi-function mechanism, three equations can be got as following for Main VR rail :

$$V_{TSEN\_Main(25°C)}=80\mu\times(R_3//R_{NTC\,(25°C)})+(R_1//R_2)=1.624V$$

$$V_{TSEN\_Main(100°C)}=80\mu\times(R_3//R_{NTC\,(100°C)})+(R_1//R_2)=1.092V$$

$$3.2\times\frac{R_2}{R_1+R_2}=1.851V$$

R_1 = 15.214kΩ, R_2 = 20.898kΩ and R3 = 5618.685kΩ.

Three equations can be got as following for AUXI VR rail :

$$V_{TSEN\_AUXI(25°C)}=80\mu\times(R_3//R_{NTC(25°C)})+(R_1//R_2)=1.624V$$

$$V_{TSEN\_AUXI(100°C)}=80\mu\times(R_3//R_{NTC(100°C)})+(R_1//R_2)=1.092V$$

$$3.2\times\frac{R_2}{R_1+R_2}=550mV$$

R_1 = 16.083kΩ, R_2 = 19.059kΩ and R3 = 5618.685kΩ.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-52L 6x6 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (26.5°C/W) = 3.77W for WQFN-52L 6x6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 26 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

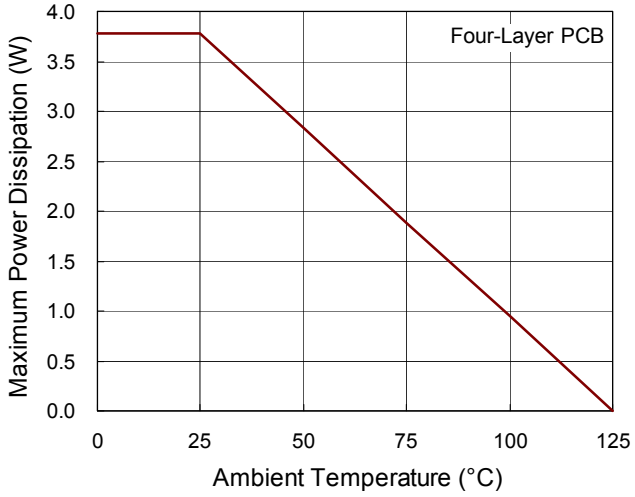
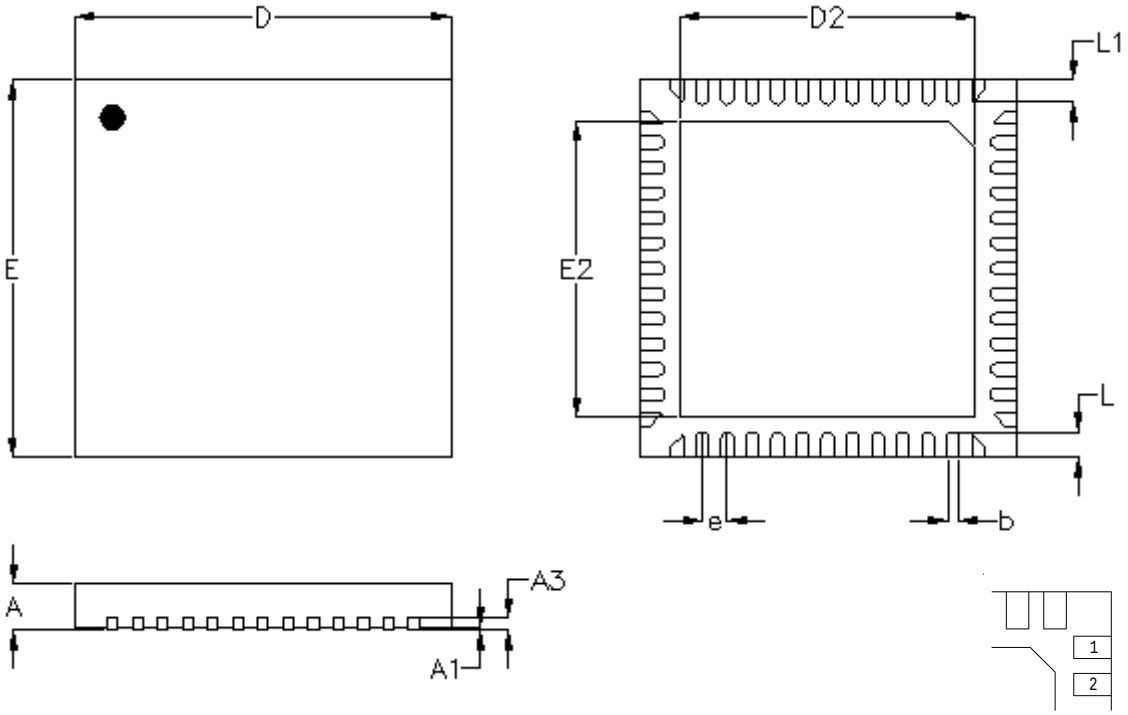


Figure 26. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
E	5.950	6.050	0.234	0.238
E2	4.650	4.750	0.183	0.187
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.300	0.400	0.012	0.016

W-Type 52L QFN 6x6 Package

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Item	Description
P00	2014/6/6		First Edition
P01	2014/8/11	Features Pin Configurations Functional Pin Description Function Block Diagram Operation Table 1 Electrical Characteristics Application Information	Modify Add Application Information
P02	2015/4/15	Pin Configurations Functional Pin Description Function Block Diagram Operation Electrical Characteristics Typical Application Circuit Applications information	Modify