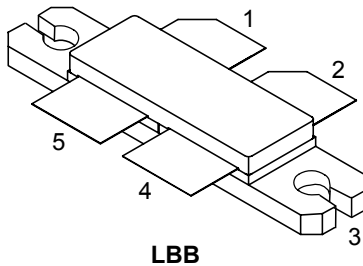


150 W, 28/32 V, HF to 1 GHz RF power LDMOS transistor



Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
RF3L05150CB4	520 MHz	28 V	150 W	23 dB	60 %

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the european directive 2002/95/EC

Applications

- 2-30 MHz HF or short wave communication
- 30-88 MHz ground communication
- 118-140 MHz Avionics
- 136-174 MHz commercial ground communication
- 30-512 MHz Jammer, ground/air communication
- HF to 1000 MHz ISM - instrumentation

Pin connection	
Pin	Connection
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Description

The RF3L05150CB4 is a 150 W, 28/32 V LDMOS FET designed for wide-band communication and ISM applications with frequencies from HF to 1 GHz. It can be used in class AB, B or C for all typical modulation formats.



Product status link
RF3L05150CB4

Product summary	
Order code	RF3L05150CB4
Marking	3L05150
Package	LBB
Packing	Tape and reel 13"
Base/bulk quantity	100/100

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	90	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	36	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	0.4	°C/W

1. $T_C = 85\text{ °C}$, $T_J = 200\text{ °C}$, DC test.

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 4. Static

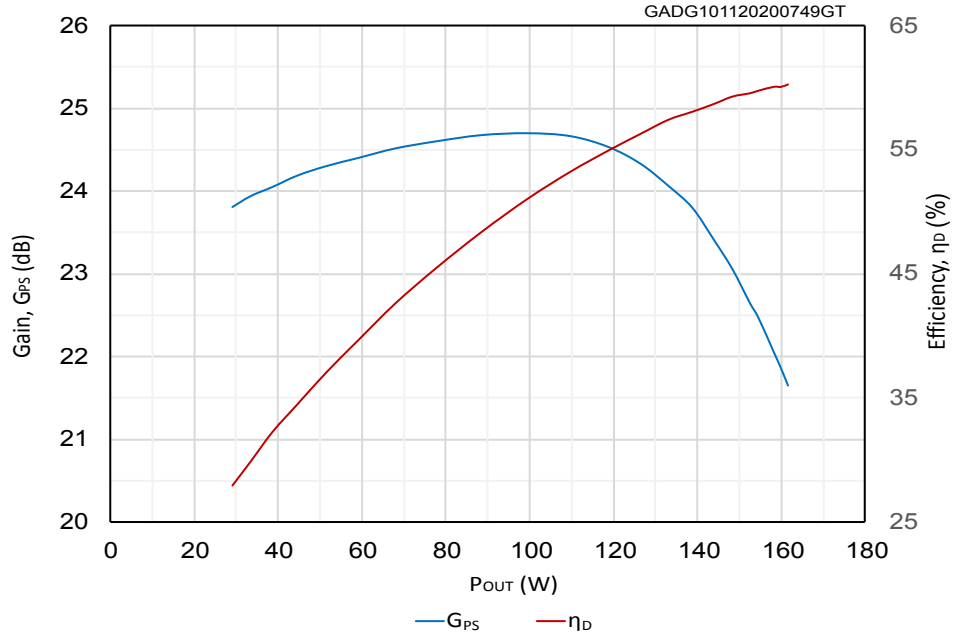
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 100\text{ }\mu\text{A}$	90			V
I_{DSS}	Zero gate voltage drain leakage current	$V_{GS} = 0\text{ V}$, $V_{DS} = 75\text{ V}$			1	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = -8/10\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 42\text{ V}$, $I_{DS} = 600\text{ }\mu\text{A}$	1.75		2.50	V
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 1\text{ V}$, $I_{DS} = 800\text{ mA}$	2.0		5.0	V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}$, $I_{DS} = 2\text{ A}$			650	mV
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$			1	Ω
C_{ISS}	Common source input capacitance			70		pF
C_{RSS}	Common source feedback capacitance	$V_{GS} = 0\text{ V}$, $V_{DD} = 28\text{ V}$, $f = 1\text{ MHz}$		1.1		pF
C_{OSS}	Common source output capacitance			30		pF

Table 5. Dynamic

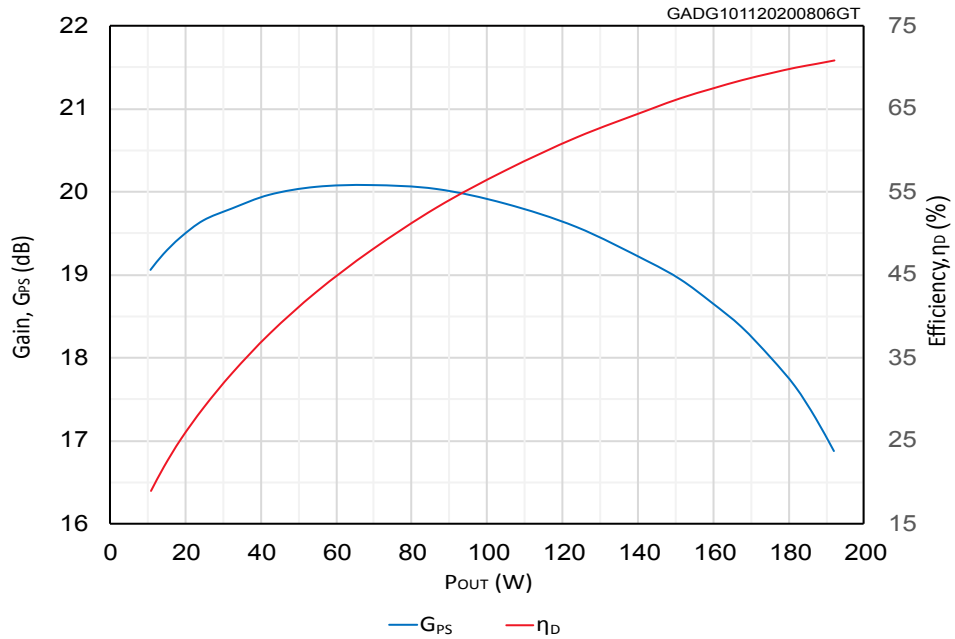
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency				1000	MHz
P_{OUT}	Output power	f = 520 MHz 1 dB compression, pulsed CW		150		W
G_{PS}	Power gain			23		dB
η_D	Drain efficiency			60		%
VSWR	Load mismatch	At 150 W pulsed CW output power, all phase angles			20:1	

Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 500\text{ mA}$, pulse width = 20 μs , duty cycle = 10%.

3 Typical performances

Figure 1. Power gain and drain efficiency vs output power (f = 520 MHz)


Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 500\text{ mA}$, pulsed CW, pulse width = 20 μs , duty cycle = 10%.

Figure 2. Power gain and drain efficiency vs output power (f = 860 MHz)


Note: $V_{DD} = 32\text{ V}$, $I_{DQ} = 400\text{ mA}$, pulsed CW, pulse width = 20 μs , duty cycle = 10%.

Figure 3. Gain, efficiency and P_{1dB} vs frequency (typical broadband data)

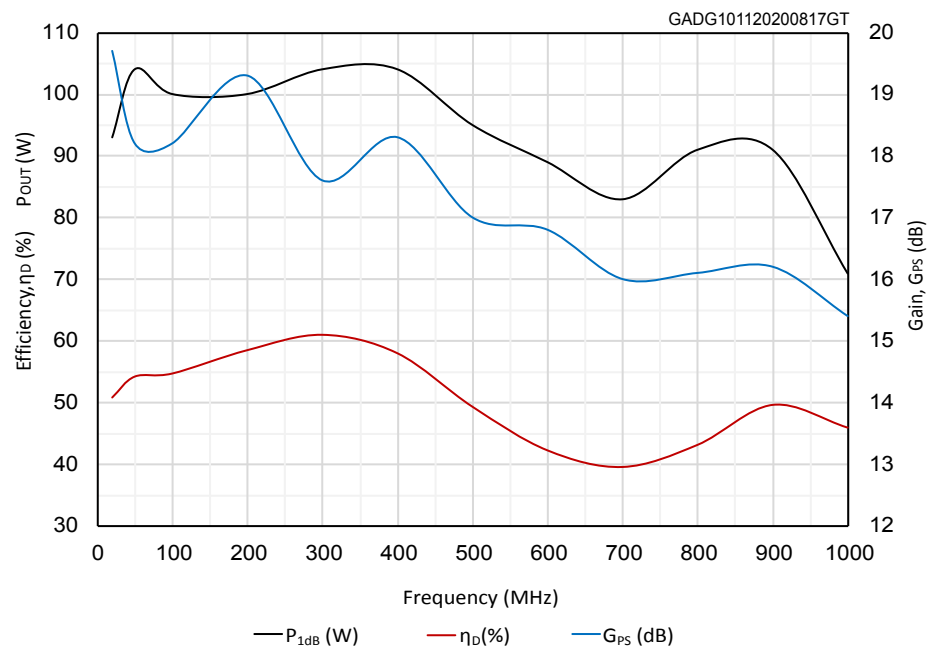
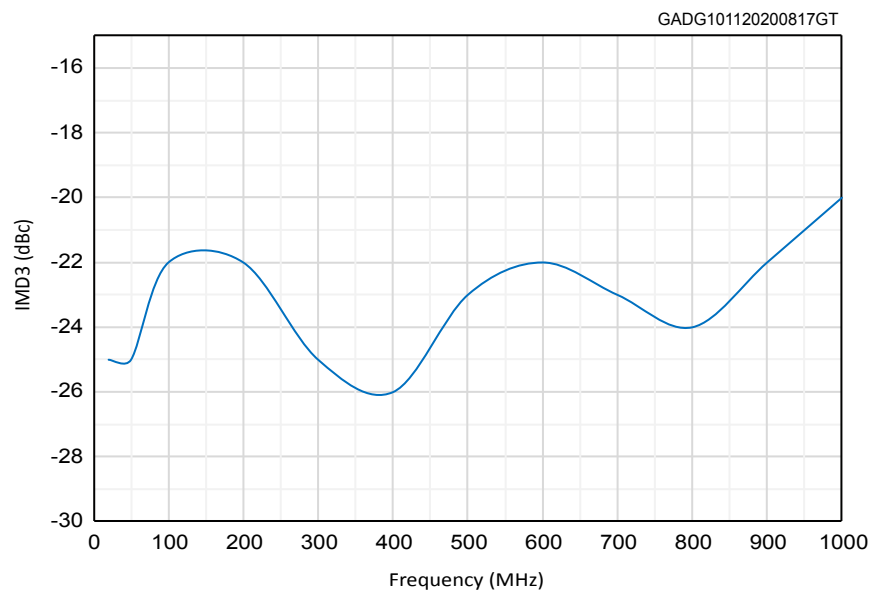


Figure 4. IMD3 versus Frequency (2 tones test, 200 kHz spacing)



Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 400\text{ mA}$, pulsed CW, pulse width = 20 μs , duty cycle = 10%.

4 Test circuits

Figure 5. Test circuit layout (f = 520 MHz)

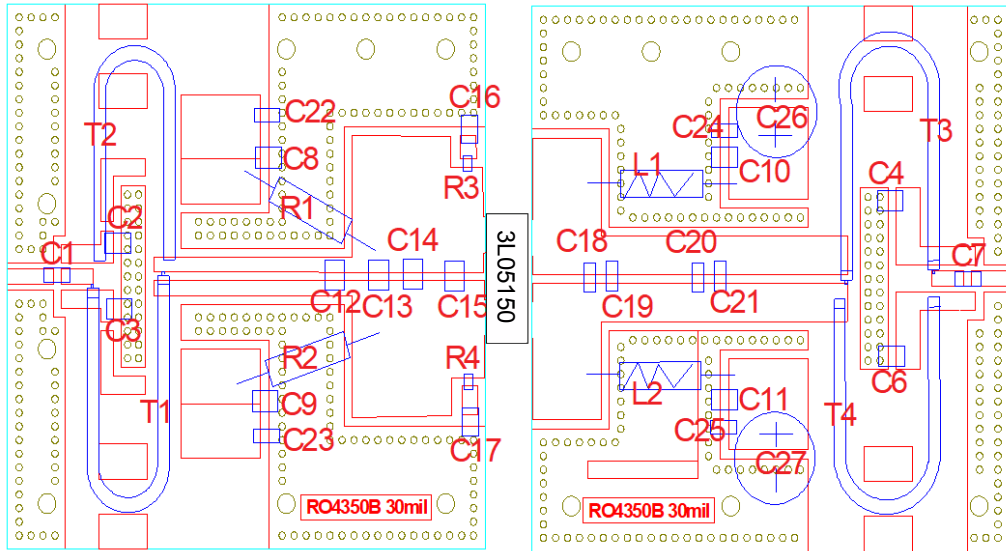


Figure 6. Test circuit photo (f = 520 MHz)

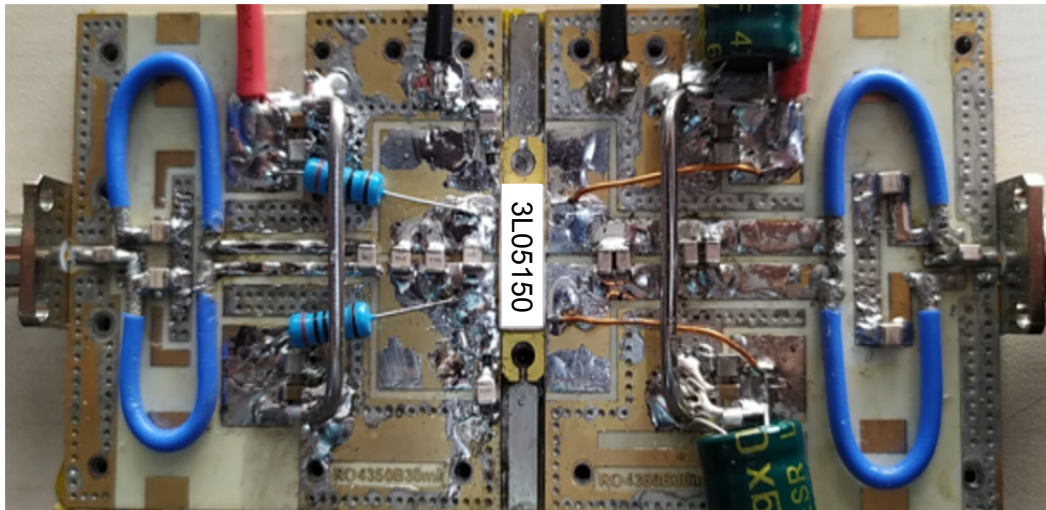


Table 6. Components list (f = 520 MHz)

Component	Value	Reference
C1~C7	47 pF	DLC70B
C8~C11	68 pF	ATC800B
C12, C13, 14	18 pF	DLC70B
C15	20 pF	DLC70B
C16, C17	1000 pF	DLC70B
C18	2.2 pF	DLC70B
C19	5.6 pF	DLC70B
C20	12 pF	DLC70B
C21	5.6 pF	DLC70B
C22~C25	10 μ F	100 V multilayer ceramic capacitor
C26, C27	470 μ F	63 V Aluminum electrolytic capacitor
R1, R2	200 Ω	
R3, R4	15 Ω	0805 chip resistor
L1, L2	ϕ 0.5, 30 mm, enameled wire	
T1, T2, T3, T4	25 Ω , 50 mm	SF-086-1.5
PCB	30 mils Rogers 4350B	

Figure 7. Test circuit photo (f = 860 MHz)

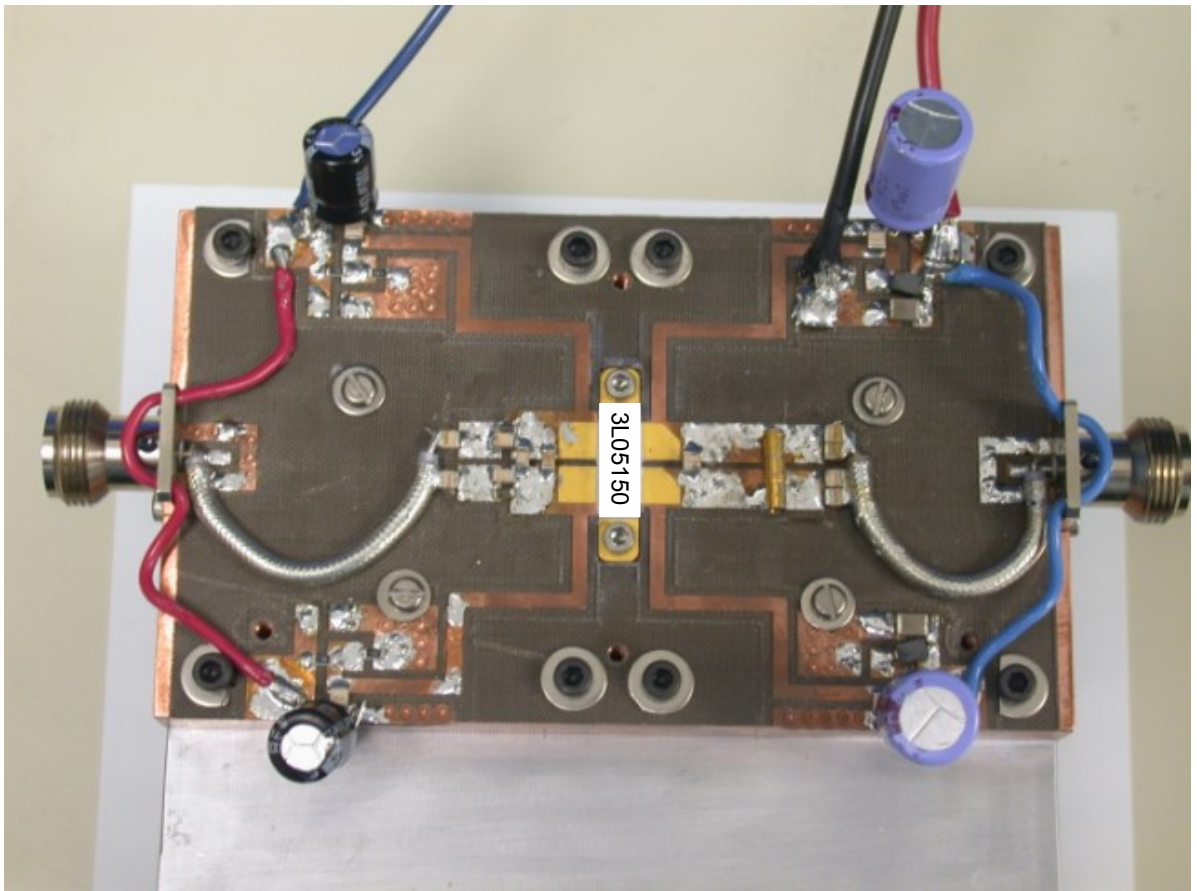


Figure 8. Test circuit schematic (f = 860 MHz)

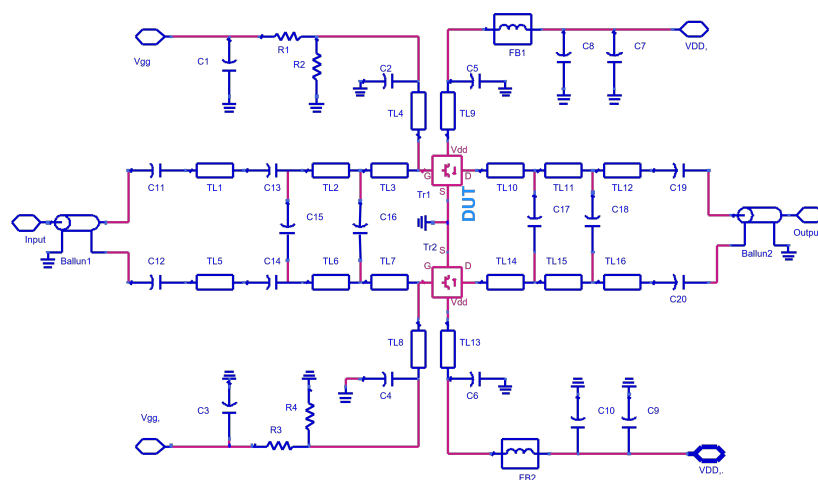


Table 7. Components list (f = 860 MHz)

Component	Value	Reference	Description
R1, R3	CR1206-8W-130JB	Venkel	13 Ω , 1/8W surfacr mount chip resistor
R2,R4	CR1206-8W-122JB	Venkel	1.2 k Ω , 1/8W surfacr mount chip resistor
R5,R6	CR1206-8W-250JB	Venkel	25 Ω , 1/8W surfacr mount chip resistor
FB1,FB2	2743021447	FAIR-RITE CORP	Surface mount EMI sheild bead
C1,C3,C7,C9			100 μ F, 63 V electrolytic capacitor
C2,C4,C5,C6	ATC100B910XXXX	ATC	91 pF chip capacitor
C8,C10	C1812X7R501-104KNE	Venkel	0.1 μ F 500 V surface mount ceramic chip capacitor
C11,C12	ATC100B620XXXX	ATC	62 pF chip capacitor
C13, C14	ATC100B151XXXX	ATC	150 pF chip capacitor
C15	ATC100B110XXXX	ATC	11pF chip capacitor
C16	ATC100B7R5XXXX	ATC	7.5pF chip capacitor
C17	ATC100B1R1XXXX	ATC	1.1pF chip capacitor
C18	27291PC	Johanson	0.8-8pF giga trim variable capacitor
C19, C20	ATC100B101XXXX	ATC	100 pF chip capacitor
B1, B2	EZ 141	Huber-Suhner	Balun , 50 Ω sucoform, od 0.141. 2.37 lg coaxial cable or equivalent
TL1, TL5			L = 0.250 in [6.35 mm] W = 0.214 in [5.44 mm]
TL2, TL6			L = 0.182 in [4.62 mm] W = 0.284 in [7.21 mm]
TL3, TL7			L = 0.318 in [8.08 mm] W = 0.284 in [7.21 mm]
TL4, TL8, TL9, TL13			L = 2.37 in [60.19 mm] W = 0.082 in [2.08 mm]
TL10, TL14			L = 0.314 in [7.97 mm] W = 0.230 in [5.84 mm]
TL11, TL15			L = 0.460 in [11.68 mm] W = 0.230 in [5.84 mm]
TL12, TL16			L = 0.280 in [7.11 mm] W = 0.230 in [5.84 mm]
Board 3X5		Rogers Corp	$\epsilon_r = 2.55$ t = 0.0026 in h = 0.030 in

Figure 9. Test circuit photo (broadband)



Table 8. Components list (broadband)

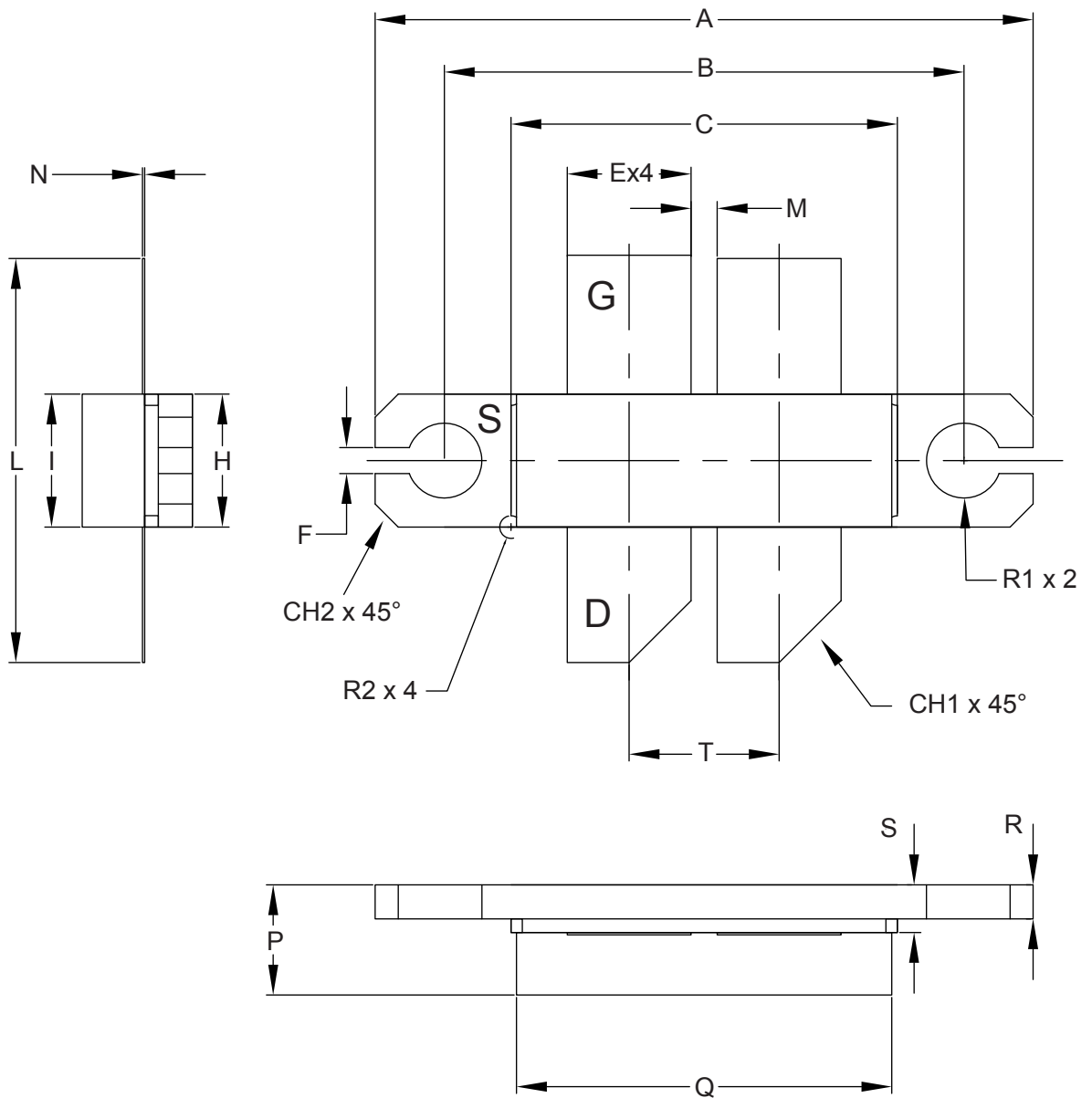
Reference	Value	Reference
C1	12 pF	ATC600F
C2	15 pF	ATC600F
C3	18 pF	ATC600F
C4	8.2 pF	ATC800B
C5	1 pF	ATC600F
C6	120 pF	ATC100B
C7, C8	220 pF	ATC100B
C9,C10	1 nF	ATC100B
C11,C12	10 μ F	
R1, R2, R3	300 Ω	
T1, T2	17 Ω - 65 mm	BN-61-202
T3, T4	25 Ω - 65 mm	BN-61-202
T5, T6	50 Ω - 65 mm	BN-61-202
L1	8 turns - diameter = 7 mm	
PCB	30 mils Rogers4350B	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LBB package information

Figure 10. LBB package outline



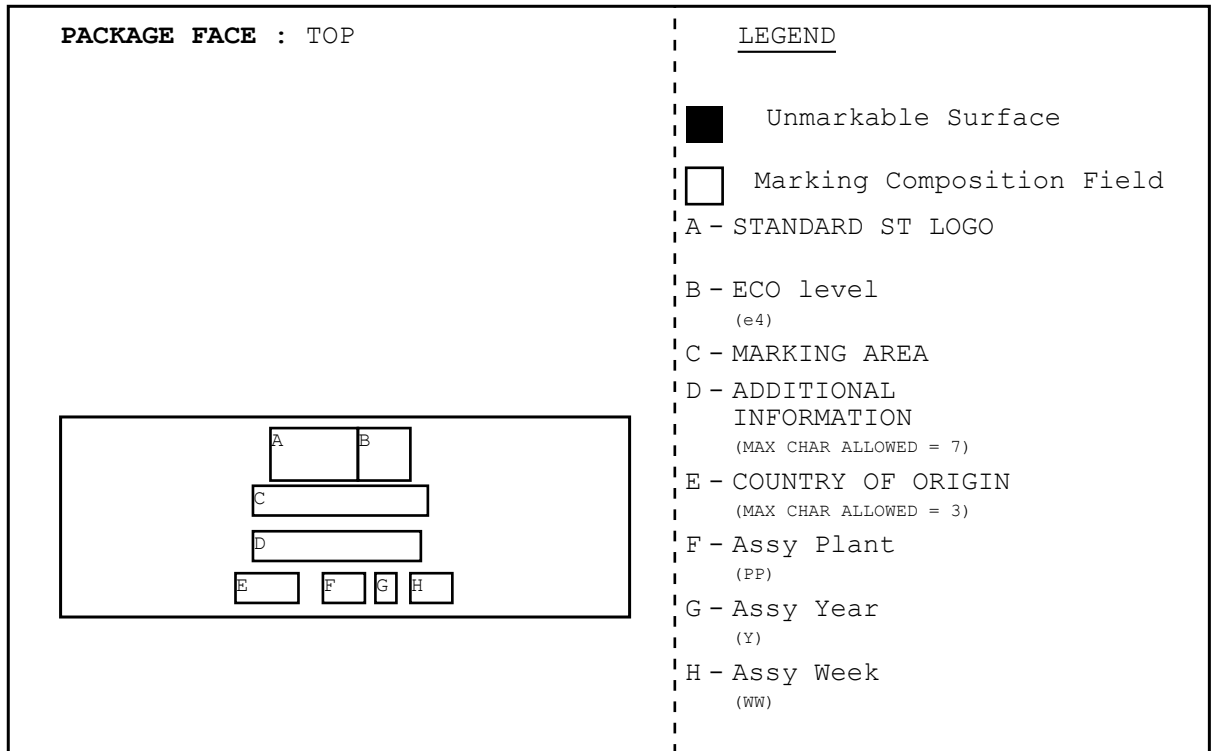
DM00666717_2

Table 9. LBB mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	28.82	28.95	29.08
B	22.73	22.86	22.99
C	16.87	17.00	17.13
E	5.32	5.45	5.58
F	1.01	1.14	1.27
H	5.72	5.85	5.98
I	5.72	5.85	5.98
L	17.65	17.78	17.91
M	1.02	1.15	1.28
N		0.10	
P	4.72	4.85	4.98
Q	16.38	16.51	16.64
R	1.37	1.50	1.63
S	1.97	2.10	2.23
T		6.60	
CH1		2.72	
CH2		1.02	
R1		1.65	
R2		0.50	

5.2 Marking information

Figure 11. Marking composition



GADG040220211644GT

Revision history

Table 10. Document revision history

Date	Version	Changes
08-Jun-2020	1	First release
12-Nov-2020	2	Updated Features. Updated Table 5. Dynamic. Updated Section 3 Typical performances. Updated Test circuit (f = 650 MHz). Minor text changes.
16-Mar-2021	3	Updated title and table product summary in cover page. Updated Table 3. ESD protection, Section 2 Electrical characteristics, Section 3 Typical performances and Section 4 Test circuits. Added Section 5.2 Marking information. Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
3	Typical performances	4
4	Test circuits	6
5	Package information	11
5.1	LBB package information	11
5.2	Marking information	13
	Revision history	14

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