The Over-Power Phenomenon In DCM/CCM-Operated Flyback Converters (Part 1)

by Christophe Basso, ON Semiconductor, Toulouse, France

A flyback converter is usually designed to operate within a certain input-voltage range, characterized by a low-line and a high-line level. Between these two input voltages, the converter must be capable of delivering the nominal power for which it has been designed. To account for the unavoidable production tolerances, the engineer includes a certain margin in his calculations, ensuring the delivery of nominal power in worst-case situations such as low line and high temperature.

If the adopted margin benefits the converter at low line, experience shows that the output-power capability of the converter may double under high-line conditions. In this article series, we will explore the origins of this excess power and explain how it can be controlled so that output power remains within a reasonable range.

Operating Modes Of A Flyback Converter

A flyback converter transmits power in two operating cycles. When the primary switch is closed, energy is absorbed from the input source and stored in the magnetizing inductor of the transformer, L_p. Because of the transformer's winding configuration, the secondary-side diode is blocked, decoupling its downstream circuitry from the primary side. When the switch opens, the energy stored in the primary is transferred to the secondary side, producing a current that circulates in the output capacitor and the load. Fig. 1. depicts these events occurring during the on time (Fig. 1a) and the off time (Fig. 1b.)

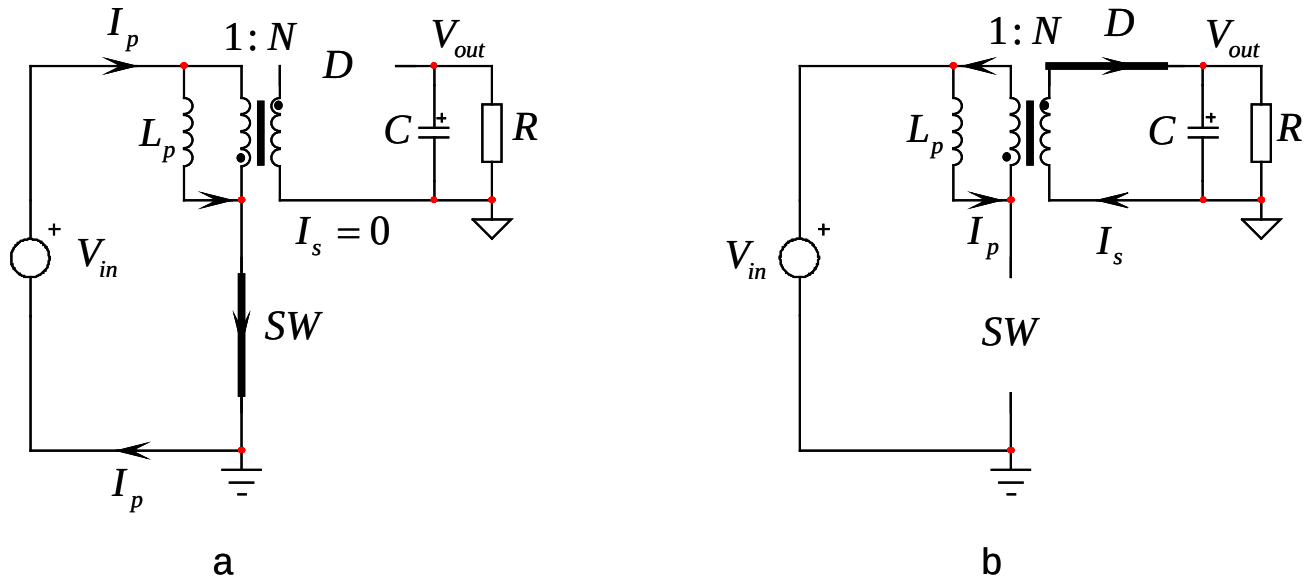

Fig.1. The two operating states of a flyback converter show energy storage in the primary side (a) followed by energy circulation in the secondary side (b).

Assuming 100% of the stored energy is transferred to the secondary side during a switching cycle, the primary inductor is fully demagnetized at the beginning of the next cycle. In this case, the converter is said to operate in the discontinuous-conduction mode (DCM): there is no current "memory" from the previous inductor state and the primary current ramps up from zero at the beginning of each switching cycle. On the other hand, if some energy remains in the transformer gap at the beginning of the next switching cycle, the inductor current no longer starts from zero but from an initial value known as the valley current (I_{valley}). In that case, the converter is said to operate in the continuous-conduction mode (CCM).

If we plot idealized currents circulating in a CCM flyback converter during the on and off times of the primary switch, we see the waveforms presented in Fig. 2. When the switch turns on, the current in the inductor ramps up linearly with a slope equal to:

$$S_{on} = \frac{V_{in}}{L_p} \quad (1)$$

If we operate in CCM, the value of the initial current in the inductor is not zero but the valley current. As the current ramps up and reaches a value I_{peak} imposed by the controller, the switch turns off. To fight against the collapsing magnetic field, the voltage across the primary inductor reverses and the secondary-side diode now conducts: the current circulates in the secondary winding, supplying both the capacitor and the load. The current in the secondary side now decreases with a slope equal to:

$$S_{off} = \frac{V_{out} + V_f}{L_s} \quad (2)$$

where V_f represents the diode's forward drop; V_{out}, the output voltage; and L_s, the transformer's secondary-side inductance.

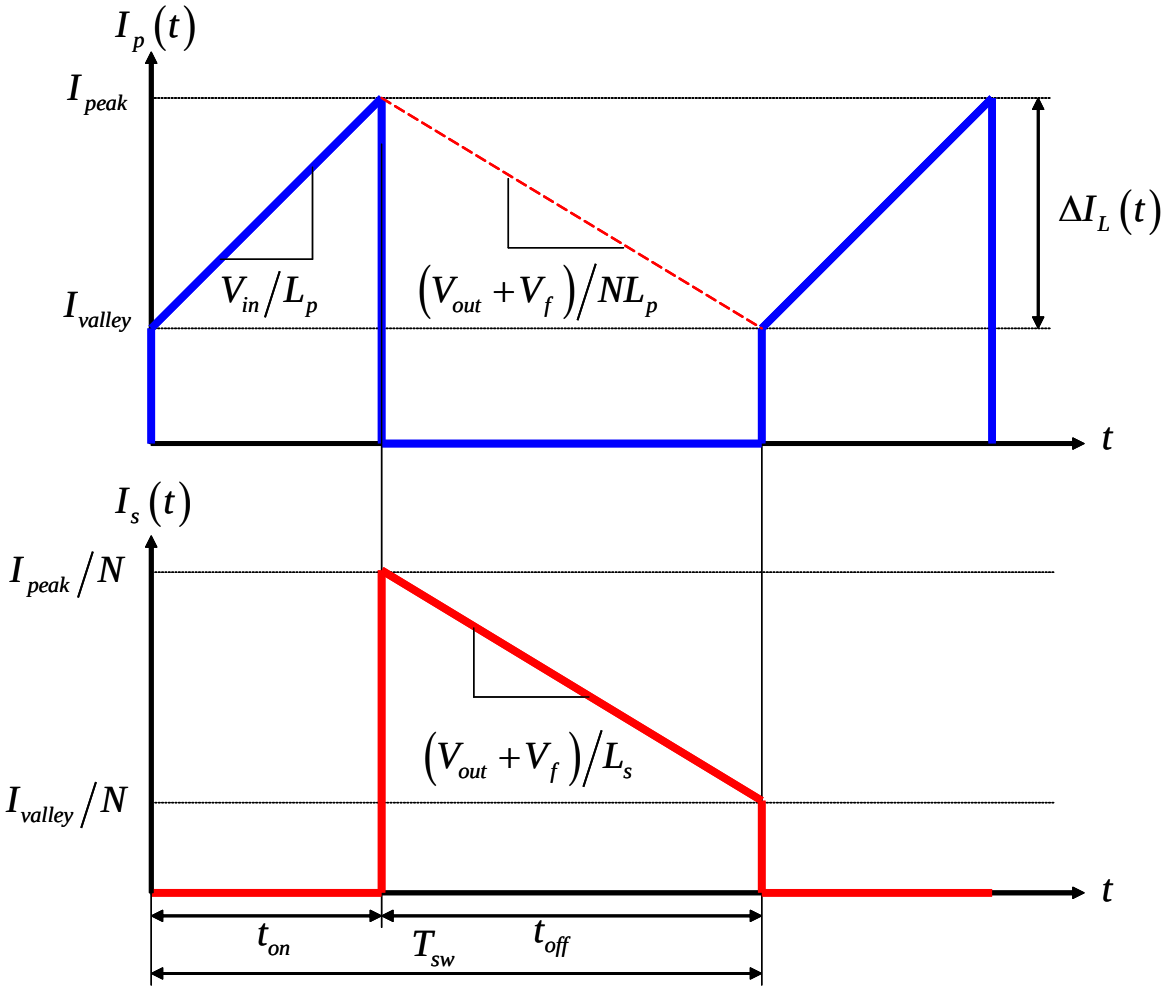

Fig 2. In CCM, the current first ramps up in the primary side until the switch opens and transfers the stored energy to the secondary side.

If we could observe the magnetizing inductor current from the primary side during the off time, we would see the secondary downslope described by equation (2) but reflected on the primary side as:

$$S_{off} = \frac{V_{out} + V_f}{NL_p} \tag{3}$$

where N is the turns ratio linking the primary and the secondary windings.

In Fig. 2., the inductor current swings between two values, I_{valley} and I_{peak}. The excursion between these points is called the ripple current and is defined by:

$$\Delta I_L = I_{peak} - I_{valley} \tag{4}$$

In heavy CCM operation, the ripple current can be very small and the waveforms resemble a square-wave as I_{valley} increases. When the load gets lighter, the converter transitions to DCM and the valley current vanishes to zero. The inductor ripple current is then maximum and corresponds to the full swing. The primary- and secondary-current waveforms are updated in Fig. 3 to illustrate DCM operation.

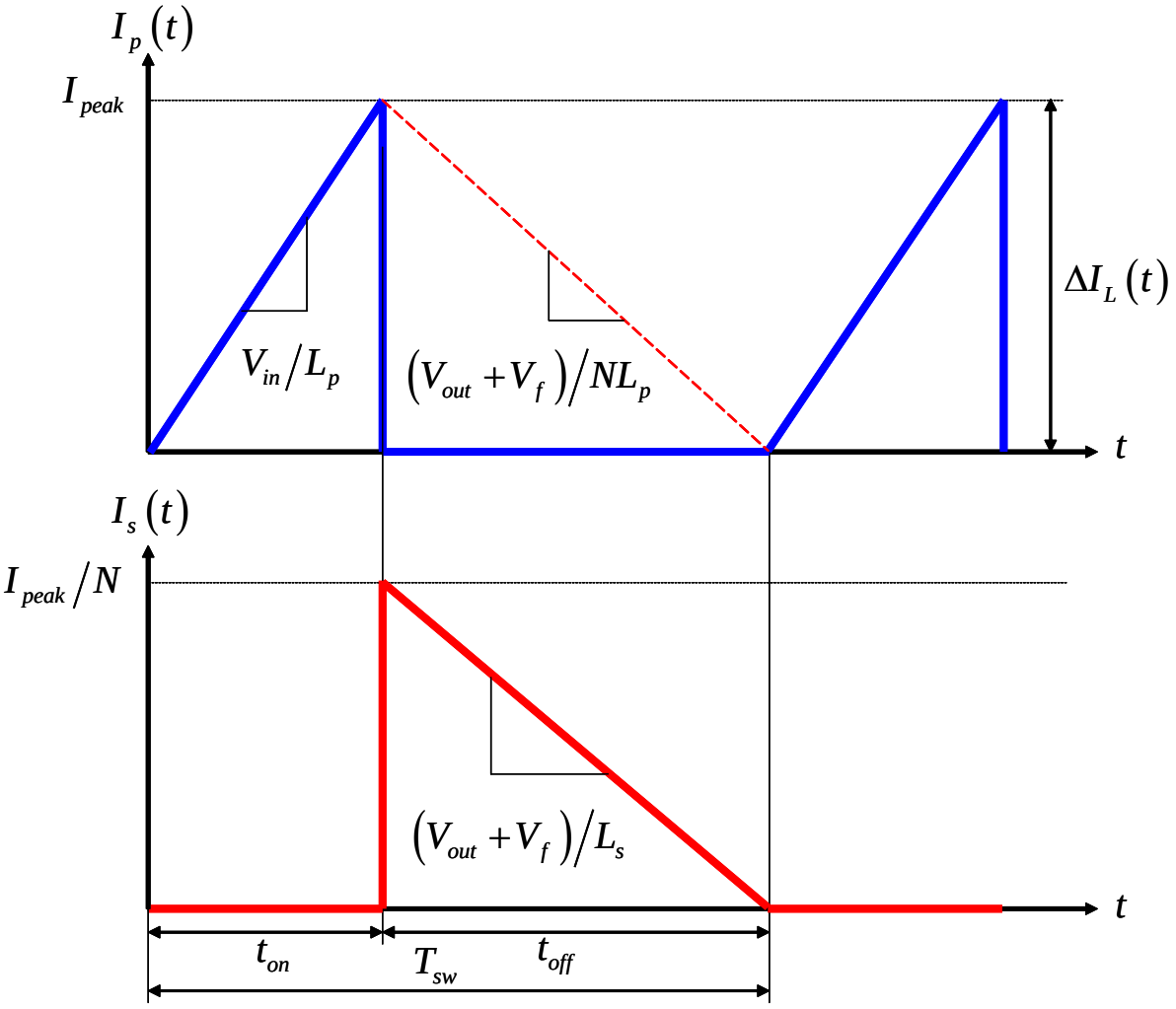

Fig. 3. When the flyback converter operates in DCM, the inductor current ramps up from zero.

At a similar power level, the circulating ac currents in CCM are smaller than in DCM, leading to lower conduction losses in the first case. Mode transition occurs as a function of the load but also the input voltage. Usually, high-power converters are designed to operate in CCM at low line and enter DCM or light CCM at high line.

Power Transfer In A DCM Flyback Converter

What we need to calculate, now, is the amount of power transferred from the source to the output during a switching cycle. When the converter is supplied by a dc source V_{in}, the power delivered by the source is:

$$P_{in} = \frac{1}{T_{sw}} \int_0^{T_{sw}} I_{in}(t) V_{in}(t)\, dt = V_{in} I_{in,avg} \tag{5}$$

By looking at the upper waveform in Fig. 2., we can see that the average input current equals:

$$I_{in,avg} = \left(I_{valley} + \frac{\Delta I_L}{2} \right) \frac{t_{on}}{T_{sw}} = \frac{I_{peak} + I_{valley}}{2} t_{on} F_{sw} \tag{6}$$

Knowing the primary inductor slope from equation (1), we can obtain a definition for the ripple current ΔI_L:

$$\Delta I_L = \frac{V_{in}}{L_p} t_{on} \tag{7}$$

Combining equations (4) and (7), we can extract a definition for the on time:

$$t_{on} = \frac{\left(I_{peak} - I_{valley} \right) L_p}{V_{in}} \tag{8}$$

Substituting equation (8) into (6), we have:

$$I_{in,avg} = \frac{\left(I_{peak} + I_{valley} \right)}{2} \frac{\left(I_{peak} - I_{valley} \right)}{V_{in}} L_p F_{sw} \tag{9}$$

If we now multiply both sides of the equation by V_{in} and re-arrange the expression:

$$P_{in} = \frac{1}{2} L_p \left({I_{peak}}^2 - {I_{valley}}^2 \right) F_{sw} \tag{10}$$

This equation describes the power absorbed from the source by a flyback converter operated in CCM. Should the converter operate in DCM, the valley current would drop to zero, simplifying the expression to:

$$P_{in} = \frac{1}{2} L_p {I_{peak}}^2 F_{sw} \tag{11}$$

The transmitted output power, available to the load on the secondary side, is simply the absorbed power affected by the overall efficiency, η (eta).

$$P_{out} = \frac{1}{2} L_p \left({I_{peak}}^2 - {I_{valley}}^2 \right) F_{sw} \eta \tag{12}$$

Effect Of Propagation Delay On Maximum Output-Power Level

In a current-mode-controlled power supply, the feedback loop adjusts the primary-inductor peak current on a cycle-by-cycle basis as a function of the input/output parameters. In a classical arrangement, a sense resistor converts the primary current into a voltage that is then applied to the current-sense pin of the selected controller.

However, there are some situations where the feedback loop is lost, e.g. in output short circuits, at start-up or when the optocoupler is destroyed. In these fault conditions, it is important to keep the acceptable peak current within safe limits. A high peak current could cause transformer saturation, clamping voltage runaway, and possibly smoke.

For this reason, it is common to find an internal clamp in the pulse-width modulation (PWM) controller that limits the current-setpoint excursion. As an example, consider the UC384X controller family, which contains a clamp that is set to 1 V. Because of this clamp, the maximum voltage developed on the current-sense resistor can never exceed 1 V, which would correspond to 1 A flowing through a 1-Ω resistor. In the new NCP1250 from ON Semiconductor, this voltage limit has been reduced to 0.8 V, ensuring a slight increase in the converter's overall efficiency. Fig. 4. depicts the internal implementation of such a circuit.

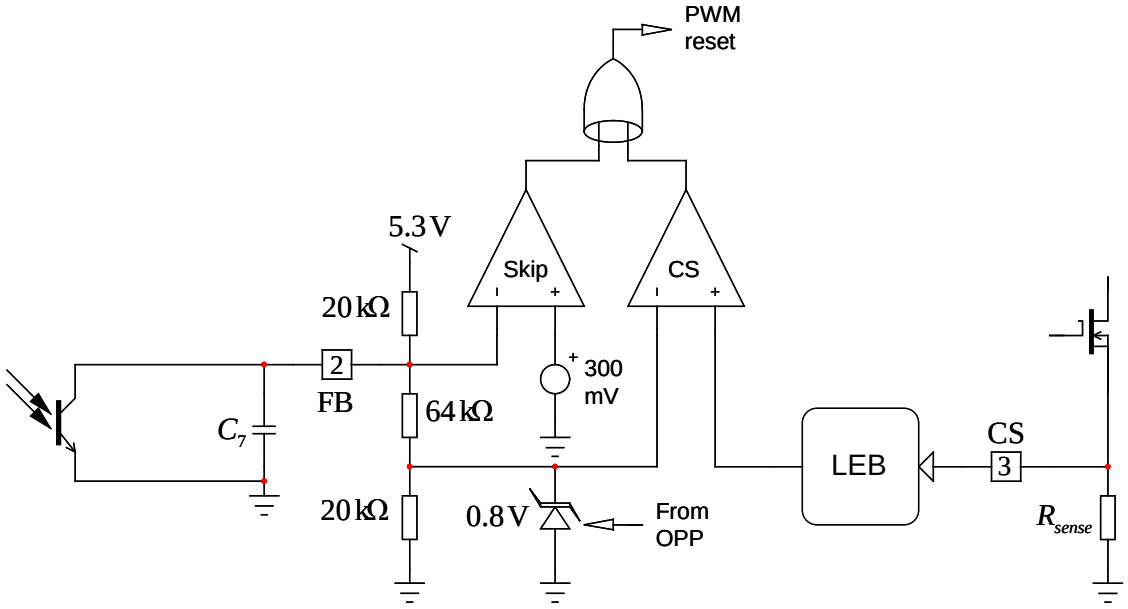

Fig. 4. The maximum peak current is set by the 0.8-V reference voltage.

In Fig. 4., the feedback voltage reaches the current setpoint after voltage division by a factor of 4.2. In case of loop failure, the feedback voltage jumps to 5.3 V but thanks to the 0.8-V active Zener diode, the current setpoint cannot exceed the following value:

$$I_{peak,\max} = \frac{V_{sense,\max}}{R_{sense}} = \frac{0.8}{R_{sense}} \qquad (13)$$

At least, that is the current limit in theory. Unfortunately, the reality is different as illustrated by Fig. 5.

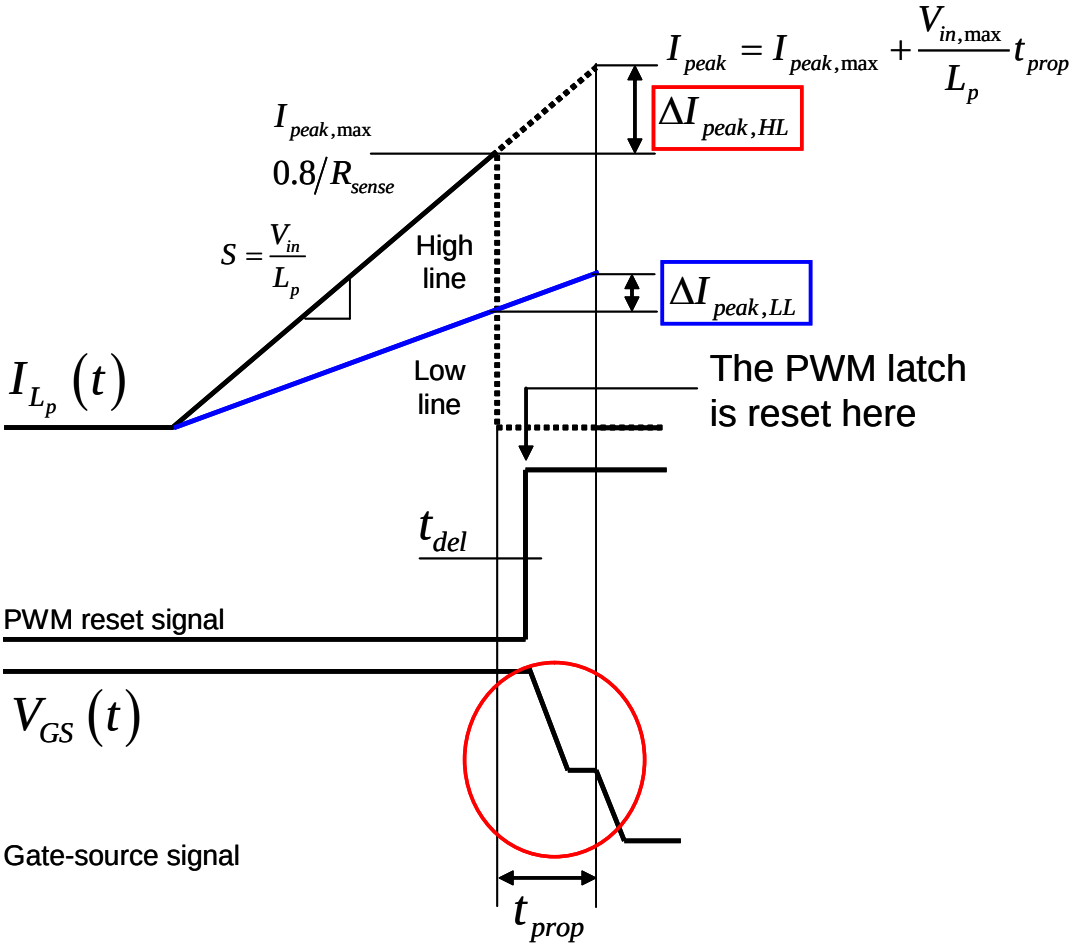

Fig. 5. When an overcurrent condition is detected, it takes a certain amount of time before the controller acknowledges the fault and propagates the turn-off signal to the MOSFET gate.

In this picture, we can see the current level growing and reaching the maximum value imposed by equation (13). We would expect the comparator to immediately react, however, this device is affected by a response time. Before the reset order reaches the latch and instructs the driver output to go low, a certain amount of time elapses. Furthermore, even when the controller drive pin goes to ground, there will still be an additional delay in the propagation of this drive signal to the MOSFET gate. This second delay is due to the resistive elements in the path from the controller to the MOSFET. During this period of delays, the inductor current keeps increasing according to the slope defined by equation (1). When the MOSFET eventually opens, the current has reached a peak defined by:

$$I_{peak,\max} = \frac{V_{sense,\max}}{R_{sense}} + \frac{V_{in}}{L_p} t_{prop} \qquad (14)$$

As the equation indicates, the variable part depends on the input voltage. At low line, there is a slight current overshoot that barely affects the maximum delivered power before the controller protection trips. On the other hand, in high-line conditions, the overshoot can be quite large, particularly if the driver sink capability is weak and large-Q_G MOSFETs are selected. If we calculate the percentage of maximum peak-current increase from low line ($_{LL}$) to high line ($_{HL}$), we can show that the equation is:

$$\frac{I_{peak,\max,HL} - I_{peak,\max,LL}}{I_{peak,\max,LL}} = \frac{V_{in,HL} - V_{in,LL}}{\frac{L_p V_{sense,\max}}{t_{prop} R_{sense}} + V_{in,LL}} \qquad (15)$$

where

$V_{in,HL}$ is the dc input voltage high line, 370 V

$V_{in,LL}$ is the dc input voltage low line, 120 V

L_p is the transformer primary inductor, 200 µH

t_{prop} is the total propagation delay, 350 ns

R_{sense} is the sense resistor, 0.33 Ω

V_{sense} is the maximum authorized sense value, 0.8 V

If we use the above values, which were derived for a universal mains 30-W DCM-adapter featuring an NCP1250, we have a peak current with a variation from low to high line of:

$$\frac{\Delta I_{peak}}{I_{peak,\max,LL}} = \frac{370-120}{\frac{200u\times 0.8}{350n\times 0.33}+120} = 0.166 \text{ or } 16.6\% \quad (16)$$

Practically speaking, if the low-line maximum current is:

$$I_{peak,\max,LL} = \frac{0.8}{0.33}+\frac{120}{200u}\times 350n = 2.63\,\text{A} \quad (17)$$

It increases under high-line conditions to:

$$I_{peak,\max,HL} = I_{peak,\max,LL}\left(1+\frac{\Delta I_{peak}}{I_{peak,\max,LL}}\right) = 2.63\times 1.166 = 3.07\,\text{A} \quad (18)$$

As a first rough calculation, the extra power available at high line in DCM can thus be quickly extrapolated from equation (16) via (11):

$$\frac{\Delta P_{out}}{P_{out,LL}} = \left(1+\frac{\Delta I_{peak}}{I_{peak,\max,LL}}\right)^2 = 1.166^2 \approx 36\% \quad (19)$$

However, in this approach, we considered a constant 100% efficiency between low and high-line conditions. In reality, the efficiency at high line is always slightly greater than that of low line. That's because as the duty-ratio decreases, the rms values of the circulating currents also decrease, naturally reducing the associated losses. If we now include the efficiency change in our calculations, we can express the maximum power at low and high lines in a fault condition (the feedback is lost and the internal 0.8-V clamp is activated.) The equations for maximum power are:

$$P_{out,LL} = \frac{1}{2}L_p I_{peak,\max,LL}{}^2 F_{sw}\eta_{LL} \quad (20)$$

$$P_{out,HL} = \frac{1}{2}L_p I_{peak,\max,HL}{}^2 F_{sw}\eta_{HL} \quad (21)$$

If we calculate the power difference between low and high line and compare it to that of low line, we have:

$$\frac{\Delta P_{out}}{P_{out,LL}} = \frac{I_{peak,\max,HL}{}^2 \eta_{HL}}{I_{peak,\max,LL}{}^2 \eta_{LL}} - 1 \quad (22)$$

Considering the respective low- and high-line efficiency numbers of 85% and 89% calculated for the 30-W adapter example, we can refine the previous calculations:

$$\frac{\Delta P_{out}}{P_{out,LL}} = \frac{3.07^2 \times 0.89}{2.63^2 \times 0.85} - 1 = 42\% \quad (23)$$

From equation (20), the maximum power output at low line is estimated to be:

$$P_{out,LL} = \frac{1}{2} L_p I_{peak,\max,LL}{}^2 F_{sw} \eta_{LL} = 0.5 \times 200u \times 2.63^2 \times 65k \times 0.85 \approx 38\,\text{W} \quad (24)$$

According to equation (23), the high-line power will rise to:

$$P_{out,\max,HL} = P_{out,\max,LL} \frac{\Delta P_{out}}{P_{out,LL}} = 38 \times 1.42 = 54\,\text{W} \quad (25)$$

If our example adapter has an output voltage equal to 19 V (which is common), the maximum current circulating in the output diode can differ significantly between low- and high-line operating conditions:

$$I_{out,\max,LL} = \frac{P_{\max,LL}}{V_{out}} = \frac{38}{19} = 2\,\text{A} \quad (26)$$

$$I_{out,\max,HL} = \frac{P_{\max,HL}}{V_{out}} = \frac{54}{19} = 2.8\,\text{A} \quad (27)$$

Why Limit the Maximum Power?

First, let's consider the output diode. Having a high-line current much larger than the nominal current forces you to oversize the diode or its associated heatsink. It comes at a cost and size/volume increase of course. Second, there's a compliance issue. In safety document IEC950 [1], the section on Limited Power Sources (LPS) describes a certification for maximum output-power limit. Table 1 describes the maximum power that can be delivered by a power supply fulfilling the LPS requirements.

Table 1. Maximum power capability of LPS-compliant power supplies.

Output Voltage $V_{out}\,(\text{V})$		Output Current $I_{out}\,(\text{A})$	Apparent Power $S\,(\text{VA})$
V_{rms}	V_{dc}		
≤ 20	≤ 20	≤ 8	$\le 5 \cdot V_{out}$
$20 < V_{out} \le 30$	$20 < V_{out} \le 30$	≤ 8	≤ 100
-	$20 < V_{out} \le 60$	$\le 150/V_{out}$	≤ 100

If a power supply manufacturer can show the compliance of his converter with the LPS test, the manufacturer may use less expensive materials for the enclosure.

In our example, a 19-V adapter can comply with the LPS definition if its output current is less than 8 A and its maximum power in fault condition stays below 5 x 19, or 95 W. Despite a power runaway at high line, our 30-W adapter does not exceed the LPS limit. Provided the diode can accept the extra current, no special precautions are needed. The problem becomes more challenging with higher-power adapters.

How Do We Limit Maximum Power?

In our explanation, we saw that the culprit for this extra power is the primary peak-current runaway at high line. For the typical example reflected in equation (16), the difference amounts to almost 17%. A solution to this problem is to reduce the maximum peak-current limit as a function of the input voltage as shown in Fig. 6 (graph on right). At low line, the current limit is unchanged, but as the input voltage grows, the peak current limit is gradually reduced. The final peak-current value could be selected so that the high-line output power roughly matches the low-line level. This technique is called over-power protection or OPP.

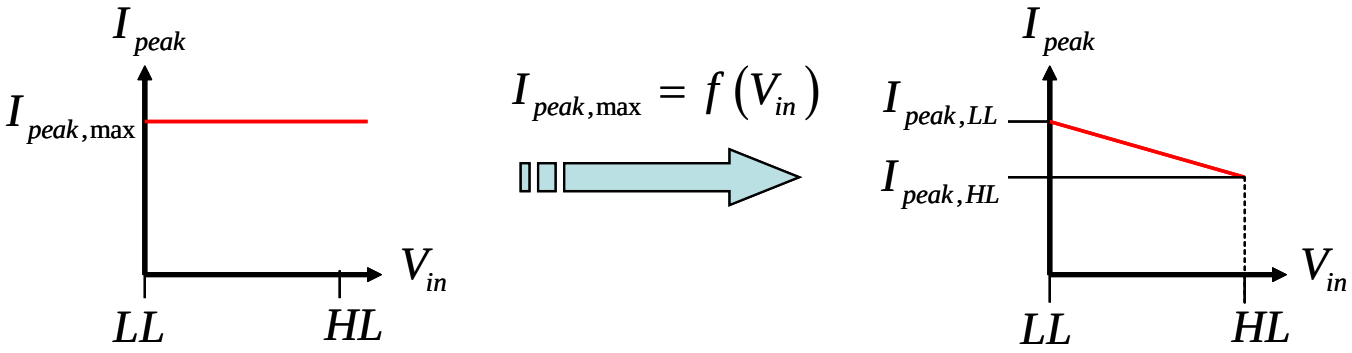

Fig. 6. One approach to implementing over-power protection is to limit the peak current as a function of input voltage.

To calculate the required peak current limit we must impose at high line, one option is to check what value of this parameter would force the high-line power to equal the low-line power. As our converter operates in DCM over the full range, we can formulate this requirement as follows:

$$\frac{1}{2}L_p\left(I_{peak,\max,LL}{}^2\right)F_{sw}\eta_{LL} = \frac{1}{2}L_p\left(I_{peak,\max,HL}{}^2\right)F_{sw}\eta_{HL} \qquad (28)$$

Extracting the peak-current definition, we obtain:

$$I_{peak,\max,HL} = \sqrt{\frac{2P_{\max,LL}}{L_pF_{sw}\eta_{HL}}} \qquad (29)$$

However, this value corresponds to the final peak current seen by the transformer inductor at high line. The current sensed by the controller on its dedicated pin (scaled in voltage by the sense resistor) must then reflect the propagation delay contribution that appears in equation (14):

$$I_{sense,\max,HL} = I_{peak,\max,HL} - \frac{V_{in,HL}}{L_p}t_{prop} = \sqrt{\frac{2P_{\max,LL}}{L_pF_{sw}\eta_{HL}}} - \frac{V_{in,HL}}{L_p}t_{prop} \qquad (30)$$

If we use the numerical values given previously and want our power supply delivering 38 W at high line, then applying equation (30) leads us to the following current sensed by the controller:

$$I_{sense,\max,HL} = \sqrt{\frac{2\times 38}{200u\times 65k\times 0.85}} - \frac{370}{200u}\times 350n = 1.927\,\text{A} \quad (31)$$

Given the usage of a 0.33-Ω resistor, the corresponding voltage sensed by the controller dedicated pin will be:

$$V_{sense,\max,HL} = I_{sense,\max,HL} R_{sense} = 1.927\times 0.33 = 636\,\text{mV} \quad (32)$$

In the NCP1250, the maximum sensed voltage is limited to 0.8 V. To reduce this level down to what equation (32) recommends, we must subtract 164 mV from 0.8 V.

There are several options to implement peak-current reduction at high line. Two of these options are illustrated in Fig. 7.

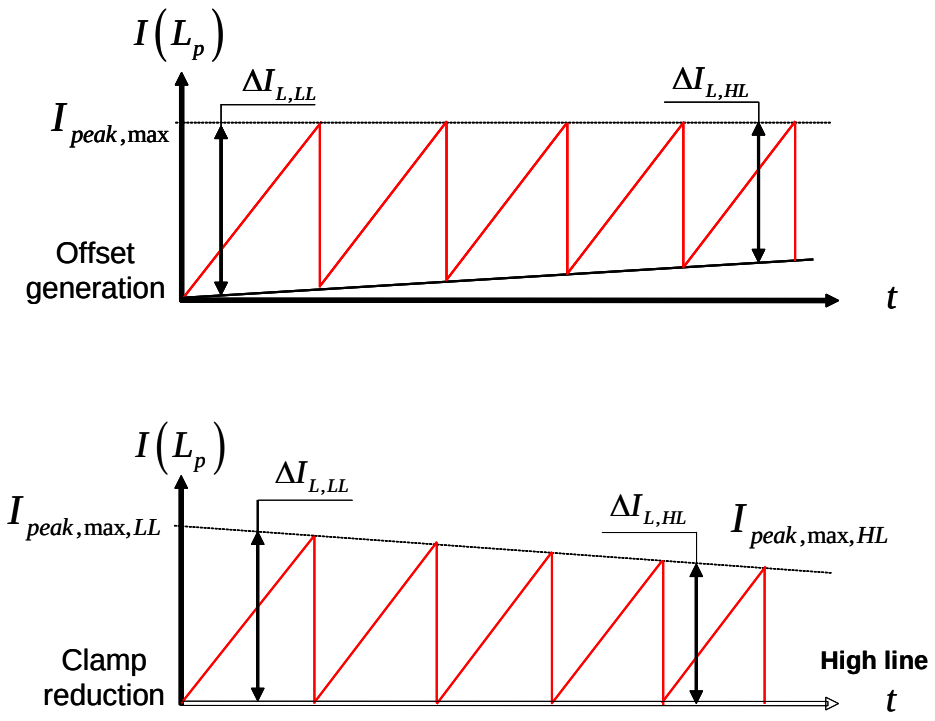

Fig. 7. The reduction in the peak-current limit at high line can be obtained by either offsetting the current-sense signal (top graph) or by reducing the internal clamping value (bottom graph).

In one approach, an offset is added to the current-sense voltage information. If the offset builds up with the growing input voltage, the available current shrinks dynamically, leading to the expected result. This technique is illustrated in the upper graph of Fig. 7.

A possible implementation of the offset method appears in Fig. 8. Experience shows that the obtained results are good and fit the bill in terms of peak-current reduction. However, the permanent presence of the OPP resistors connected to the bulk rail affects the standby power dramatically. Not only is there extra power dissipation in the resistors, there are also additional losses under light or no-load conditions because the permanent offset disturbs skip-cycle operations.

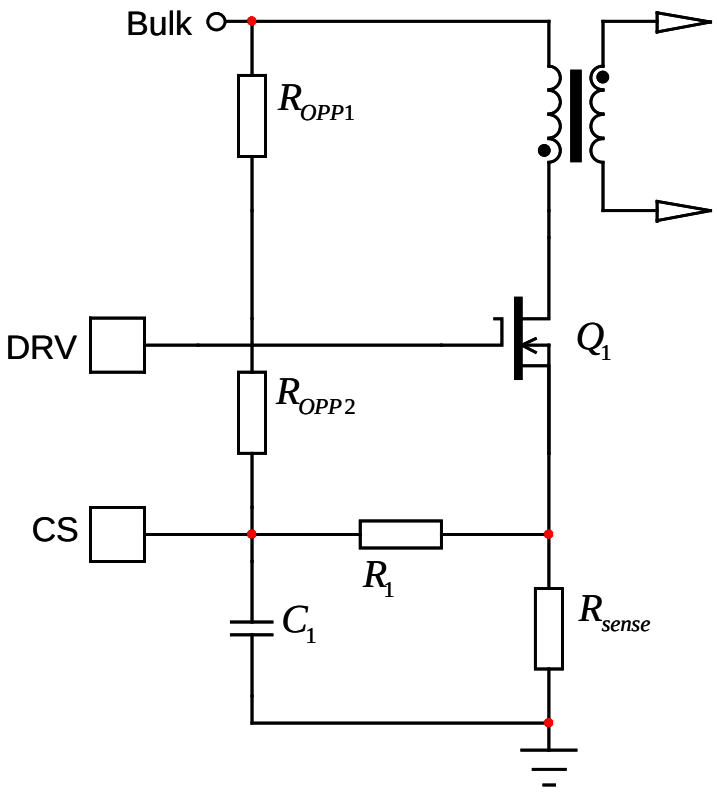

Fig. 8. By generating an offset from the bulk capacitor to the current sense pin, we can create a variable offset affecting the maximum output power of the converter.

The lower section of Fig. 7 represents another way of reaching the goal. The ground level is no longer affected, but the maximum allowed value of peak inductor current is reduced as the input voltage rises.

This is the technique implemented in the NCP1250 using a new circuit developed by ON Semiconductor. This circuit limits the maximum output power as effectively as the offset-generation technique but without the extra power dissipation associated with that technique. Furthermore, with the alternative method implemented in the NCP1250 (whose technical details appear in Fig. 9), the skip cycle is not affected.

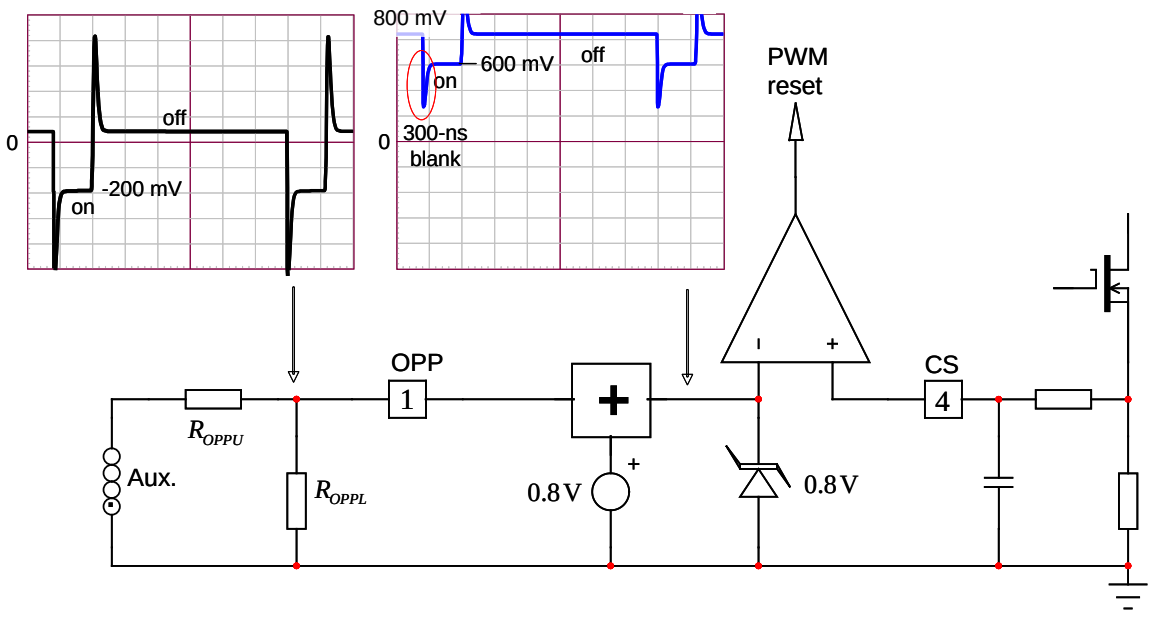

Fig. 9. Sensing the auxiliary winding of the flyback converter during the on time is an excellent way to obtain an image of the input voltage without incurring additional power dissipation.

The auxiliary winding of the flyback converter swings to $-NV_{in}$ during the on time. This negative voltage is thus representative of the input-voltage variations. If we scale it down via a resistive divider consisting of R_{OPPU} and R_{OPPL}, we can directly sum it with the internal positive 0.8-V reference voltage used for the active clamp. With this adopted technique, we can easily reduce the maximum clamping voltage down to 450 mV.

Final Results For OPP Implementation

Using the 30-W DCM adapter values, we have entered the formulas we derived in Mathcad and plotted the power variations with and without OPP implementation. In the calculations, the efficiency varies linearly from 85% to 89%. The results appear in Fig. 10.

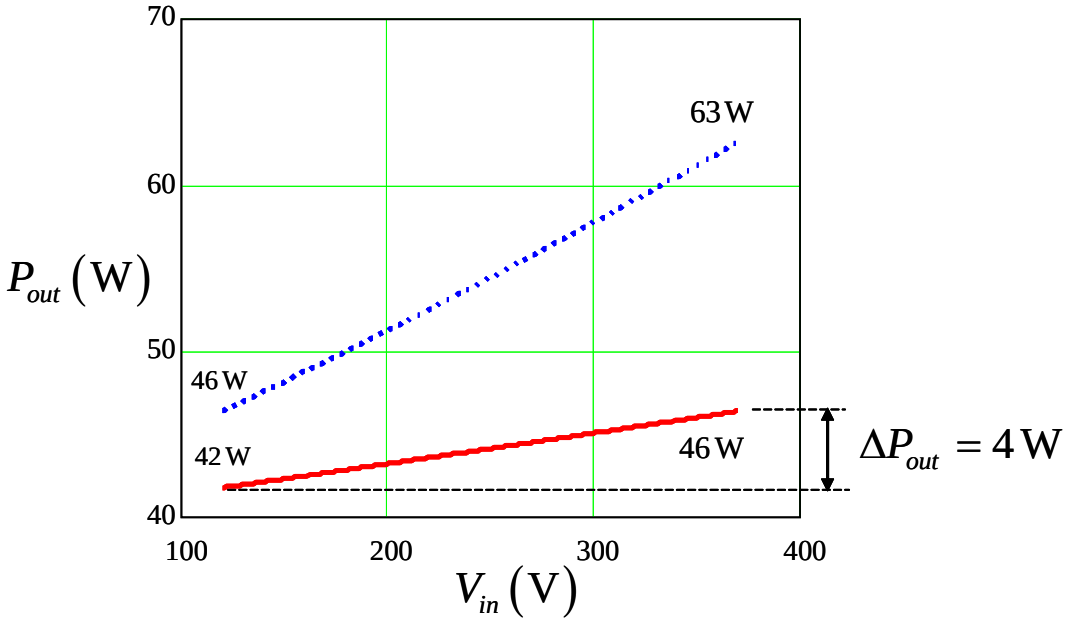

Fig. 10. OPP implementation clearly improves the output-power limiting of the flyback converter.

Owing to a linear variation of the compensation level, the delivered power stays within control. It does not exceed 4 W between the two input-voltage extremes. This nondissipative OPP technique has also been implemented in a high-voltage switcher, the NCP1027.

Conclusion

In this first part of this article, we have explained why a flyback converter operated in the discontinuous conduction mode can deliver more power at high line than at low line. With moderate power adapters, this extra power is not detrimental to converter operation. However, when adapters of higher power levels must comply with the Limited Power Source specifications, it is important to understand the phenomenon at play and minimize its impacts on final performance. Two compensation techniques have been disclosed. The second technique is implemented in the NCP1250 and offers excellent performance without increasing power dissipation.

References

UL60950-1, Information Technology Equipment – Safety – Part 1: General Requirements.

About the Author

Christophe Basso is an application engineering director at ON Semiconductor in Toulouse, France. He has originated numerous integrated circuits among which the NCP120X series has set new standards for low standby power converters. SPICE simulation is also one of his favorite subjects and he authored a second book, "Switch-Mode Power Supplies: SPICE Simulations and Practical Designs", published by McGraw-Hill in 2008. His work was positively reviewed in several magazines and in a recent PELS newsletter. Christophe holds a BSEE-equivalent from the Montpellier University, France and a MSEE from the Institut National Polytechnique de Toulouse, France. He holds 17 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on power protection, see the How2Power Design Guide, search the Design Area category and select Power Protection as the subcategory.