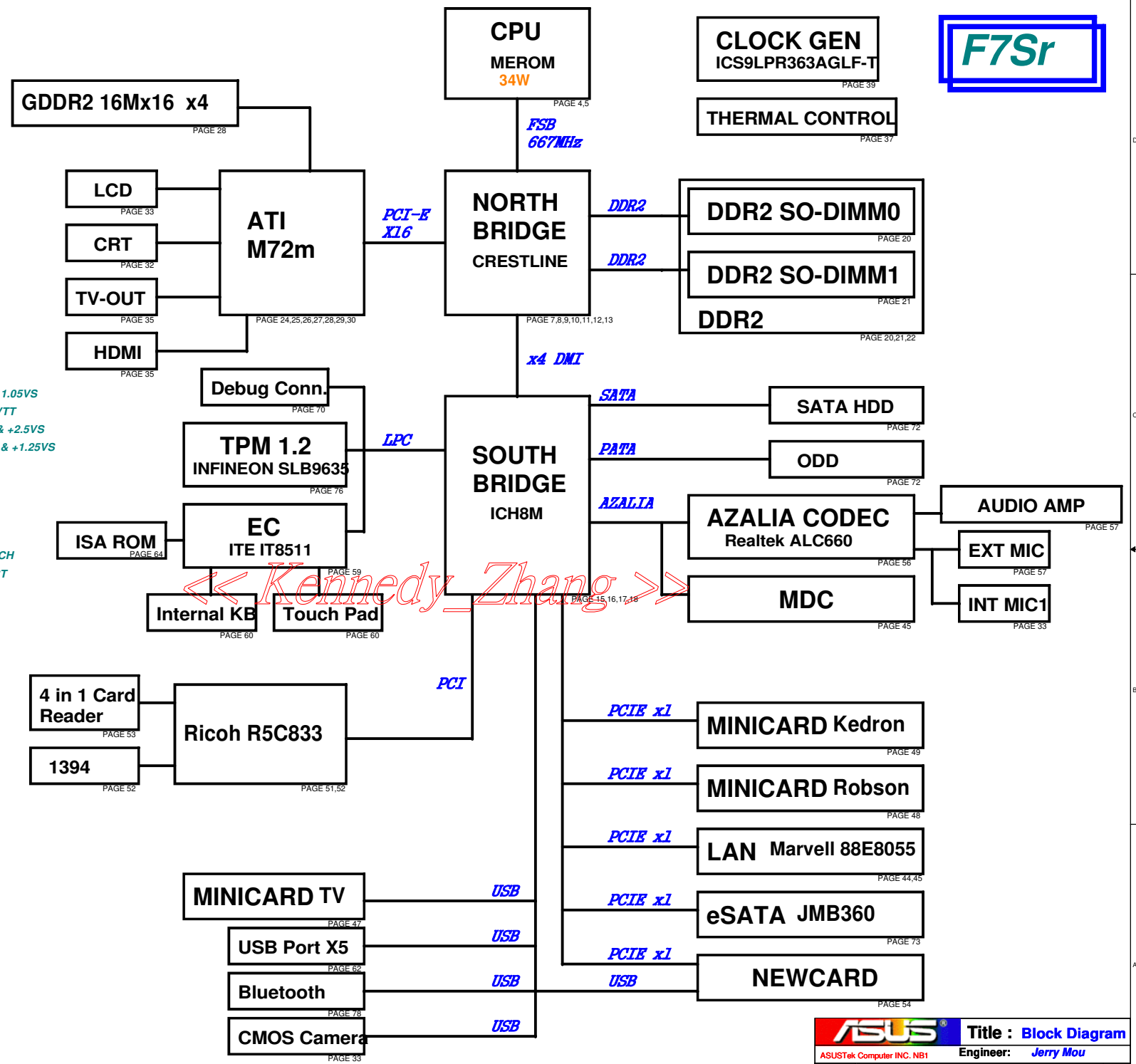


01	Block Diagram	61	*
02	System Setting	62	USB CONN
03	*	63	*
04	04_CPU-Merom(HOST)	64	ISA ROM
05	05_CPU-Merom(PWR)	65	SPI ROM
06	*	66	LED
07	07_CRESTLINE(HOST)	67	*
08	08_CRESTLINE(DMI & CFG)	68	DC & BAT IN
09	09_CRESTLINE(GRAPHIC)	69	*
10	10_CRESTLINE(DDR2)	70	Debug CONN.
11	11_CRESTLINE(PWR)	71	*
12	12_CRESTLINE(PWR2)	72	SATA-HDD & ODD
13	13_CRESTLINE(GND)	73	eSATA
14	*	74	SREW HOLE
15	15_SB-ICH8M(1)	75	*
16	16_SB-ICH8M(2)	76	TPM
17	17_SB-ICH8M(3)	77	SPRING_PAD
18	18_SB-ICH8M(PWR)	78	BT
19	*	79	POWER SEQUENCE
20	20_DDR2 SO-DIMM0	80	POWER_VCORE
21	21_DDR2 SO-DIMM1	81	POWER_SYSTEM
22	22_DDR2 TERMINATION	82	POWER_I/O_1.5VS & 1.05VS
23	*	83	POWER_I/O_DDR & VTT
24	24_VGA_ATL_M7X/66-M_MAIN(1)	84	POWER_I/O_+3VAO & +2.5VS
25	25_VGA_ATL_M7X/66-M_Memory(2)	85	POWER_VGA_CORE & +1.25VS
26	26_VGA_ATL_M7X/66-M_PCI-E(3)	86	N/A
27	VGA_ATL_M7X/66-M_POWER(4)	87	N/A
28	VGA_ATL_M7X/66-M_VRAM_A(5)	88	POWER_CHARGER
29	VGA_ATL_M7X/66-M_VRAM_B(6)	89	N/A
30	VGA_SPI_ROM (7)	90	POWER_DETECT
31	*	91	POWER_LOAD SWITCH
32	CRT	92	POWER_FLOWCHART
33	LVDS & INVERTER CONNECTOR	93	POWER_PROTECT
34	*	94	POWER_SIGNAL
35	TV OUT CONN	95	History
36	*		
37	THEIR SENSOR & FAN		
38	*		
39	CLOCK GEN-ICS9LPR363AGLF-T		
40	*		
41	Power on & Reset Freq.		
42	DISCHARGE		
43	*		
44	LAN-L1		
45	MDC & RJ45+11		
46	*		
47	MINI CARD-TV/Windigo		
48	MINI CARD-Robson		
49	MINI CARD-Kedron		
50	*		
51	CARD1394-R5C833(1)		
52	CARD1394-R5C833(2)		
53	4 in 1 CARD READER		
54	NEWCARD		
55	*		
56	CODEC-ALC660		
57	AUDIO AMP & JCAK		
58	Sequence Control Logic		
59	IT8511TE		
60	Touch Pad & KB		



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EC_IT8511TE SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCR_L_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	BUF_PLT_RST#	I
31	ECSC#/GPD3	EXT_SC#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWR5W/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	PM_SLP_M#	
110	PS2CLK0/GPF0	WALN_SW#	
111	PS2DAT0/GPF1	ME_ALERT#	
114	PS2CLK1/GPF2	/	I/O
115	PS2DAT1/GPF3	/	I/O
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	FA19	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80HL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
8	GPL0	PM_S4_STATE#	I	152	GPI2	/	
11	GPL1	S4_STATE_ON	O	155	GPI3	CHG_EN#	O
12	GPL2	SLP_M_ON	O	168	GPI5	EC_CLK_EN	O
20	GPL3	EC_WLAN_PWR	O	85	KS016/GPM2	NETDETECT	O
21	GPL4	MP_PWRGD	I				
48	GPH0	VSUS_ON	I				
54	GPH1	VSUS_GD#	O				
55	GPH2	CPUPWR_GD#	O				
69	GPH3	PM_PWRBTN#	O				
70	GPH4	SUSC_ON	O				
75	GPH5	SUSB_ON	O				
76	GPH6	CPU_VRON	O				
105	GPH7	PM_RSMRST#	O				
148	GPI0	ICH8_PWROK	O				
149	GPI1	ALL_SYSTEM_PWRGD	I				

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	A
1394	AD17	0	B

PCIe Device	Bus	PCIe Device	Bus
LAN	PE(T/R)(p/n)1	Robson	PE(T/R)(p/n)4
Kedron	PE(T/R)(p/n)2	NEWCARD	PE(T/R)(p/n)5
eSATA	PE(T/R)(p/n)3	GLAN	PE(T/R)(p/n)6

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor(MAX6657)	0100110x (4C)
VGA Thermal Sensor(MAX6657)	0100110x (4C)

ICH8-M GPIO SETTING

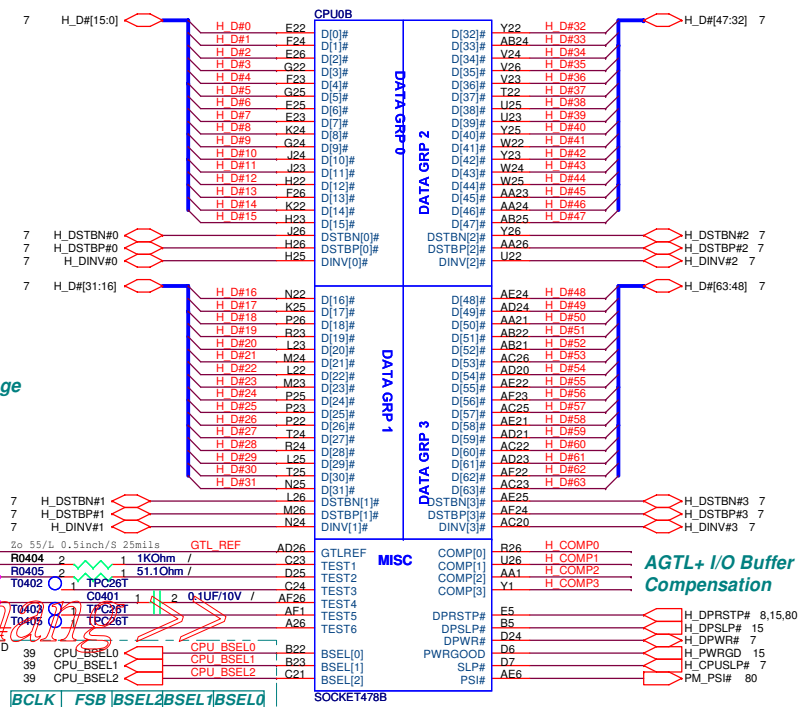
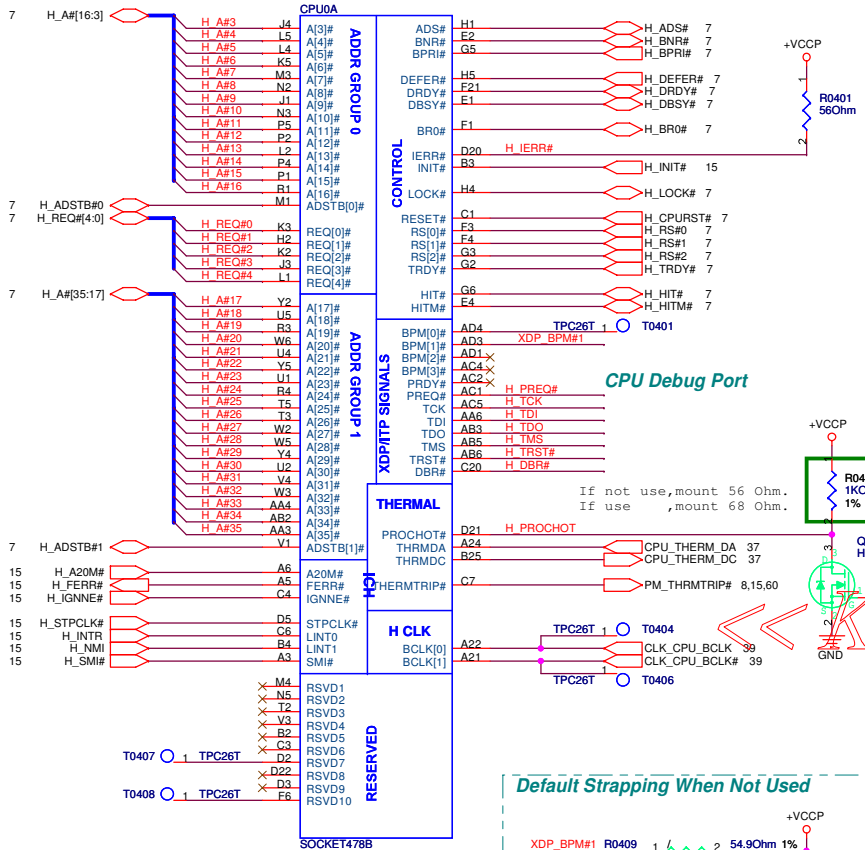
Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
AG12	GPIO0/BM_BUSY#	PM_BMBUSY#	I	AG16	GPIO40/OC#1	USB_CON_OC01#	I
AJ8	GPIO1/TACH1	EXTSMI#	I	AG15	GPIO41/OC#2	USB_CON_OC23#	I
F8	GPIO2/PIRQE#	PCI_INTE#	I	AE15	GPIO42/OC#3	USB_CON_OC23#	I
G11	GPIO3/PIRQF#	PCI_INTF#	I	E18	GPIO50/REQ1#	PCI_REQ#1	
F12	GPIO4/PIRQG#	PCI_INTG#	I	C18	GPIO51/GNT1#	PCI_GNT#1	
B3	GPIO5/PIRQH#	PCI_INTH#	I	B19	GPIO52/REQ2#	PCI_REQ#2	
AJ9	GPIO6/TACH2	BIOS_REC	I/O	F18	GPIO53/GNT2#	PCI_GNT#2	
AH9	GPIO7/TACH3	WLAN_LED_EN	I	A11	GPIO54/REQ3#	PCI_REQ#3	
AE16	GPIO8	BT_ON#	I	C10	GPIO55/GNT3#	PCI_GNT#3	
AG19	GPIO9/WOL_EN	LAN_WOL_EN	I				
AJ24	GPIO10/CLGPIO1	ME_ALERT#	O				
AG22	GPIO11/SMBALERT#	SMB_ALERT#	I				
AC19	GPIO12	KBC_SC#	I				
AH21	GPIO13/GLAN_DOCK#	NETDETECT					
AF22	GPIO14/CLGPIO2	STP_PCI#	I/O				
AE20	GPIO15/STP_PCI#	PM_DPRSPLVR	O				
AJ14	GPIO16/DPRSPLVR	WLAN_ON#	O				
AG8	GPIO17/TACH0	TP_LEDON	O				
AH12	GPIO18	PCB_ID0	I				
AJ10	GPIO19/SATA1GP	BTLED_ON	O				
AE11	GPIO20	CPU_Select	I				
AJ12	GPIO21/SATA0GP	3G_ON#	I				
AG10	GPIO22/SCLOCK	LPC_DRQ#1	I/O				
E6	GPIO23/LDRQ1#	STP_CPU#					
AJ27	GPIO24/CLGPIO0	PM_S4_STATE#					
AG18	GPIO25/STP_CPU#	BT_DET#	I				
AH27	GPIO26/S4_STATE#	CB_SD#					
AH25	GPIO27/QRT_STATE0	USB_CON_OC5#	I				
AD16	GPIO28/QRT_STATE1	NEWCARD_OC#	I				
AG17	GPIO29/OC#5	USB_OC#7	I				
AD12	GPIO30/OC#6	PM_CLKRUN#	O				
AJ18	GPIO31/OC#7	GPO35	O				
AH11	GPIO32/CLKRUN#	PCB_ID1	I/O				
AE10	GPIO33/AZ_DOCK_EN#	PCB_ID2	I/O				
AG14	GPIO34/AZ_DOCK_RST#	GPI38	I				
AG13	GPIO35/SATACLKREQ#	GPI39	I				
AF11	GPIO36/SATA2GP	PCI_GNT#4	O				
AG11	GPIO37/SATA3GP	H_PWRGD	O				
AF9	GPIO38/SLOAD						
AJ11	GPIO39/SDATAOUT0						
AD10	GPIO48/SDATAOUT1						
AG29	GPIO49/CPUPWRGD						

ICS9LPR363AGLF-T SETTING

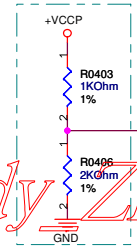
Pins	Pin Name	Device
3	PCICLK1	TPMPCI
4	PCICLK2	CardBus R5C832
5	SELPCIEX0_LCD#PCICLK3	EC IT8511E
8	ITP_EN/PCICLK_F0	ICH8
15	DOTC_96MHzL	X
14	DOTT_96MHzL	X
12	FSLA/USB_48MHz	ICH8
19	PCIeT_L1	eSATA
20	PCIeC_L1	eSATA
36	PCIeT_L5	M66M
35	PCIeC_L5	M66M
39	PCIeT_L6	MiniCard(Rob)
38	PCIeC_L6	MiniCard(Rob)
22	PCIeT_L2	ICH8
23	PCIeC_L2	ICH8
24	PCIeT_L3	MCH
25	PCIeC_L3	MCH
26	SATACLKT_L	ICH8
27	SATACLKC_L	ICH8
44	CPUITPT_L2 / PCIeT_L8	LAN
43	CPUITPC_L2 / PCIeC_L8	LAN
14	27FIX/LCD_SSCGT/PCIeT_L0M72M	
15	DOTC_96MHzL	M72M
41	PEREQ1# / PCIeT_L7	MiniCard
40	PEREQ2# / PCIeC_L7	MiniCard
32	PEREQ3#	NewCard
33	PEREQ4#	MiniCard
30	PCIeT_L4	NewCard
31	PCIeC_L4	NewCard
49	CPUT_L1F	MCH
48	CPUC_L1F	MCH
52	CPUT_L0	CPU
51	CPUC_L0	CPU
57	X2	14.318MHz
58	X1	14.318MHz
60	REF0	ICH8
61	REF1/FSLC/TEST_SEL	X

		Title : GPIO setting	
ASUSTek Computer INC. NBI		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	F7Sr	1.1	
Date: 2007.05.10		Sheet 2 of 95	

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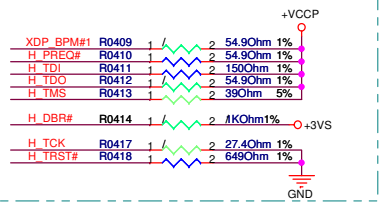


AGTL+ I/O Voltage Reference

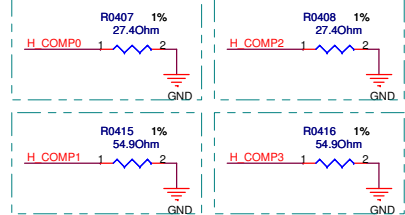


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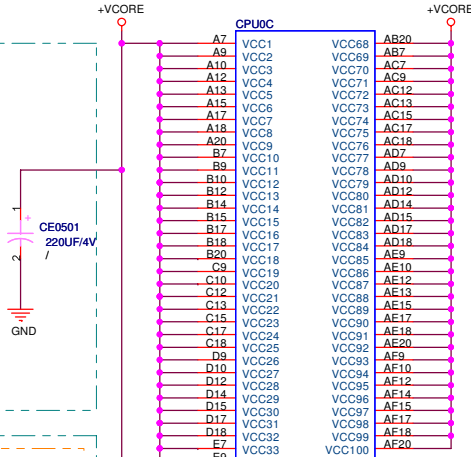
Default Strapping When Not Used



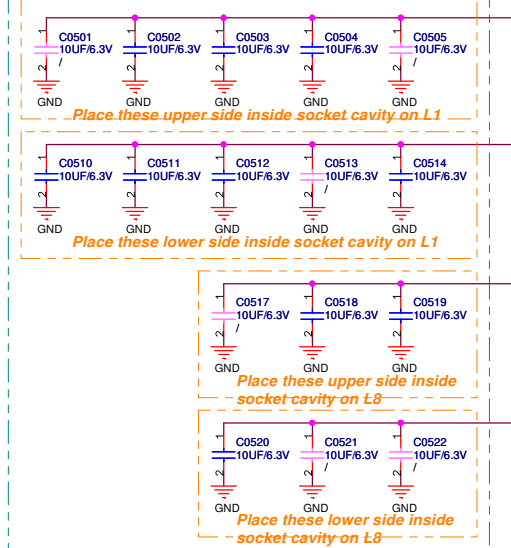
AGTL+ I/O Buffer Compensation



**CPU + VCORE
Bulk-Decoupling
Capacitors**

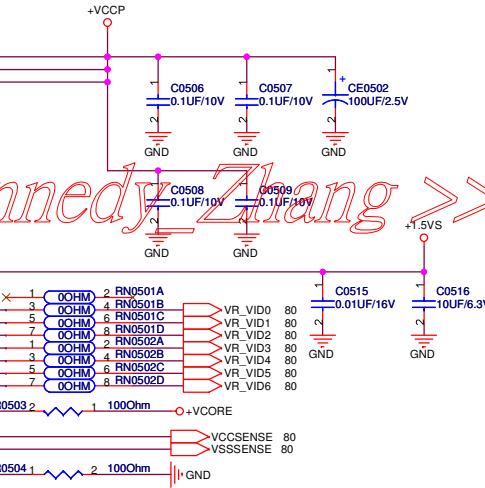


**CPU + VCORE
Mid-Frequency
Capacitors**



+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
F3S: 10UF *16
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
F3S: 100UF *1, 0.1UF *4

A7	VCC1	VCC68	AB20
A9	VCC2	VCC69	AB7
A10	VCC3	VCC70	AC2
A12	VCC4	VCC71	AC9
A13	VCC5	VCC72	AC12
A15	VCC6	VCC73	AC13
A17	VCC7	VCC74	AC15
A18	VCC8	VCC75	AC17
A20	VCC9	VCC76	AD7
B7	VCC10	VCC77	AD9
B9	VCC11	VCC78	AD10
B10	VCC12	VCC79	AD12
B12	VCC13	VCC80	AD14
B14	VCC14	VCC81	AD15
B15	VCC15	VCC82	AD17
B17	VCC16	VCC83	AD18
B18	VCC17	VCC84	AE9
B20	VCC18	VCC85	AE10
C9	VCC19	VCC86	AE12
C10	VCC20	VCC87	AE13
C12	VCC21	VCC88	AE15
C13	VCC22	VCC89	AE17
C15	VCC23	VCC90	AE18
C17	VCC24	VCC91	AE20
C18	VCC25	VCC92	AF9
D9	VCC26	VCC93	AF10
D10	VCC27	VCC94	AF12
D12	VCC28	VCC95	AF14
D14	VCC29	VCC96	AF15
D15	VCC30	VCC97	AF17
D17	VCC31	VCC98	AF18
D18	VCC32	VCC99	AF20
E7	VCC33	VCC100	
E9	VCC34	VCCP1	G21
E10	VCC35	VCCP2	J6
E12	VCC36	VCCP3	K6
E13	VCC37	VCCP4	M6
E15	VCC38	VCCP5	J21
E17	VCC39	VCCP6	K21
E18	VCC40	VCCP7	M21
F20	VCC41	VCCP8	N21
F7	VCC42	VCCP9	N22
F9	VCC43	VCCP10	R22
F10	VCC44	VCCP11	R26
F12	VCC45	VCCP12	T2
F14	VCC46	VCCP13	T9
F15	VCC47	VCCP14	W21
F17	VCC48	VCCP15	W21
F18	VCC49	VCCP16	
F20	VCC50	VCCP16	
AA7	VCC51	VCCA1	B26
AA9	VCC52	VCCA2	C26
AA10	VCC53		
AA12	VCC54		
AA13	VCC55	VID[0]	AD6 H_VID0 1
AA15	VCC56	VID[1]	AE5 H_VID1 3
AA17	VCC57	VID[2]	AE5 H_VID2 5
AA18	VCC58	VID[3]	AE5 H_VID3 7
AA20	VCC59	VID[4]	AE3 H_VID4 1
AB9	VCC60	VID[5]	AE3 H_VID5 3
AC10	VCC61	VID[6]	AE2 H_VID6 5
AB10	VCC62		
AB12	VCC63		
AB14	VCC64		
AB15	VCC65		
AB17	VCC66		
AB18	VCC67		



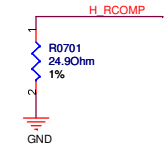
CPU0D

A4	VSS1	VSS82	P6
A8	VSS2	VSS83	P21
A11	VSS3	VSS84	P24
A14	VSS4	VSS85	R2
A16	VSS5	VSS86	R5
A19	VSS6	VSS87	R22
A23	VSS7	VSS88	R25
AF2	VSS8	VSS89	T1
B6	VSS9	VSS90	T4
B8	VSS10	VSS91	T23
B11	VSS11	VSS92	T26
B13	VSS12	VSS93	U3
B16	VSS13	VSS94	U6
B19	VSS14	VSS95	U21
B21	VSS15	VSS96	U24
B24	VSS16	VSS97	V2
C5	VSS17	VSS98	V5
C8	VSS18	VSS99	V22
C11	VSS19	VSS100	V25
C14	VSS20	VSS101	W1
C16	VSS21	VSS102	W4
C19	VSS22	VSS103	W23
C2	VSS23	VSS104	W26
C22	VSS24	VSS105	Y3
C25	VSS25	VSS106	Y2
D4	VSS26	VSS107	Y24
D8	VSS28	VSS109	AA2
D11	VSS29	VSS110	AA5
D13	VSS30	VSS111	AA8
D16	VSS31	VSS112	AA11
D19	VSS32	VSS113	AA14
D23	VSS33	VSS114	AA16
D26	VSS34	VSS115	AA19
E3	VSS35	VSS116	AA22
E8	VSS36	VSS117	AA25
E11	VSS37	VSS118	AB1
E14	VSS38	VSS119	AB4
E16	VSS39	VSS120	AB8
E19	VSS40	VSS121	AB11
E21	VSS41	VSS122	AB13
E24	VSS42	VSS123	AB16
F5	VSS43	VSS124	AB19
F8	VSS44	VSS125	AB23
F11	VSS45	VSS126	AB26
F13	VSS46	VSS127	AC3
F16	VSS47	VSS128	AC6
F19	VSS48	VSS129	AC8
F2	VSS49	VSS130	AC11
F22	VSS50	VSS131	AC16
F25	VSS51	VSS132	AC19
G4	VSS52	VSS133	AC21
G11	VSS53	VSS134	AC24
G23	VSS54	VSS135	AD2
G26	VSS55	VSS136	AD5
H3	VSS56	VSS137	ADR
H6	VSS57	VSS138	AD11
H21	VSS58	VSS139	AD13
H24	VSS59	VSS140	AD16
J2	VSS60	VSS141	AD19
J5	VSS61	VSS142	AD22
J22	VSS62	VSS143	AD25
J25	VSS63	VSS144	AE1
K1	VSS64	VSS145	AE4
K4	VSS65	VSS146	AE8
K23	VSS66	VSS147	AE11
K26	VSS67	VSS148	AE14
L6	VSS68	VSS149	AE16
L12	VSS69	VSS150	AE19
L21	VSS70	VSS151	AE23
L24	VSS71	VSS152	AE26
M2	VSS72	VSS153	A2
M5	VSS73	VSS154	AF6
M22	VSS74	VSS155	AF9
M25	VSS75	VSS156	AF11
N1	VSS76	VSS157	AF13
N4	VSS77	VSS158	AF16
N23	VSS78	VSS159	AF19
N26	VSS79	VSS160	AF21
P3	VSS80	VSS161	A25
	VSS81	VSS162	AF25
		VSS163	

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RCOMP

For Calibrating the FSB I/O Buffer



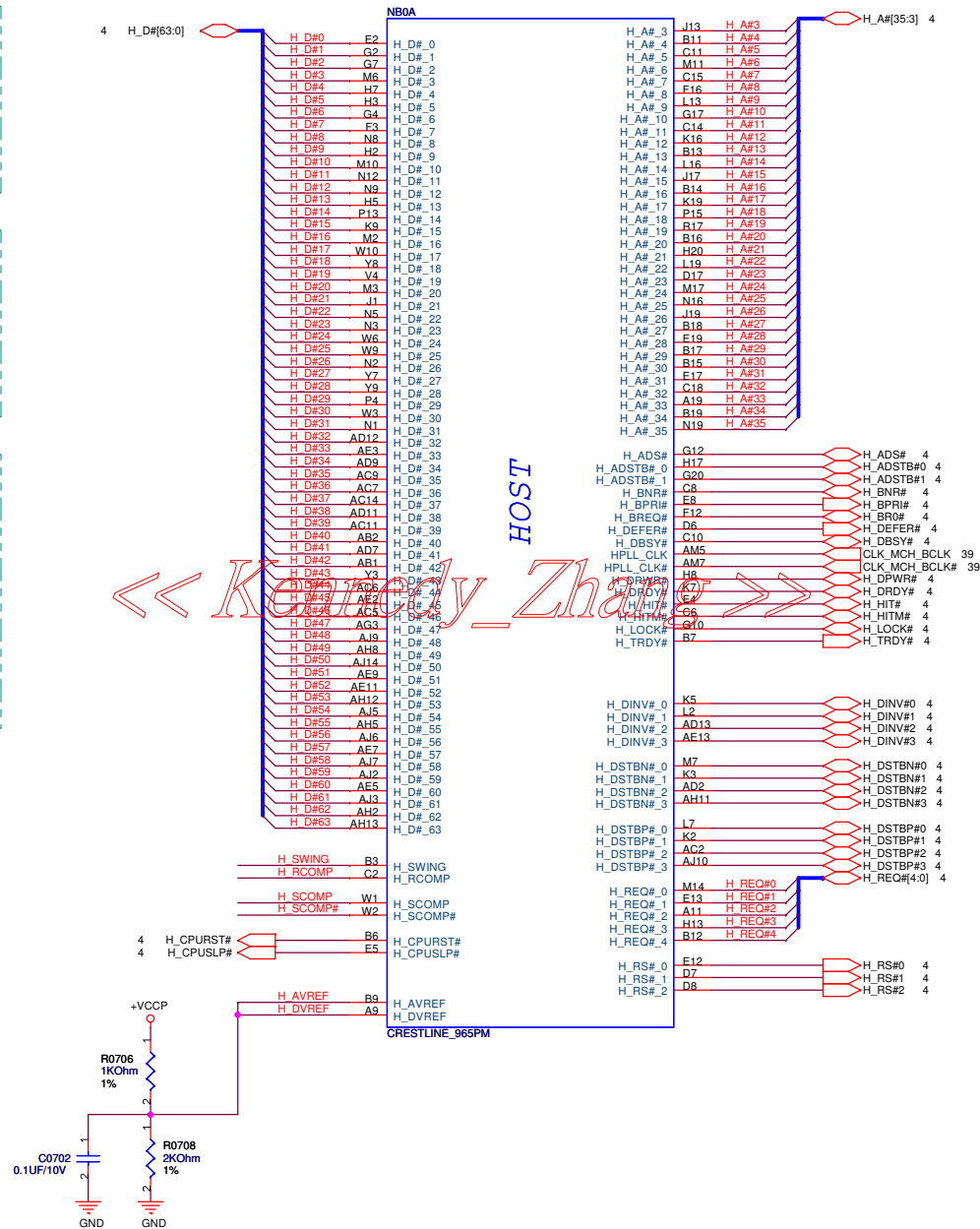
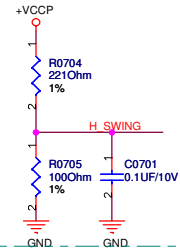
SCOMP

For Slew Rate Compensation on the FSB

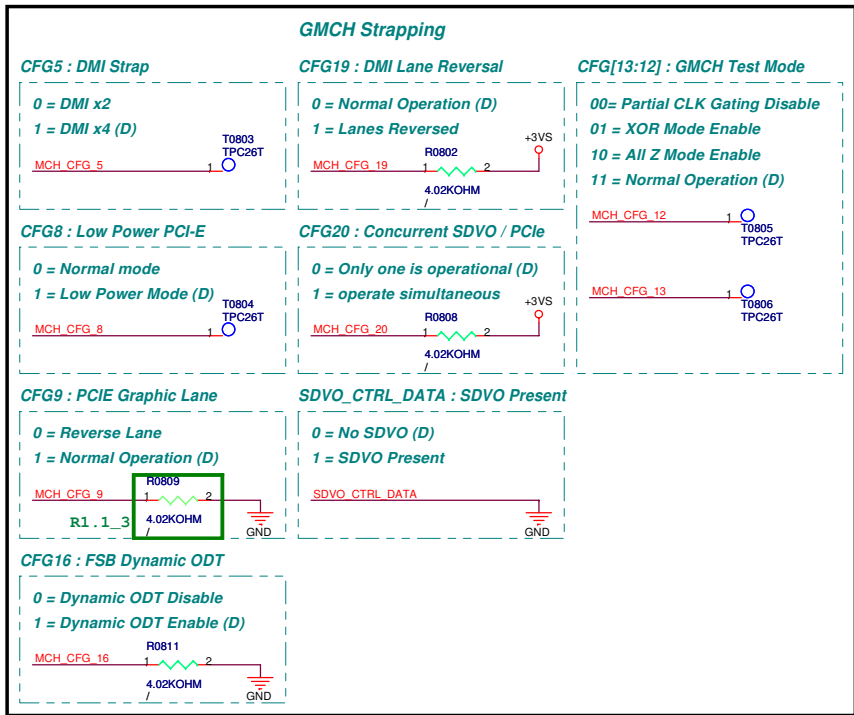


Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits

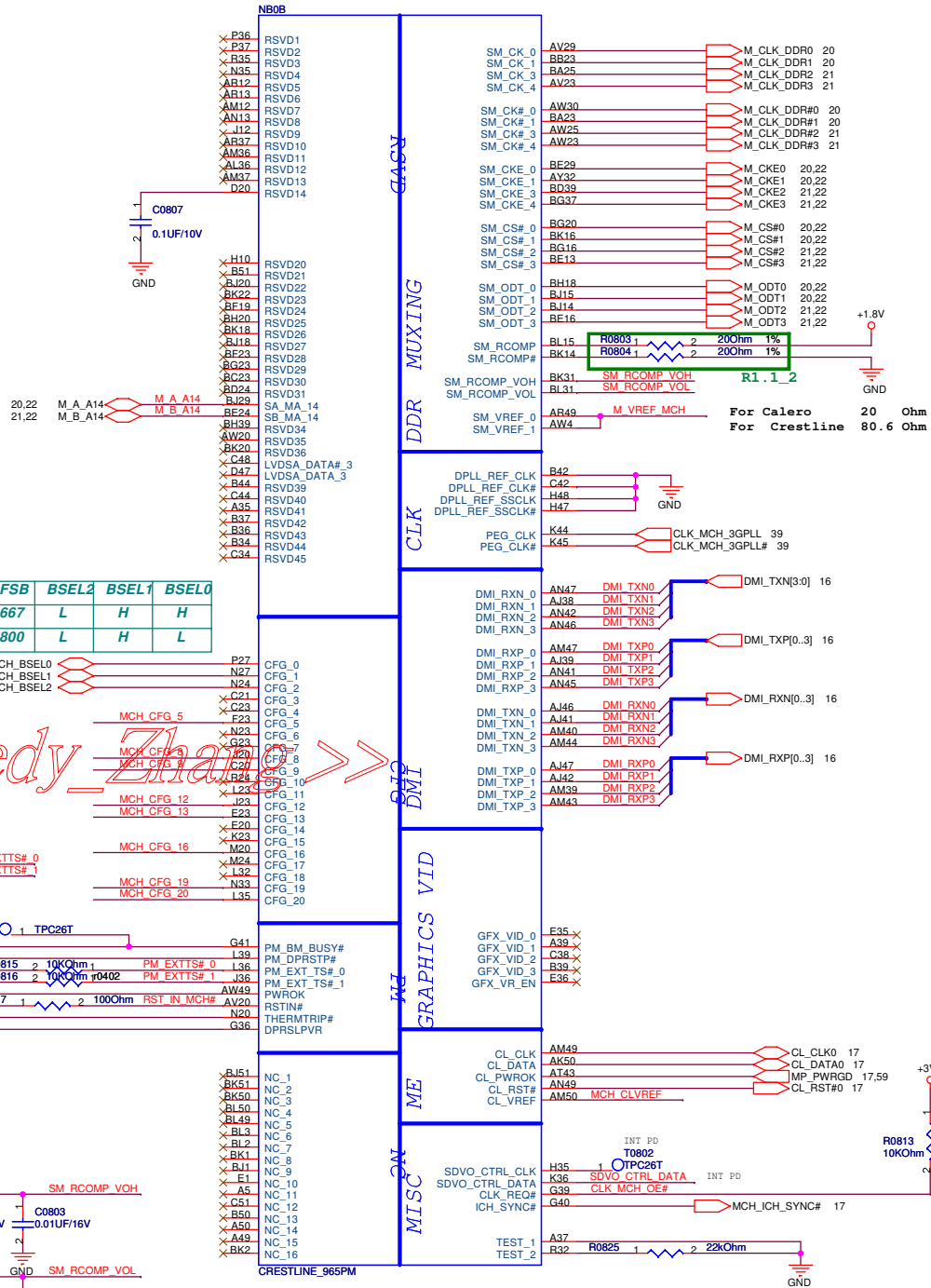
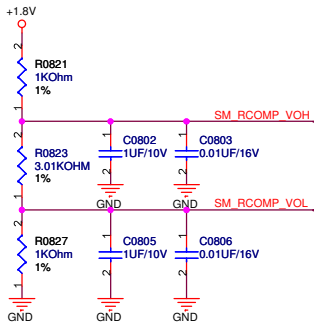
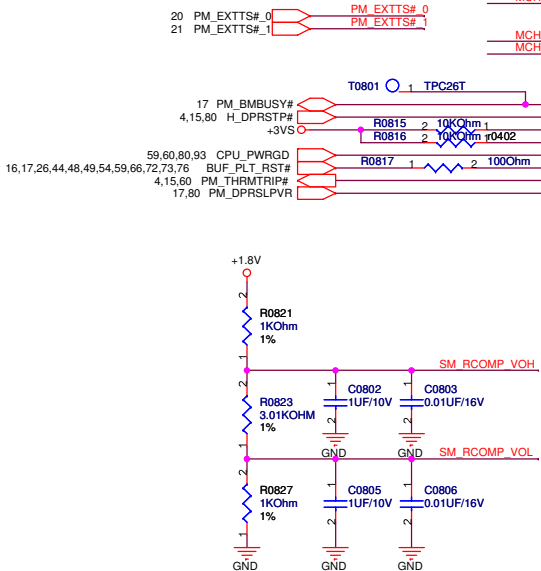
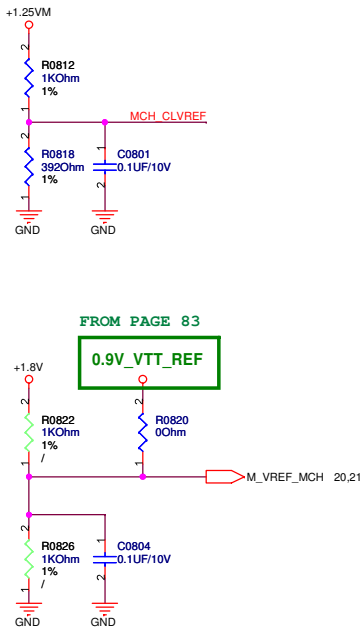


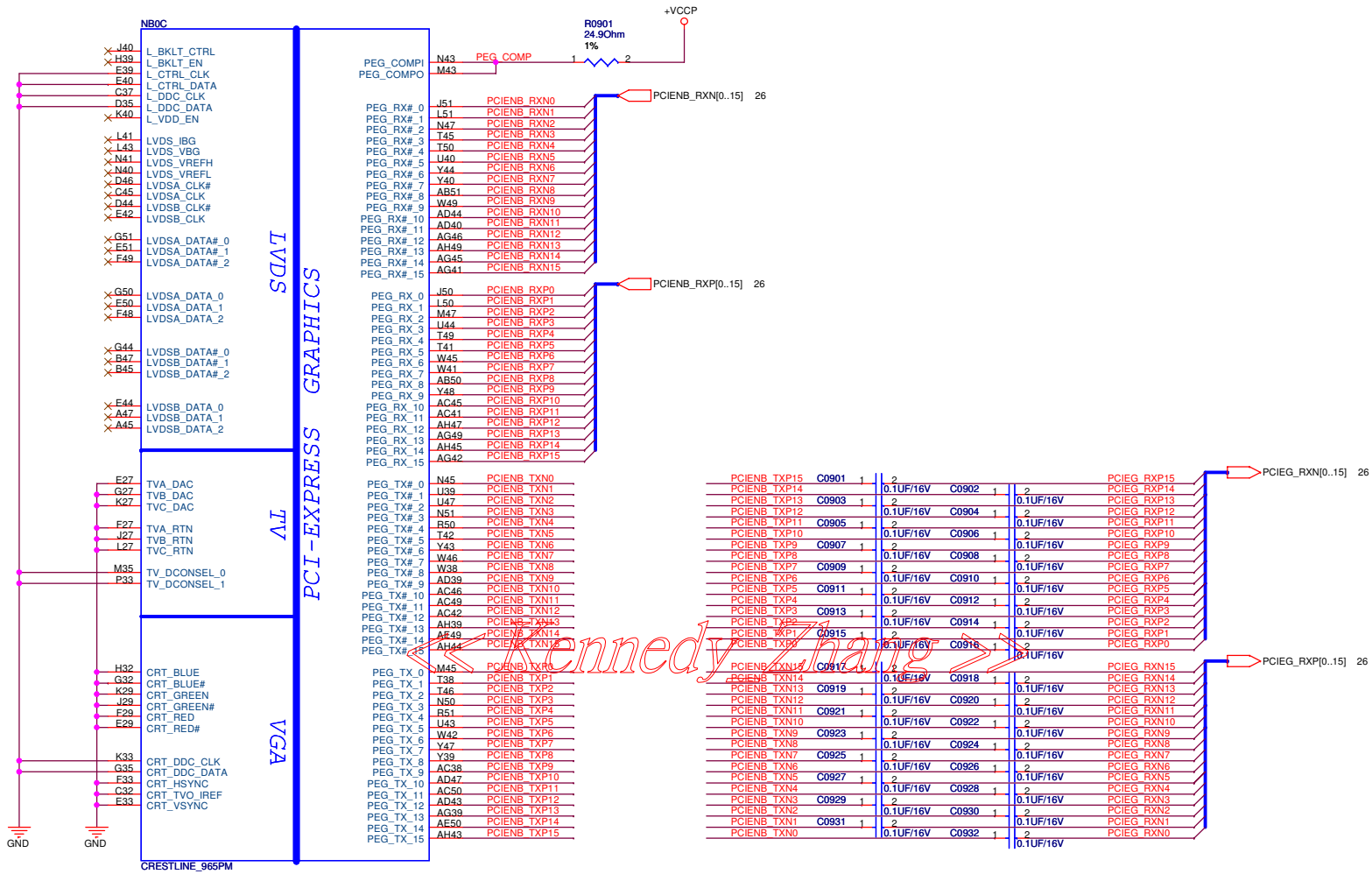
« Koolhaan Zhong »



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L

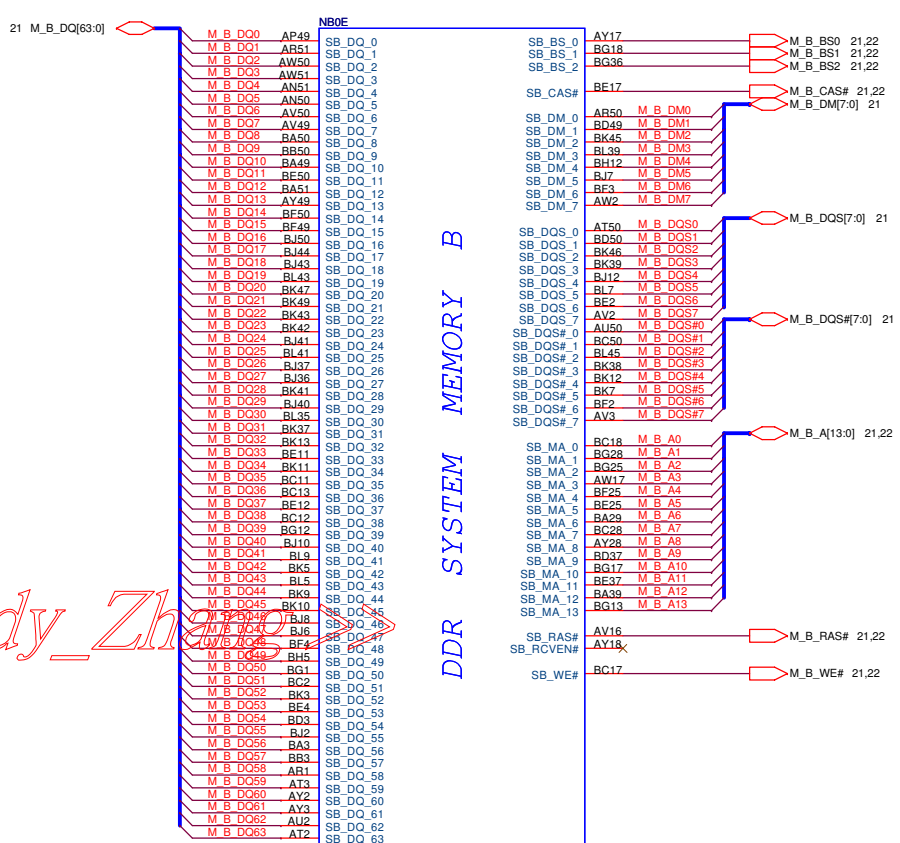
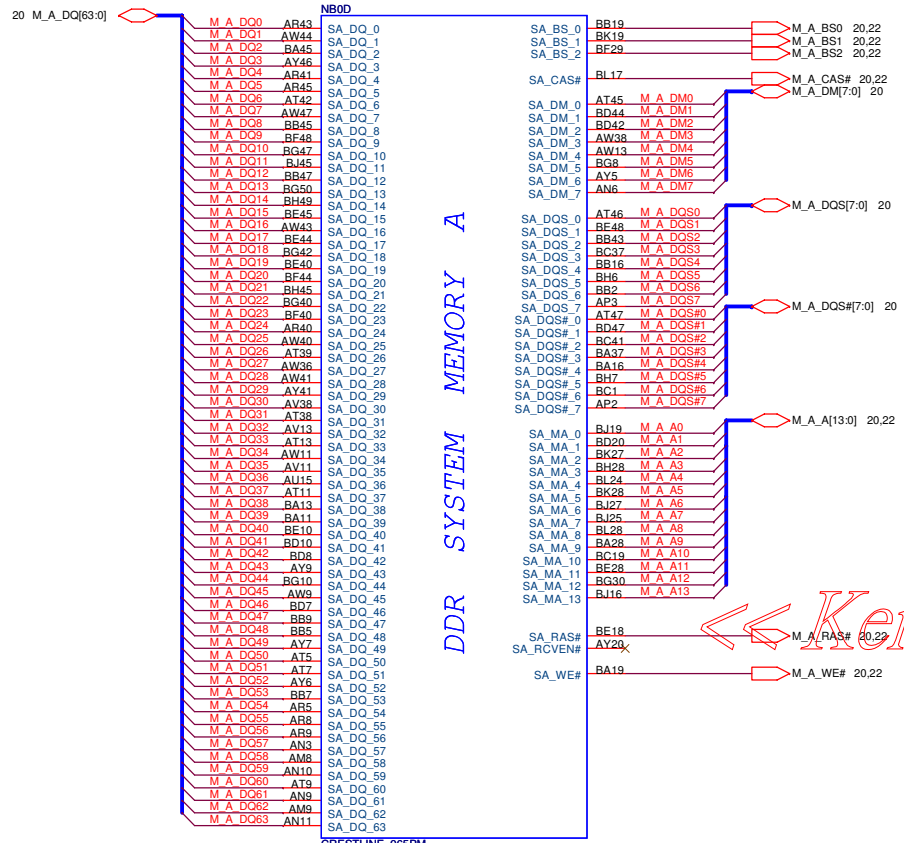
<< Kennedy_Zhai >>



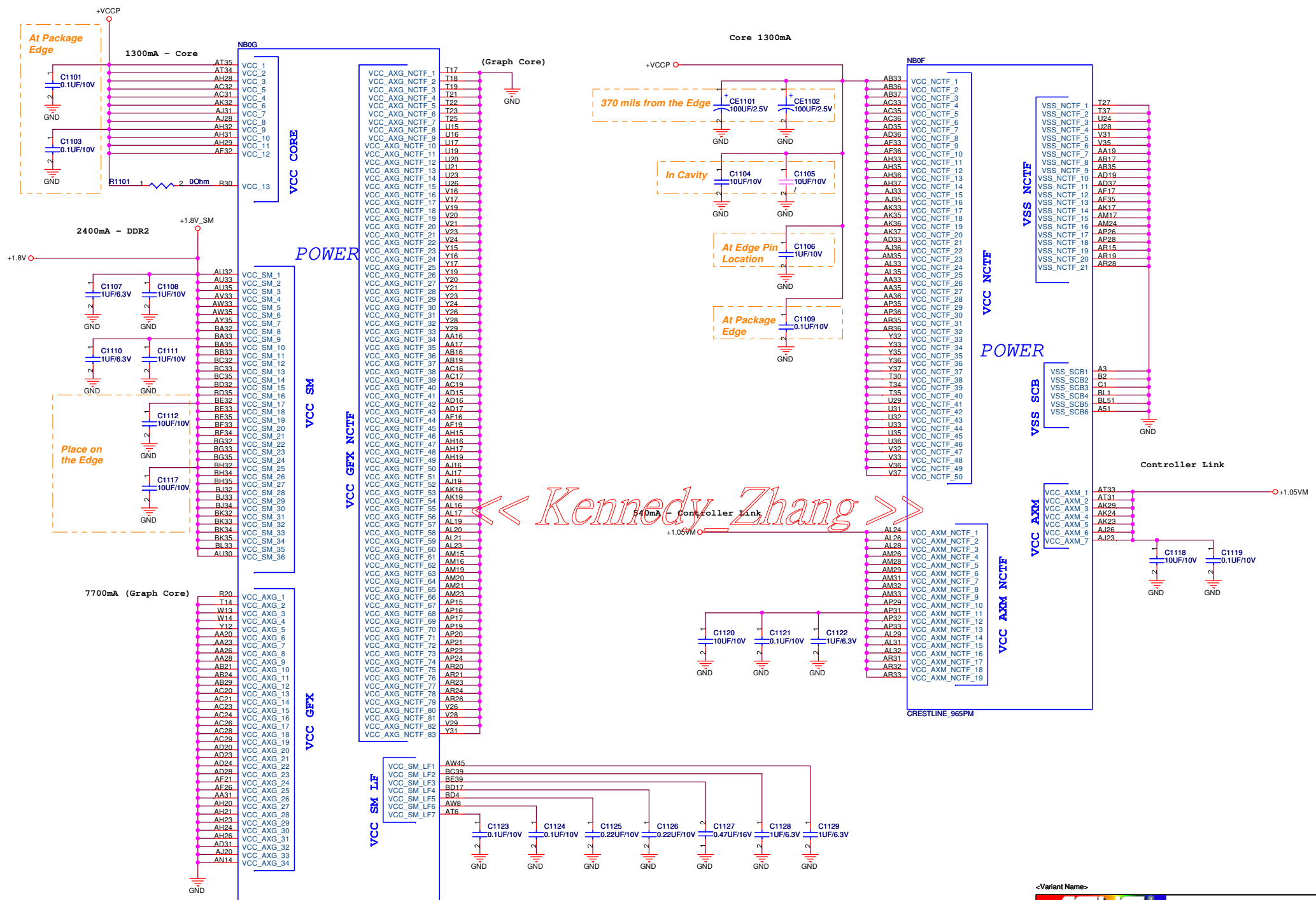


<Variant Name>

ASUS		Title : NB_965PM(GRAPHIC)	
ASUSTeK COMPUTER INC. NBI		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	F7Sr	1.1	
Date: 2007.05.10	Sheet	9	of 95



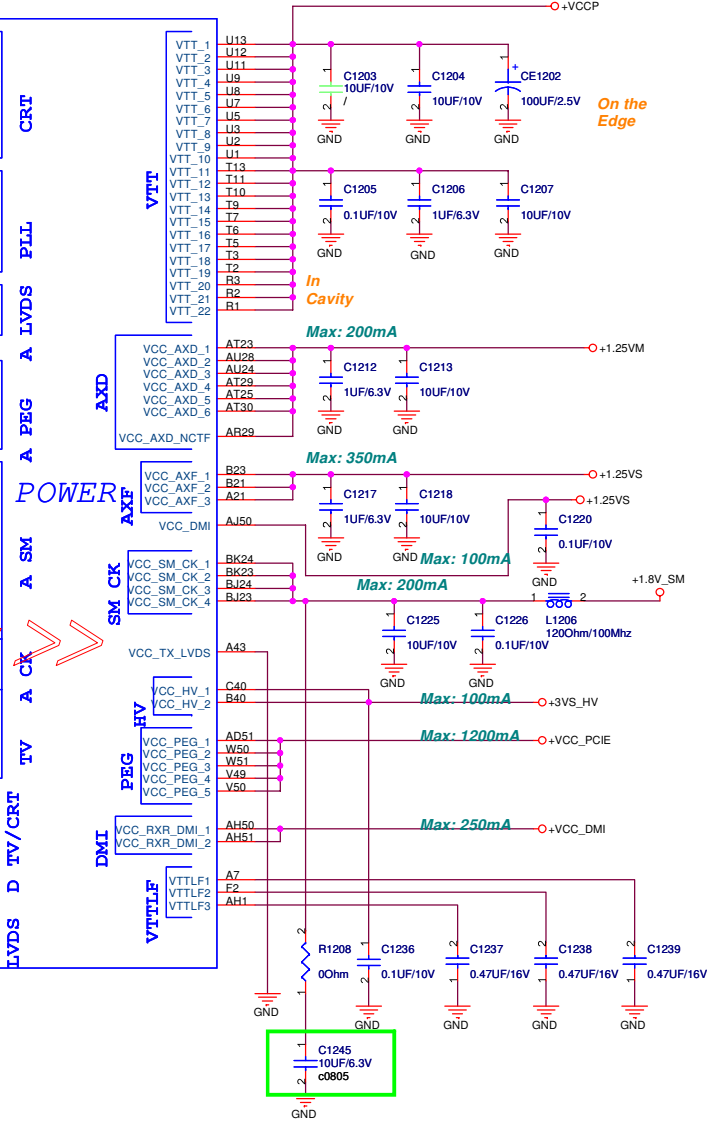
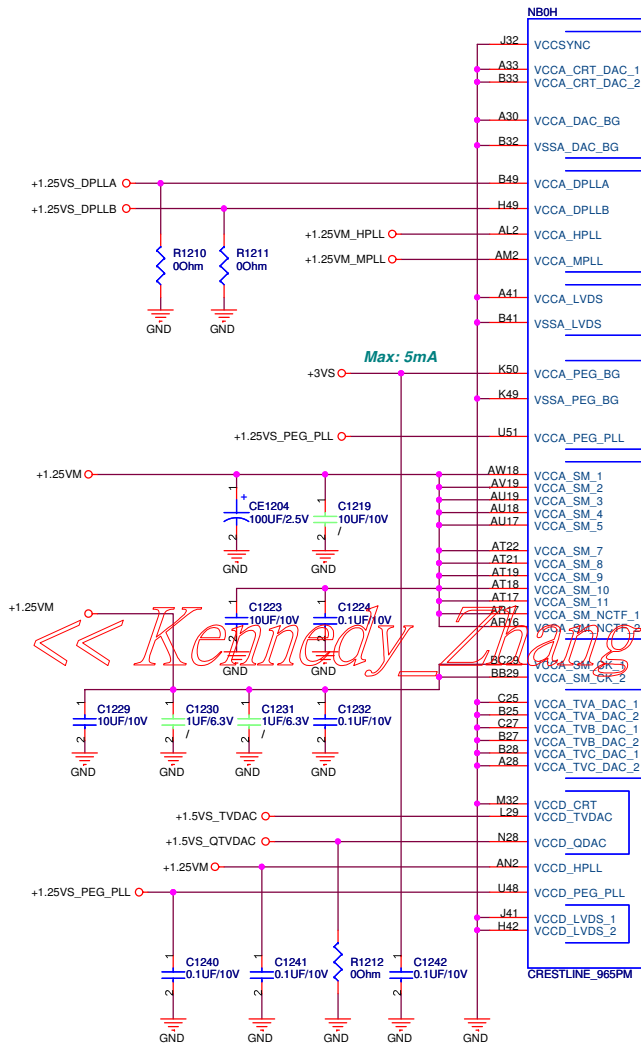
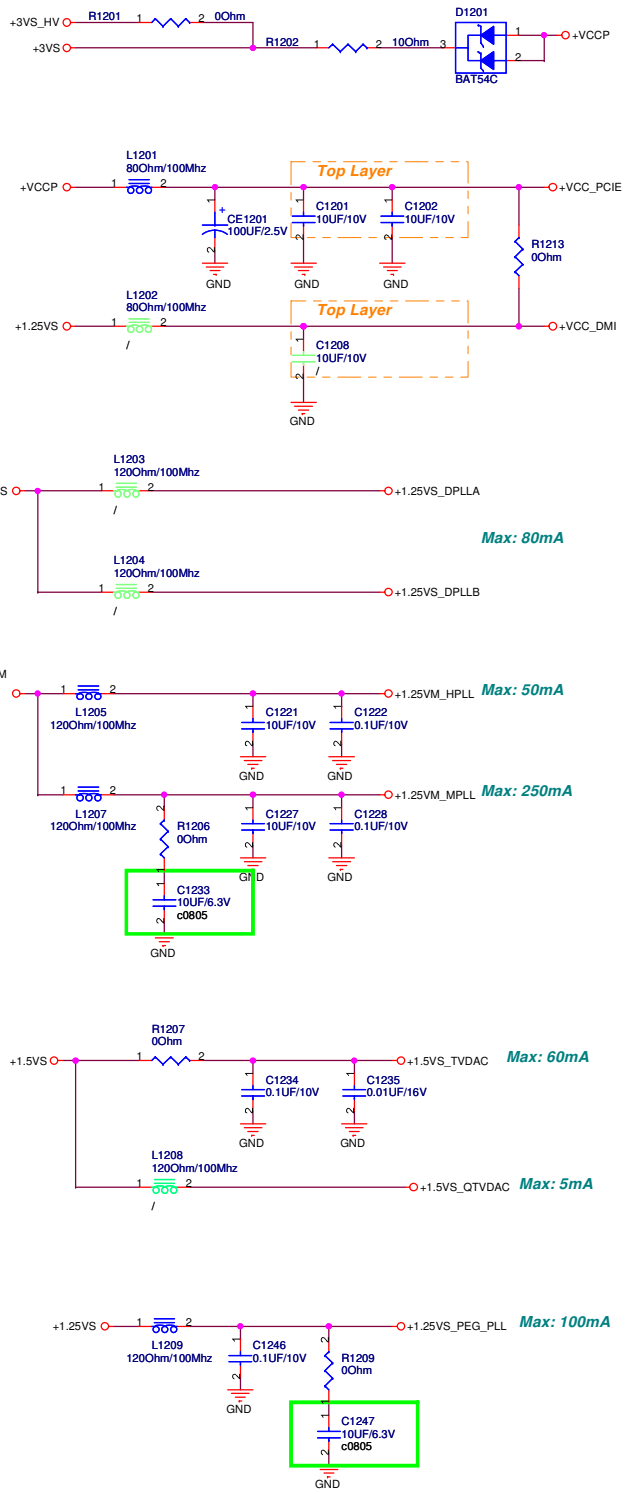
Kennedy_Zh



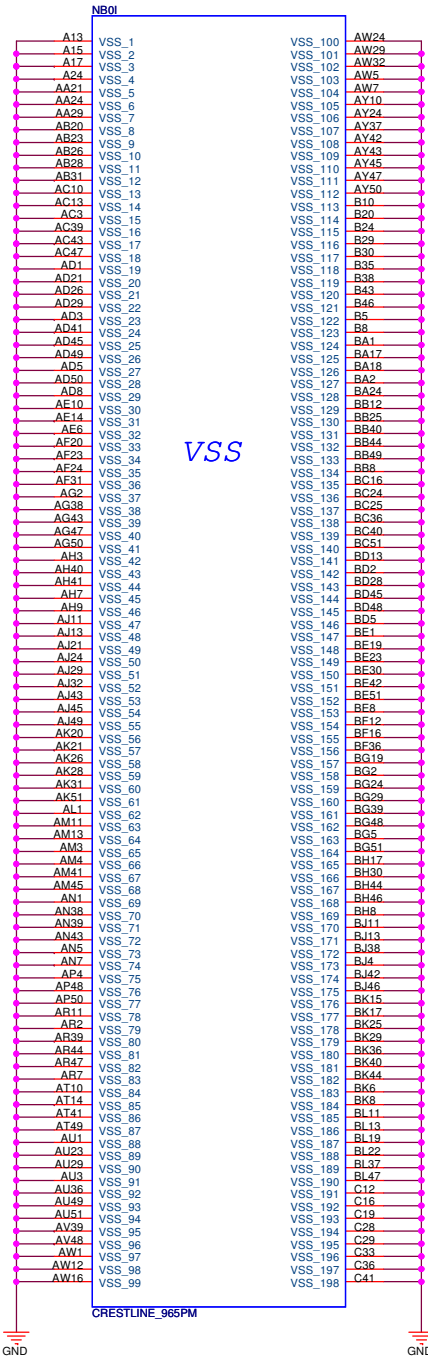
Kennedy Zhang

<Variant Names>

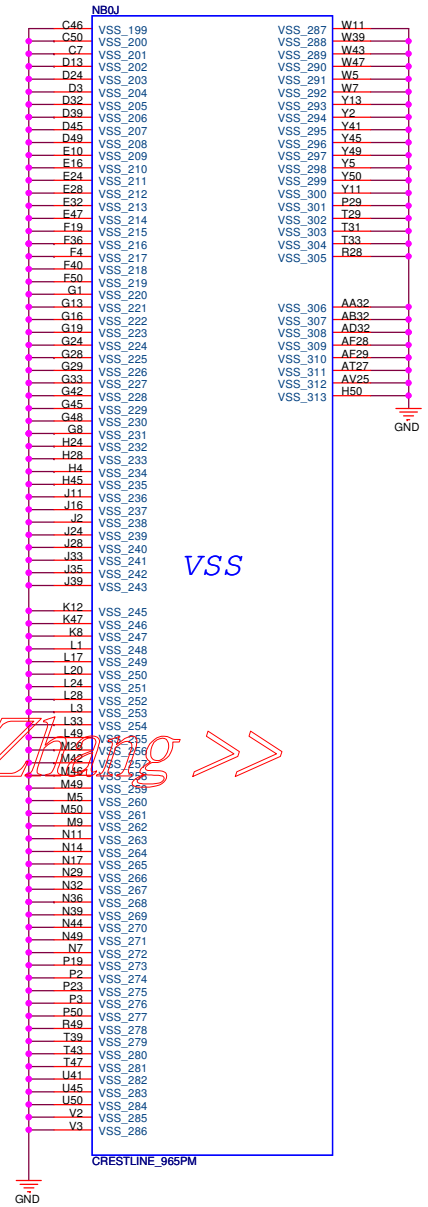
ASUS		Title : CRESTLINE(PWR)	
ASUSTek COMPUTER INC. NB1		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	F7Sr	1.1	
Date: 2007.05.10		Sheet	11 of 95



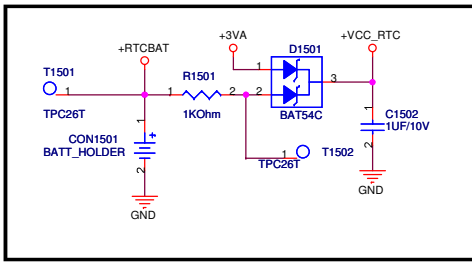
Kennedy Zhang



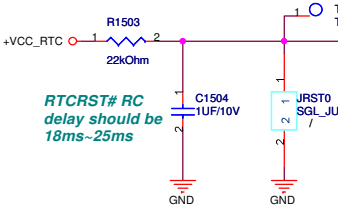
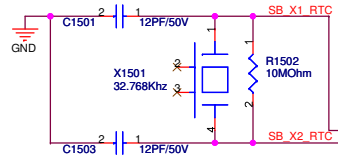
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

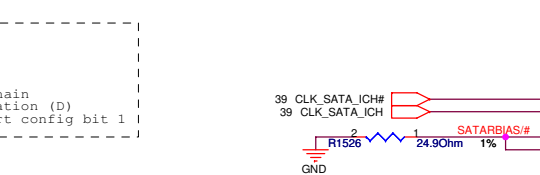
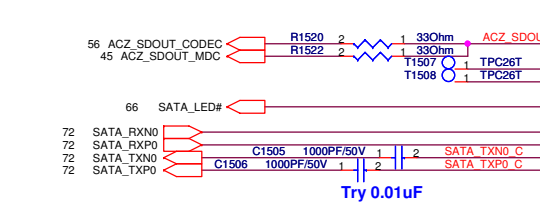
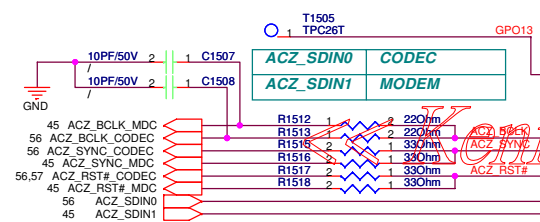


Request of CSC for CMOS clear function
Place Near the Open Door



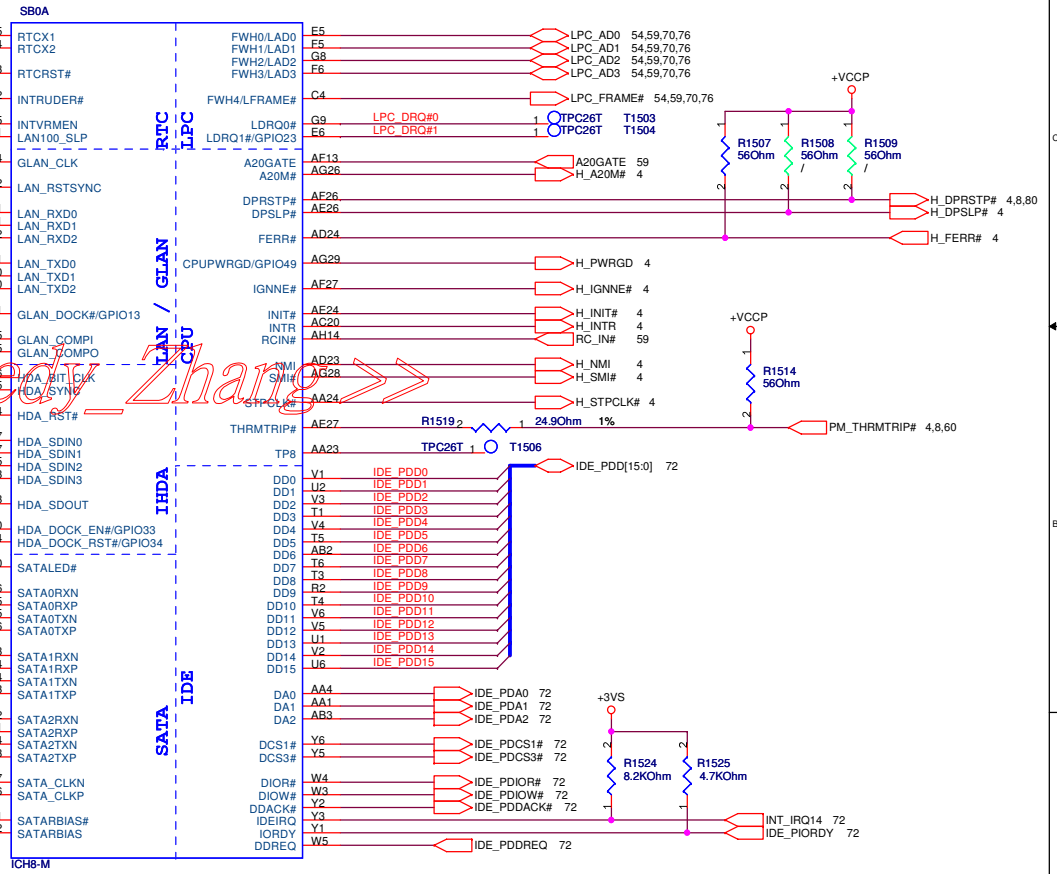
RTCST# RC delay should be 18ms~25ms

ICH_INTVRMEN (VCCSUS1_05, VCCSUS1_5, VCCCL1_5)
Low - Disabled Internal VR
High - Enable Internal VR (D)
ICH_LAN100 (VCCLAN1_05, VCCCL1_05)
Low - Disabled Internal VR
High - Enable Internal VR (D)

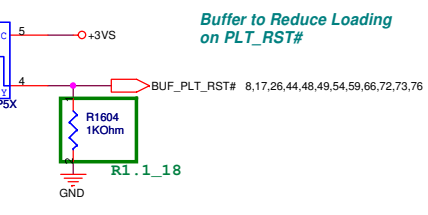
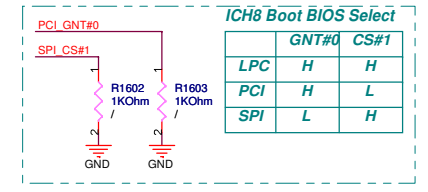
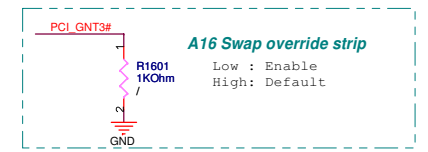
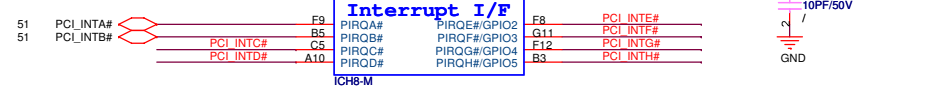
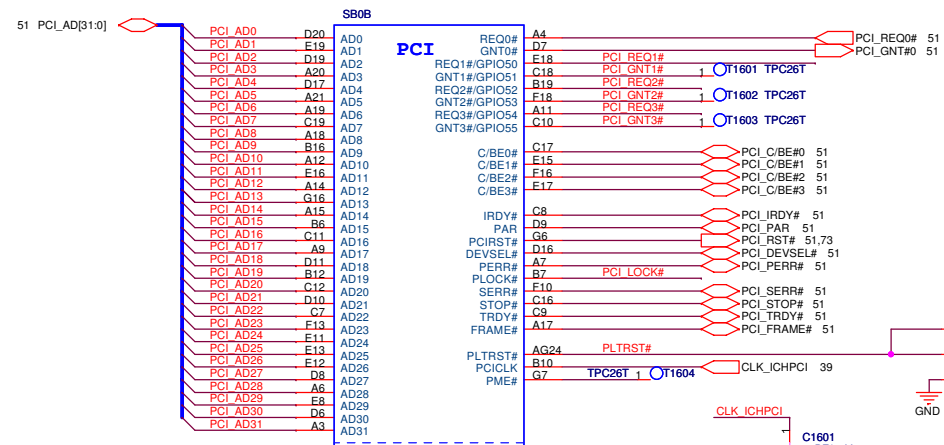


XOR Chain Entrance Strap

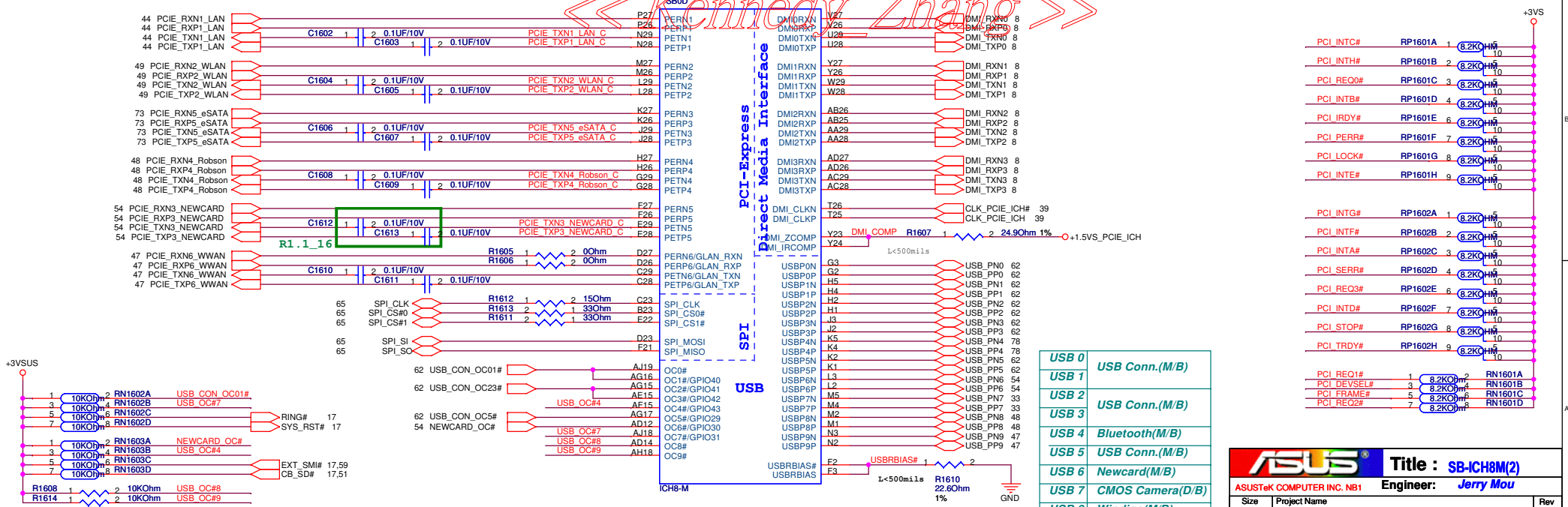
ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (D)
1	1	Set PCIe port config bit 1



Jerry Mou Zhang



« Kennedy Zhang »



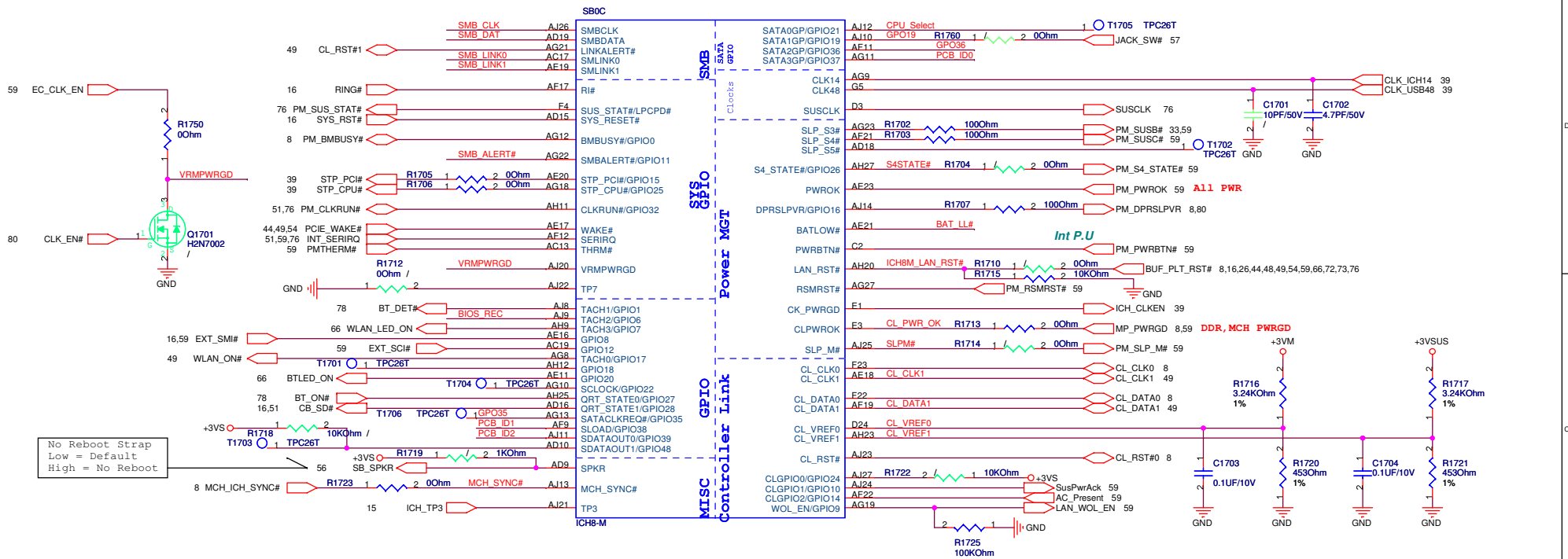
USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	USB Conn.(M/B)
USB 4	Bluetooth(M/B)
USB 5	USB Conn.(M/B)
USB 6	Newcard(M/B)
USB 7	CMOS Camera(D/B)
USB 8	Windigo(M/B)
USB 9	TV(M/B)

ASUS Title : SB-ICH8M(2)

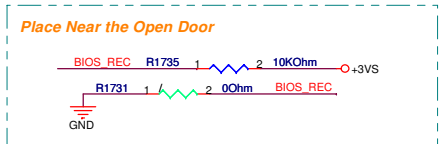
ASUSTeK COMPUTER INC. NBI Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

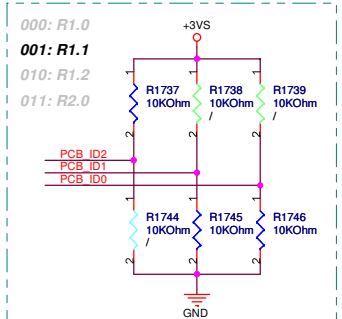
Date: 星期四, 五月 10, 2007 Sheet 16 of 95



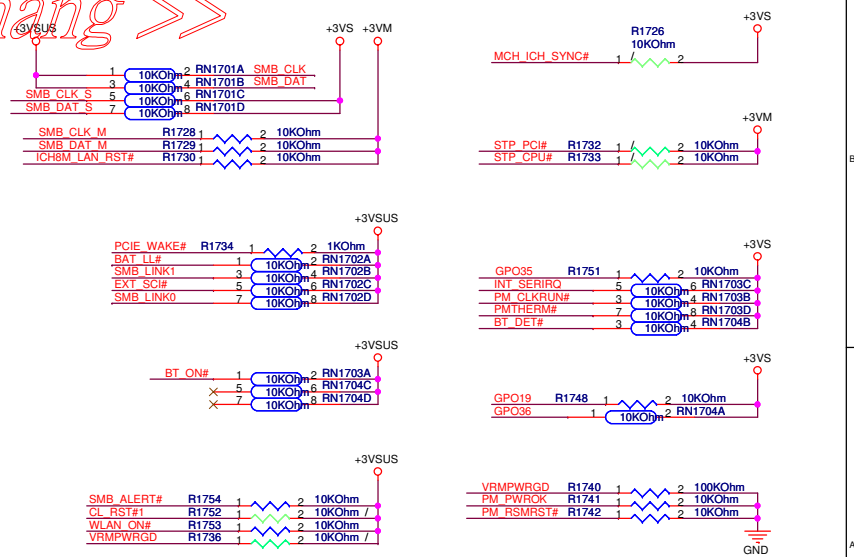
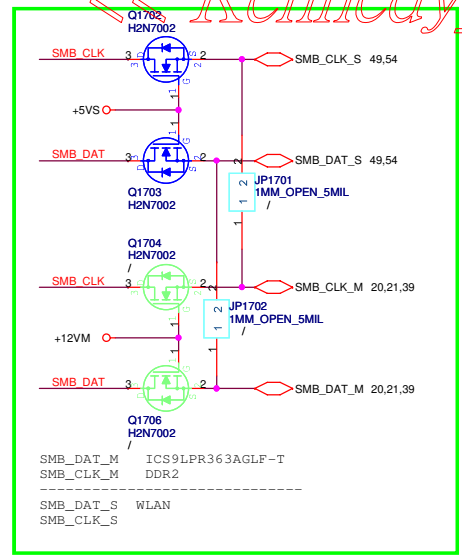
Mount for BIOS Recovery



PCB_ID[0:2]

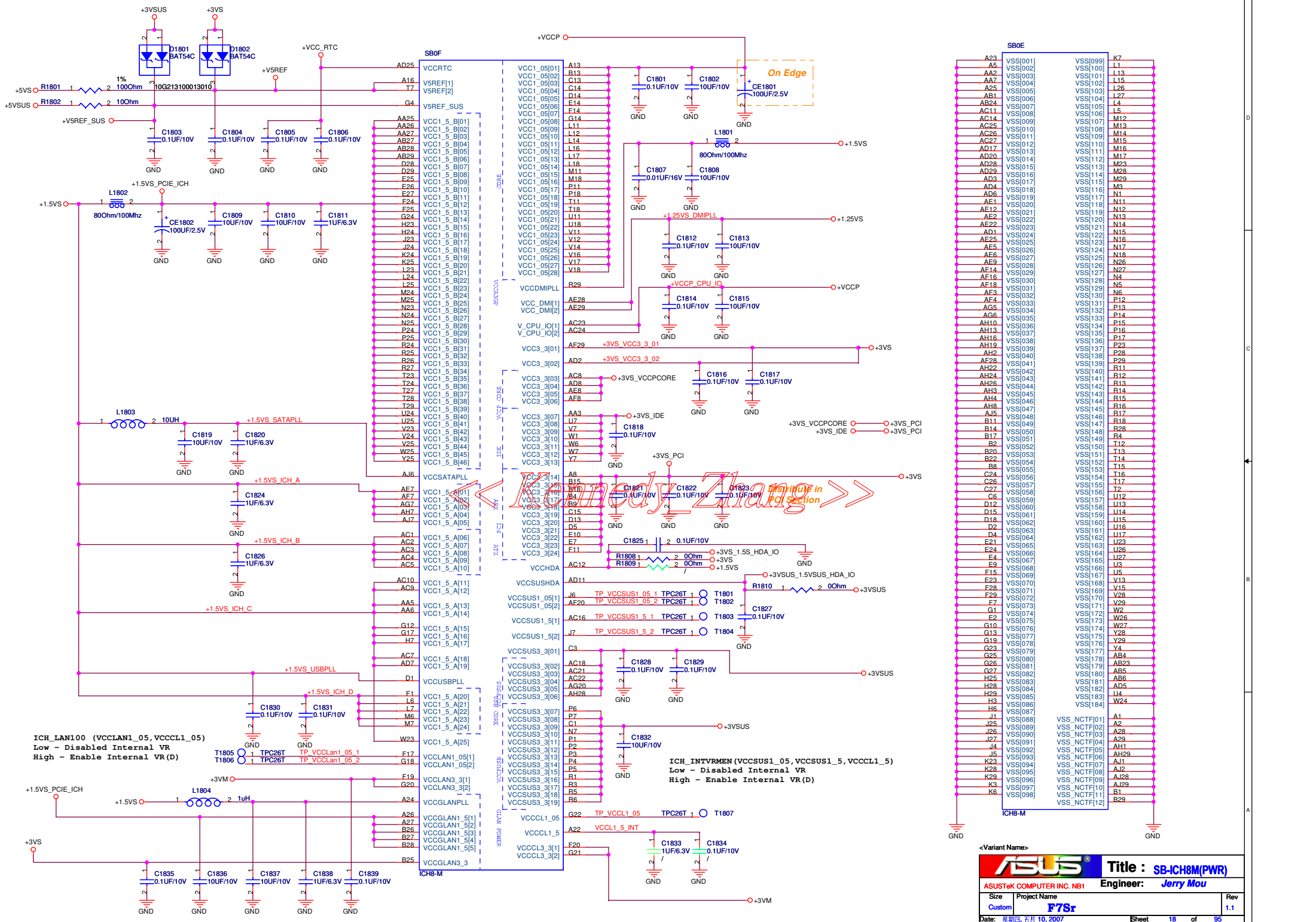


<< Kennedy_Zhang >>



PM_SUSC#	R1708	1	0Ohm	PM_S4_STATE#
PM_SUSB#	R1709	1	0Ohm	PM_SLP_M#
CL_PWR_OK	R1711	1	0Ohm	PM_PWROK
37.59 SMB1_CLK	R1758	1	0Ohm	SMB_LINK0
37.59 SMB1_DAT	R1759	1	0Ohm	SMB_LINK1

ASUS Title : SB-ICH8M(3)
 ASUSTeK COMPUTER INC. NBI Engineer: Jerry Mou
 Size Project Name
 Custom F7Sr
 Date: 2007.05.10 Rev 1.1
 Sheet 17 of 95

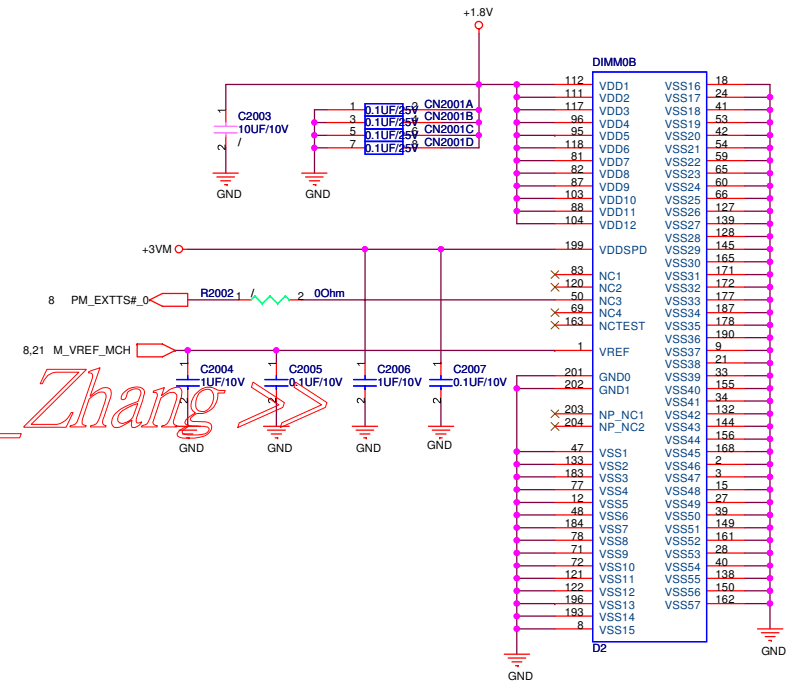
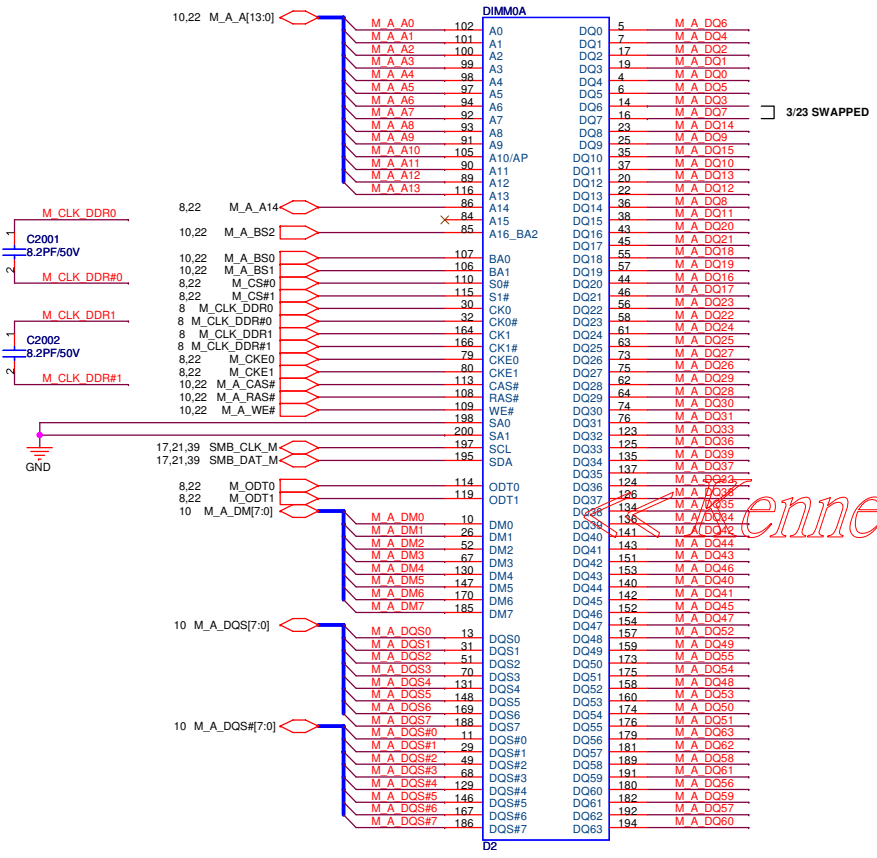


ASUS® Title: SB-ICH8M(PWR)
 ASUSTeK COMPUTER INC. NBI Engineer: Jerry Mou
 Size Project Name
 Custom F7Sr
 Date: 2007.10.10 Sheet 18 of 95

<< Kennedy_Zhang >>

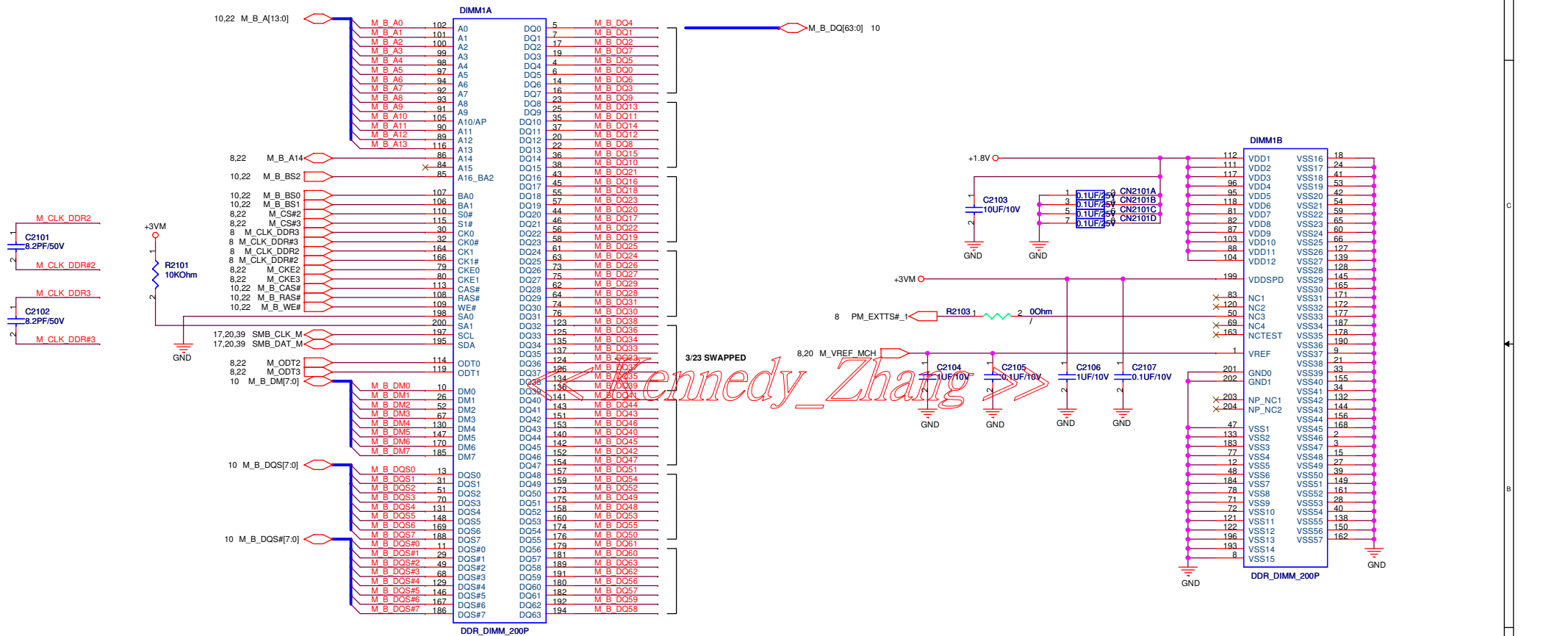
REV Type - 12G025122006
ME - 12G025332003

M_A_DQ[63:0] 10

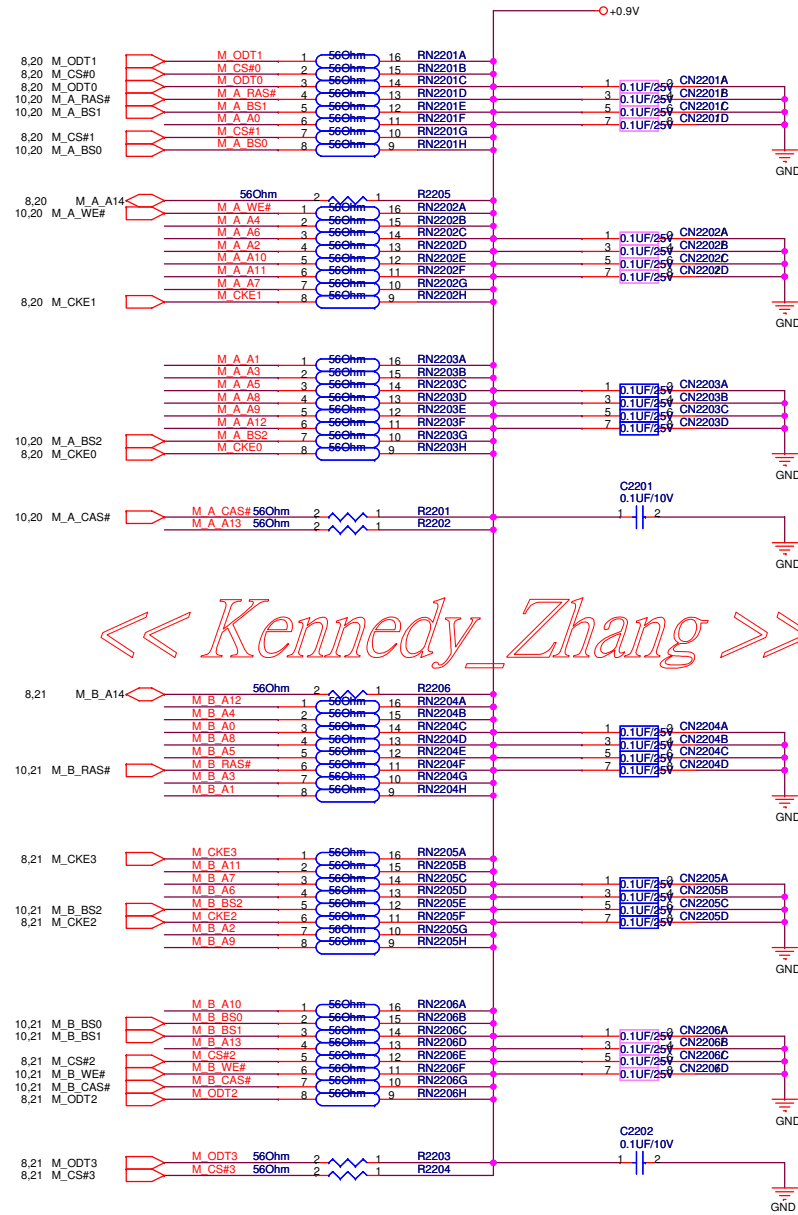


Kennedy_Zhang

STD Type - 12G025122000



10,20 M_A_A[13:0]
10,21 M_B_A[13:0]

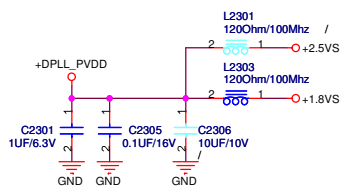


<< Kennedy_Zhang >>

<Variant Name>

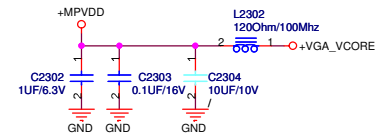
ASUS		Title : DDR2 TERMINATION
ASUSTeK COMPUTER INC. NBI		Engineer: Jerry Mou
Size	Project Name	Rev
Custom	F7Sr	1.1
Date: 2007.05.10	Sheet 22	of 95

M66/M76M Power

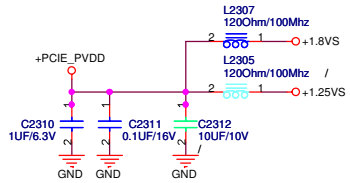


(2.5V @ 170MA DPLL_PVDD) INSTALL DPLL_PVDD TO +2.5V FOR M66M

(1.8V @ 40MA DPLL_PVDD) INSTALL DPLL_PVDD TO +1.8V FOR M76M

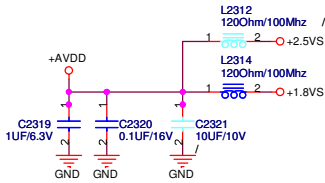


(0.95V-1.1V @ 345MA MPVDD)



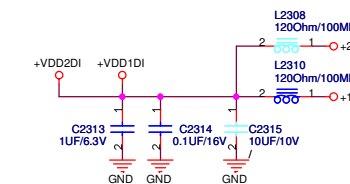
(1.8V @ 40ma PCIE_PVDD) INSTALL PCIE_PVDD TO +1.8V FOR M76M

(1.2V @ 90ma PCIE_PVDD) INSTALL PCIE_PVDD TO +1.2V FOR M66M



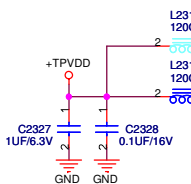
(2.5V @ 100MA AVDD) INSTALL AVDD TO +2.5V FOR M66M

(1.8V @ 100MA AVDD) INSTALL AVDD TO +1.8V FOR M76M



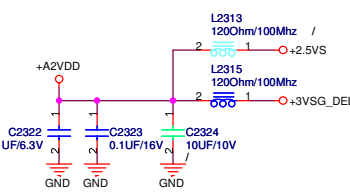
(2.5V @ 110 MA VDD1DI) INSTALL VDD1DI, VDD2DI TO +2.5V FOR M66M

(1.8V @ 100MA VDD1DI) INSTALL VDD1DI, VDD2DI TO +1.8V FOR M76M



(2.5V @ 60MA TPVDD) INSTALL TPVDD TO +2.5V FOR M66M

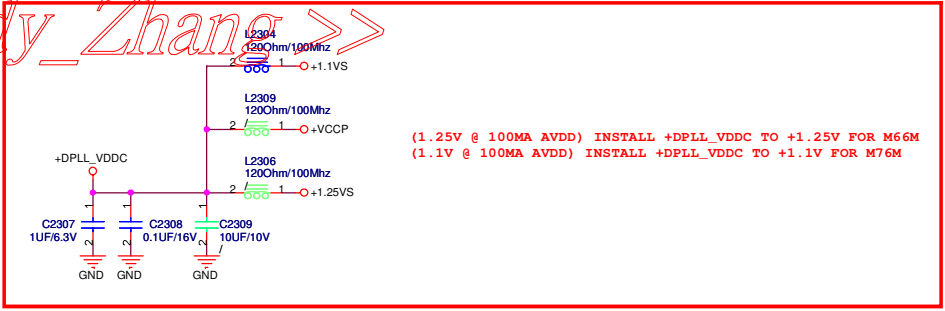
(1.8V @ 20MA TPVDD) INSTALL TPVDD TO +1.8V FOR M76M



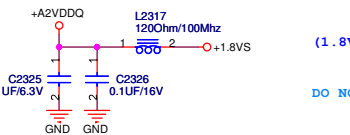
(2.5V @ 120MA A2VDD) INSTALL A2VDD TO +2.5V FOR M66M

(3.3V @ 135MA A2VDD) INSTALL A2VDD TO +3.3V FOR M76M

<< Kennedy_Zhang >>

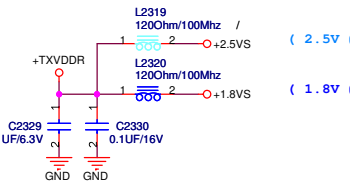


(1.25V @ 100MA AVDD) INSTALL +DPLL_VDDC TO +1.25V FOR M66M
 (1.1V @ 100MA AVDD) INSTALL +DPLL_VDDC TO +1.1V FOR M76M



(1.8V @ 2MA A2VDDQ) INSTALL A2VDDQ TO +1.8V FOR M76M

DO NOT INSTALL A2VDDQ FOR M66M



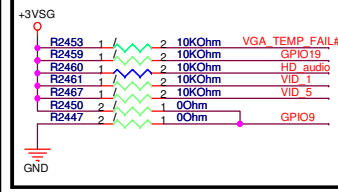
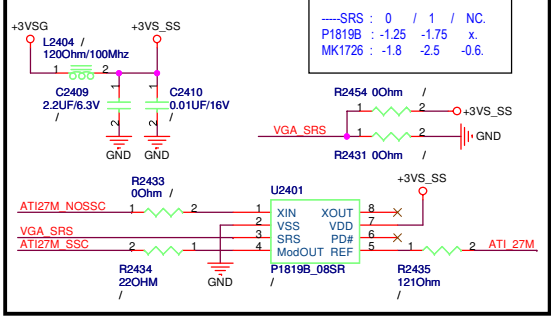
(2.5V @ 155MA TXVDDR) INSTALL TXVDDR TO +2.5V FOR M66M

(1.8V @ 200ma TXVDDR) INSTALL TXVDDR TO +1.8V FOR M76M

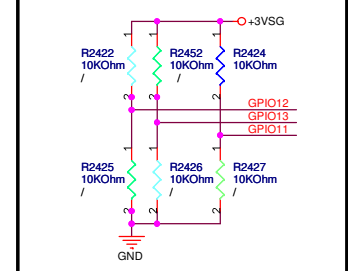
<Variant Name>

ASUS		Title : VGA M72M POWER	
ASUS TeK COMPUTER INC		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	F7Sr	1.1	
Date: 星期五, 五月 10, 2007		Sheet	23 of 95

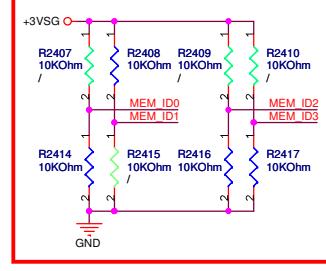
Spread Spectrum



ROM Strap



Memory ID



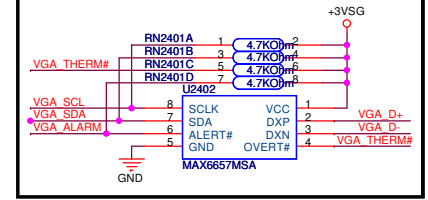
Infinion (DDR2 16M*16 for A Channel 1.8V 128M)
MEM ID[0:3] = 0100

Hynix (DDR2 16M*16 for A Channel 1.8V 128M)
MEM ID[0:3] = 1100

Primary Memory Aperture size requested at PCI Configuration

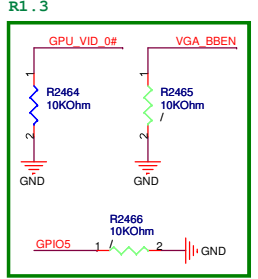
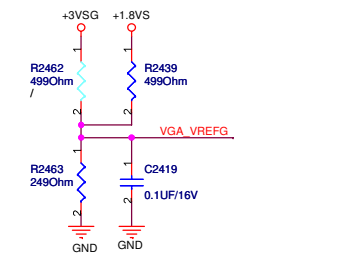
GPIO_13	GPIO_12	GPIO_11
1GB	1	0
512MB	1	0
256MB	0	1
128MB	0	0
64MB	0	1
32MB	0	1

Thermal

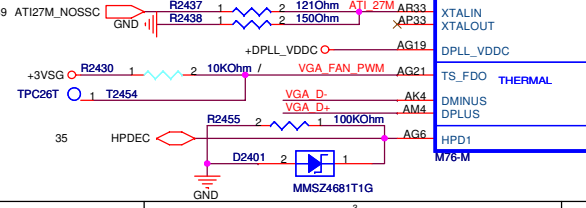


FOR M76M
VREFG VOLTAGE DIVIDER IS VREFG = VDDR4,5 = 1.8V / 3 = 0.6V
R2463=249ohm

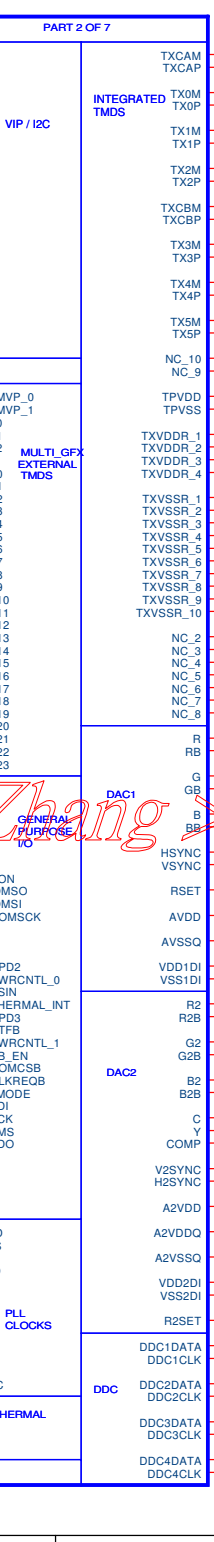
FOR M66M
VREFG VOLTAGE DIVIDER IS VREFG = 3.3V / 2 = 1.65V
R2463=499ohm



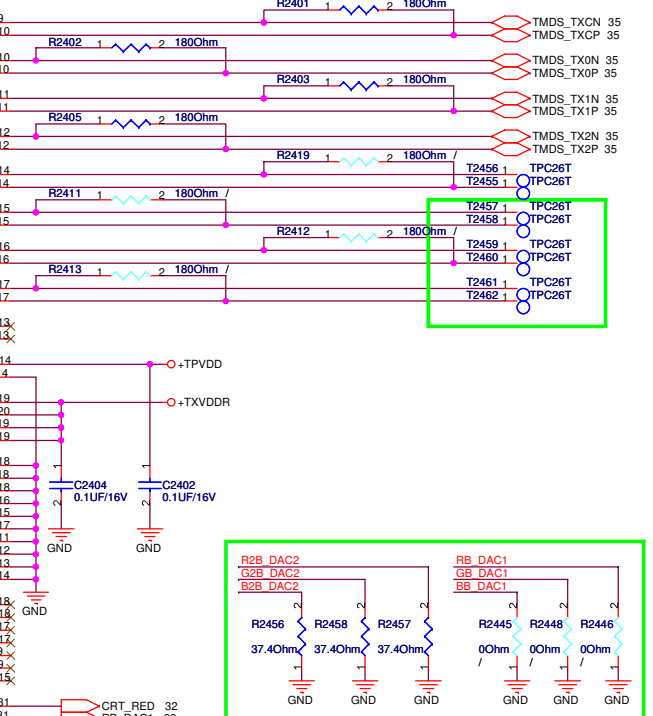
XTALIN VOLTAGE LEVEL
1.2V FOR M66M (R2438 = 71.5ohm)
1.8V FOR M76M (R2438 = 150ohm)



VGA0B



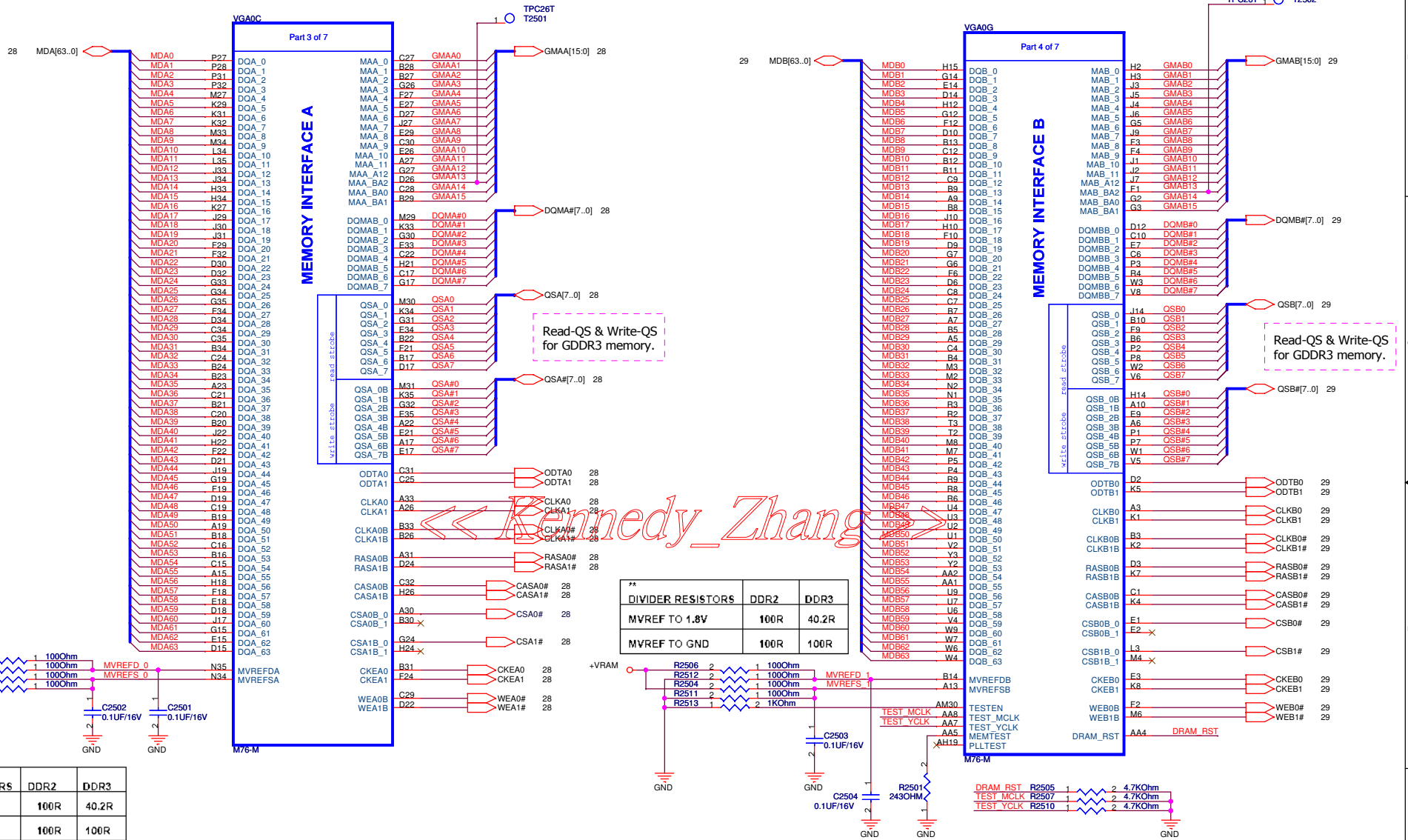
INSTALL TERMINATION RESISTORS CLOSE TO ASIC



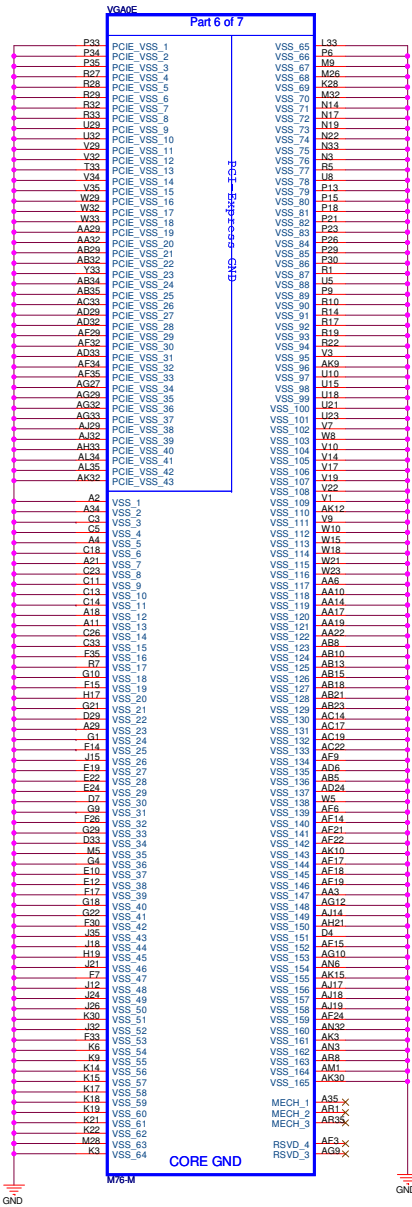
M72 - Close to GPU
M76 - All mount 0 ohm

HDMI_EN

CHANGE BOM P/N TO M72

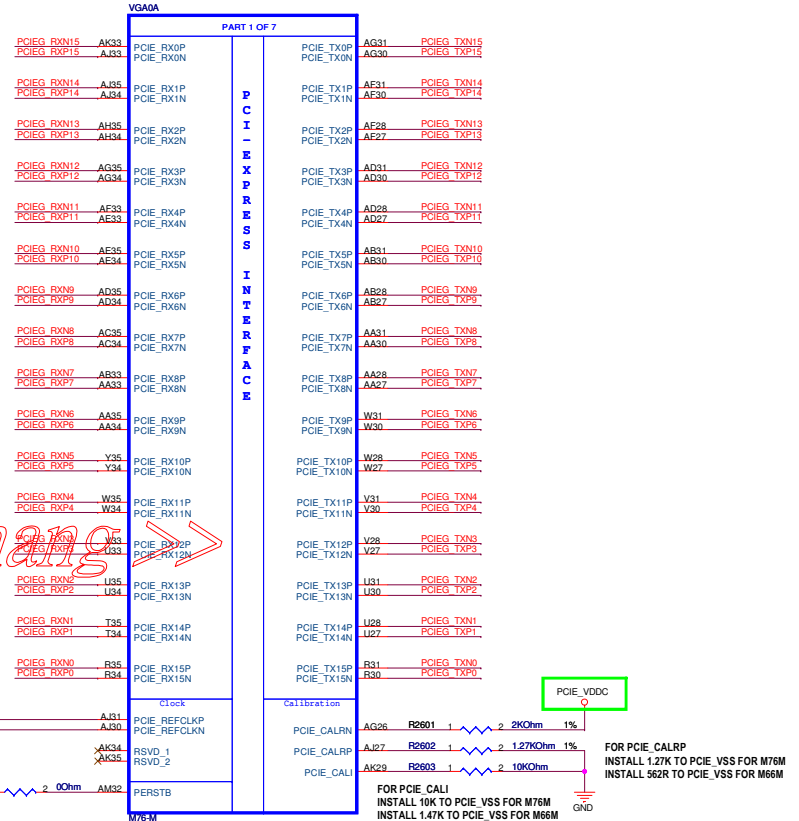


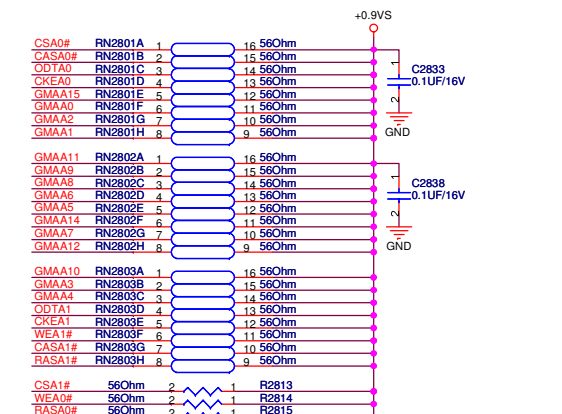
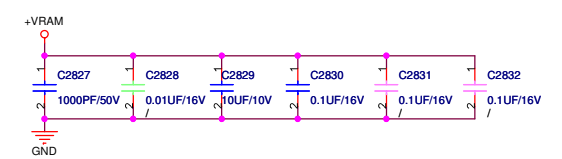
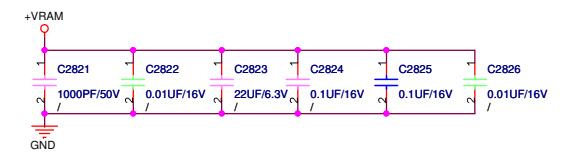
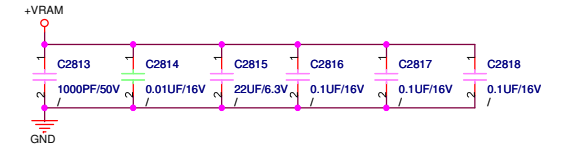
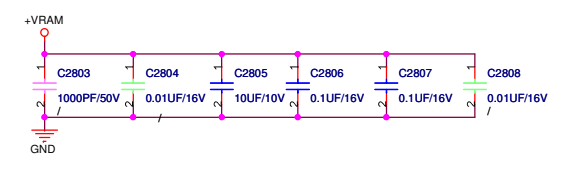
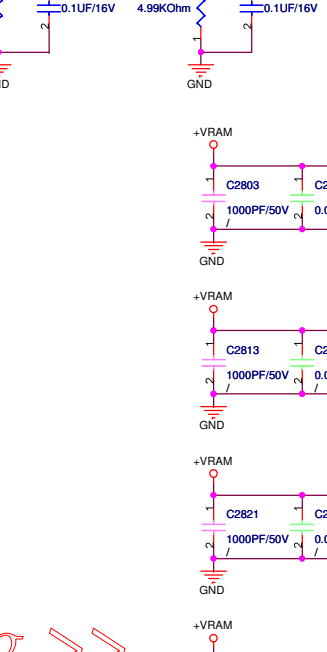
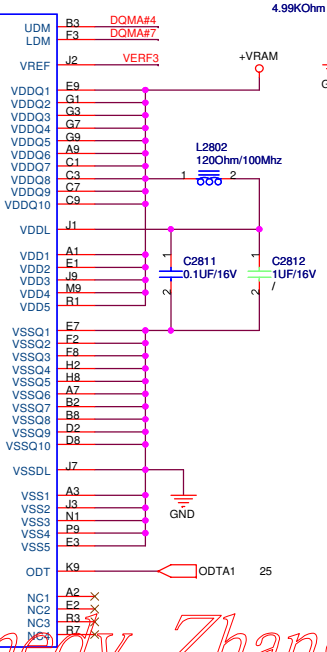
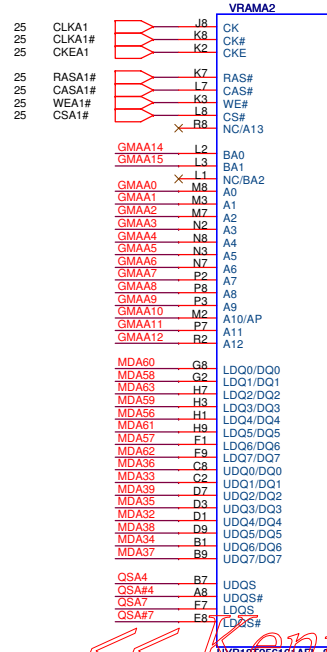
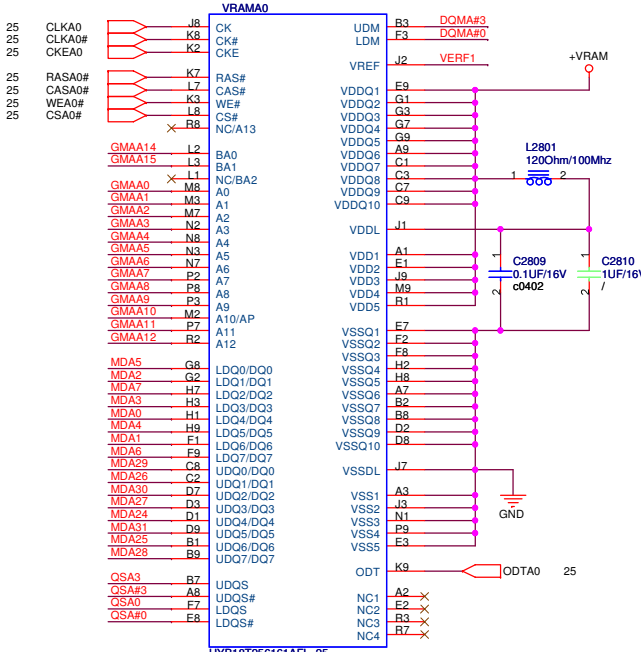
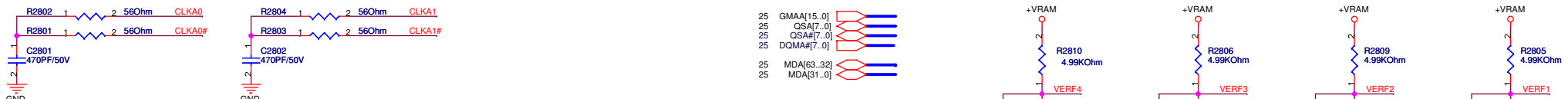
Kennedy_Zhang



PCIEB_RXN15	C2601	1	2	0.1uF/16V	PCIEG_TXN15
PCIEB_RXP15	C2602	1	2	0.1uF/16V	PCIEG_TXP15
PCIEB_RXN14	C2603	1	2	0.1uF/16V	PCIEG_TXN14
PCIEB_RXP14	C2604	1	2	0.1uF/16V	PCIEG_TXP14
PCIEB_RXN13	C2605	1	2	0.1uF/16V	PCIEG_TXN13
PCIEB_RXP13	C2606	1	2	0.1uF/16V	PCIEG_TXP13
PCIEB_RXN12	C2607	1	2	0.1uF/16V	PCIEG_TXN12
PCIEB_RXP12	C2608	1	2	0.1uF/16V	PCIEG_TXP12
PCIEB_RXN11	C2609	1	2	0.1uF/16V	PCIEG_TXN11
PCIEB_RXP11	C2610	1	2	0.1uF/16V	PCIEG_TXP11
PCIEB_RXN10	C2611	1	2	0.1uF/16V	PCIEG_TXN10
PCIEB_RXP10	C2612	1	2	0.1uF/16V	PCIEG_TXP10
PCIEB_RXN9	C2613	1	2	0.1uF/16V	PCIEG_TXN9
PCIEB_RXP9	C2614	1	2	0.1uF/16V	PCIEG_TXP9
PCIEB_RXN8	C2615	1	2	0.1uF/16V	PCIEG_TXN8
PCIEB_RXP8	C2616	1	2	0.1uF/16V	PCIEG_TXP8
PCIEB_RXN7	C2617	1	2	0.1uF/16V	PCIEG_TXN7
PCIEB_RXP7	C2618	1	2	0.1uF/16V	PCIEG_TXP7
PCIEB_RXN6	C2619	1	2	0.1uF/16V	PCIEG_TXN6
PCIEB_RXP6	C2620	1	2	0.1uF/16V	PCIEG_TXP6
PCIEB_RXN5	C2621	1	2	0.1uF/16V	PCIEG_TXN5
PCIEB_RXP5	C2622	1	2	0.1uF/16V	PCIEG_TXP5
PCIEB_RXN4	C2623	1	2	0.1uF/16V	PCIEG_TXN4
PCIEB_RXP4	C2624	1	2	0.1uF/16V	PCIEG_TXP4
PCIEB_RXN3	C2625	1	2	0.1uF/16V	PCIEG_TXN3
PCIEB_RXP3	C2626	1	2	0.1uF/16V	PCIEG_TXP3
PCIEB_RXN2	C2627	1	2	0.1uF/16V	PCIEG_TXN2
PCIEB_RXP2	C2628	1	2	0.1uF/16V	PCIEG_TXP2
PCIEB_RXN1	C2629	1	2	0.1uF/16V	PCIEG_TXN1
PCIEB_RXP1	C2630	1	2	0.1uF/16V	PCIEG_TXP1
PCIEB_RXN0	C2631	1	2	0.1uF/16V	PCIEG_TXN0
PCIEB_RXP0	C2632	1	2	0.1uF/16V	PCIEG_TXP0

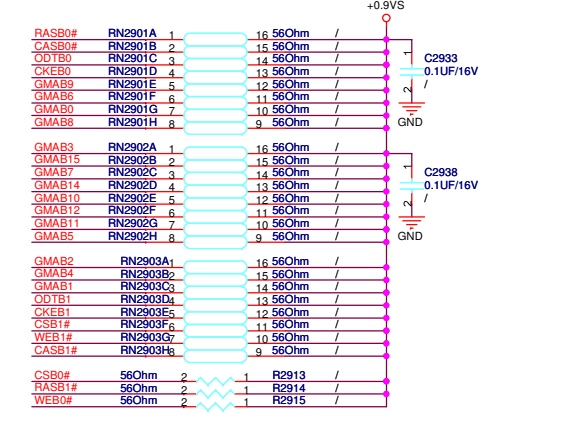
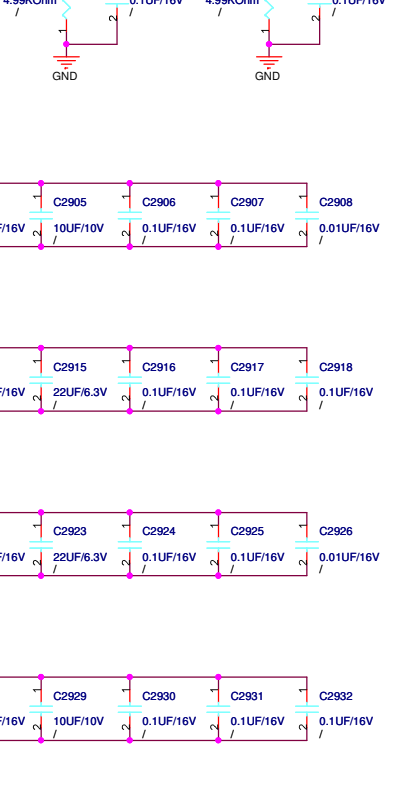
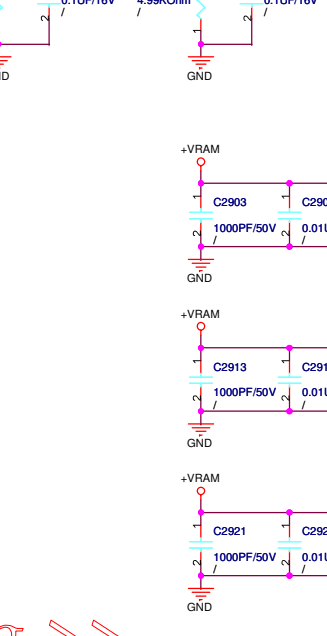
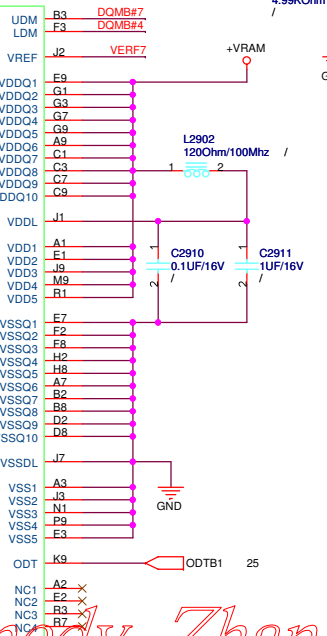
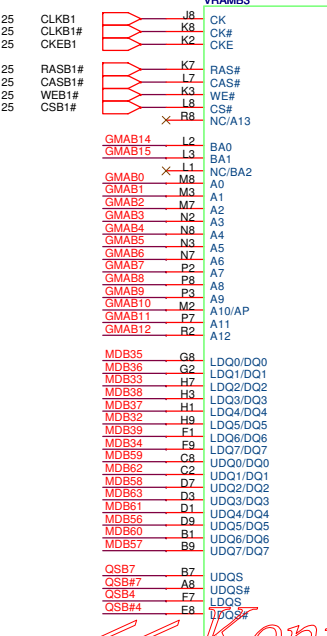
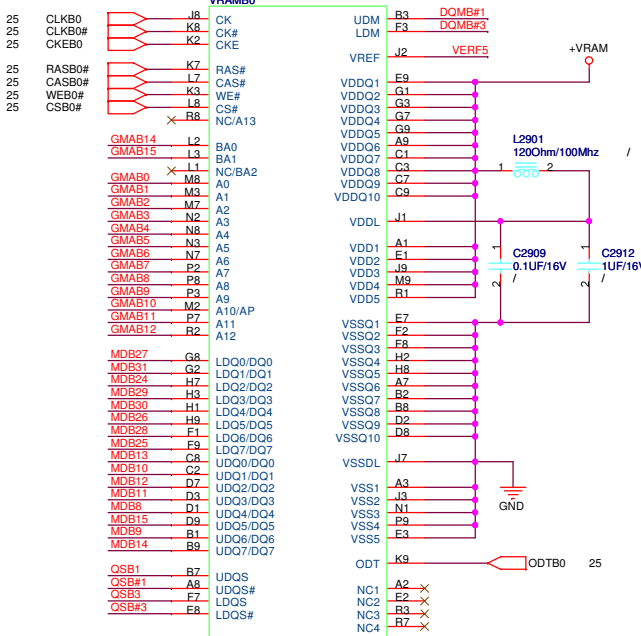
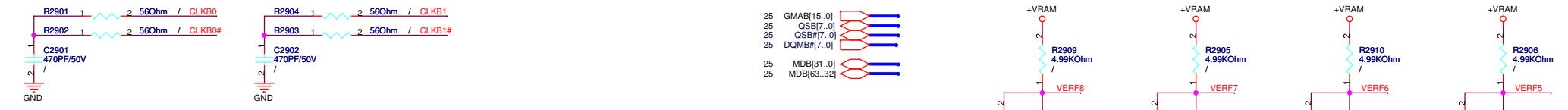
<< Kennedy_Zhang >>



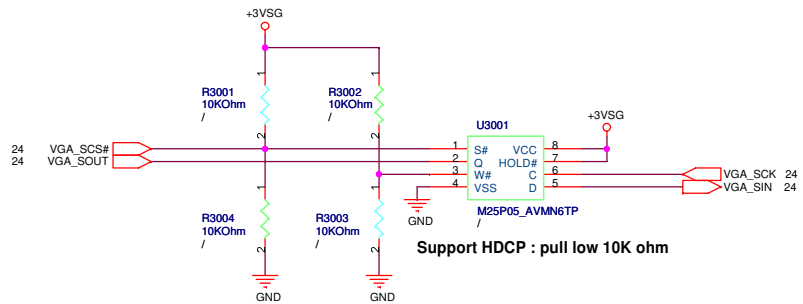


<< Kennedy_Zhang >>

ASUS		Title : AT1_M7X/66-M_VRAM_A	
ASUSTek COMPUTER INC		Engineer: Jerry Mou	
Size	Project Name		Rev
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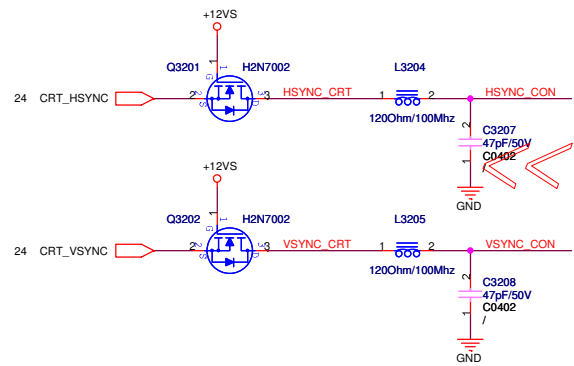
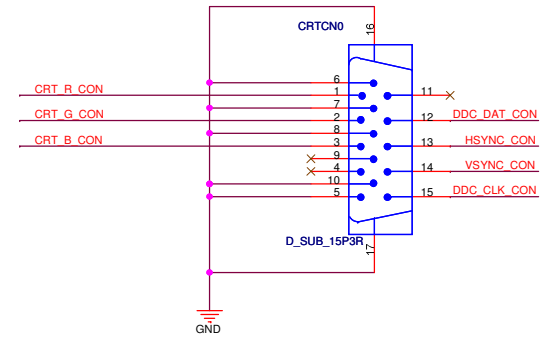
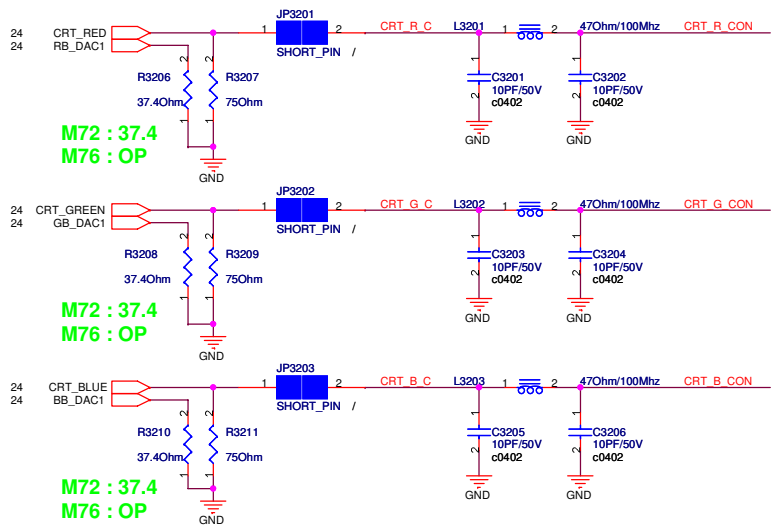


<< Kennedy_Zhang >>



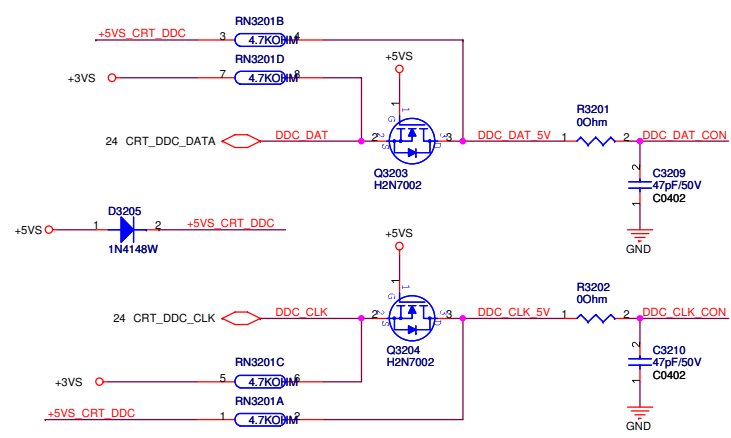
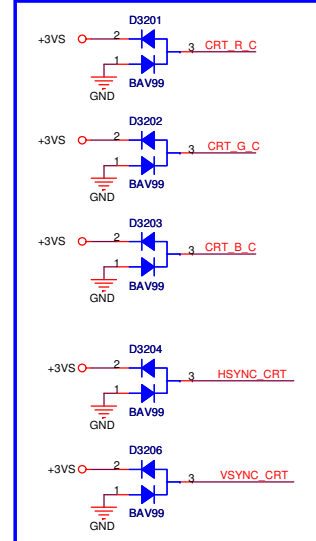
<< Kennedy_Zhang >>

<< Kennedy_Zhang >>



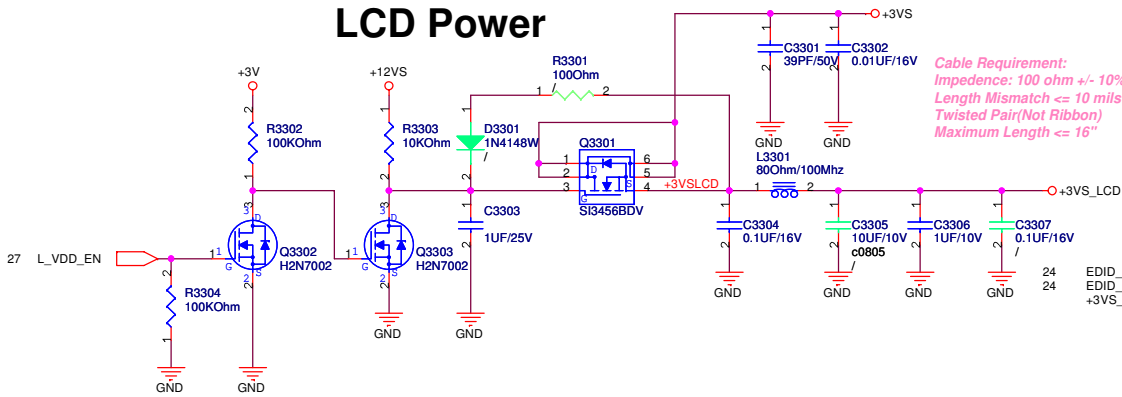
<< Kennedy_Zhang >>

PLACE ESD Diodes near VGA port



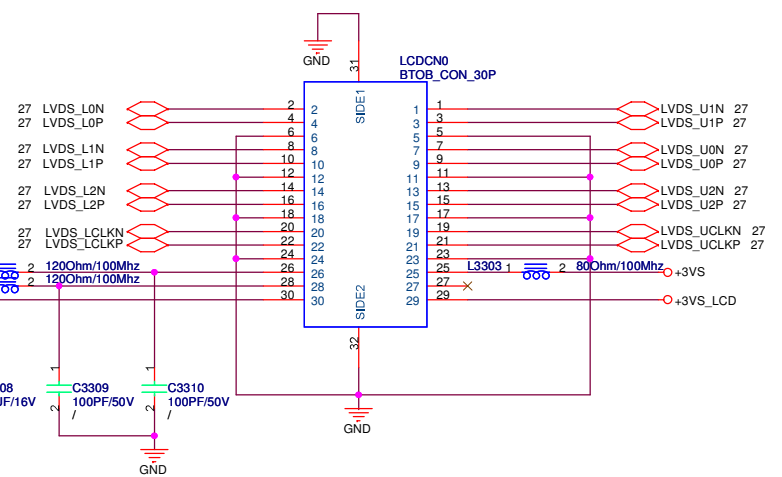
LCD Backlight Control

LCD Power

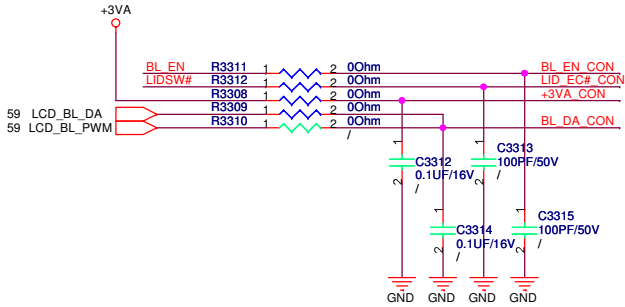


Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

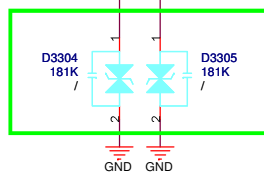
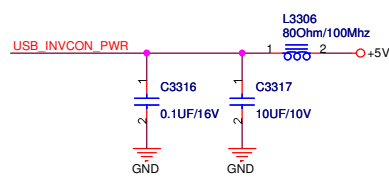
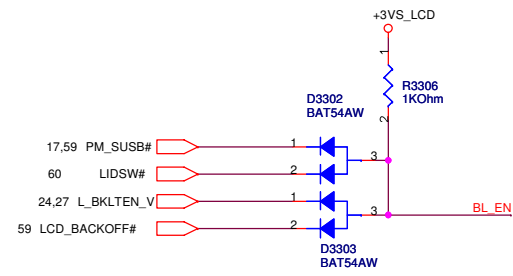
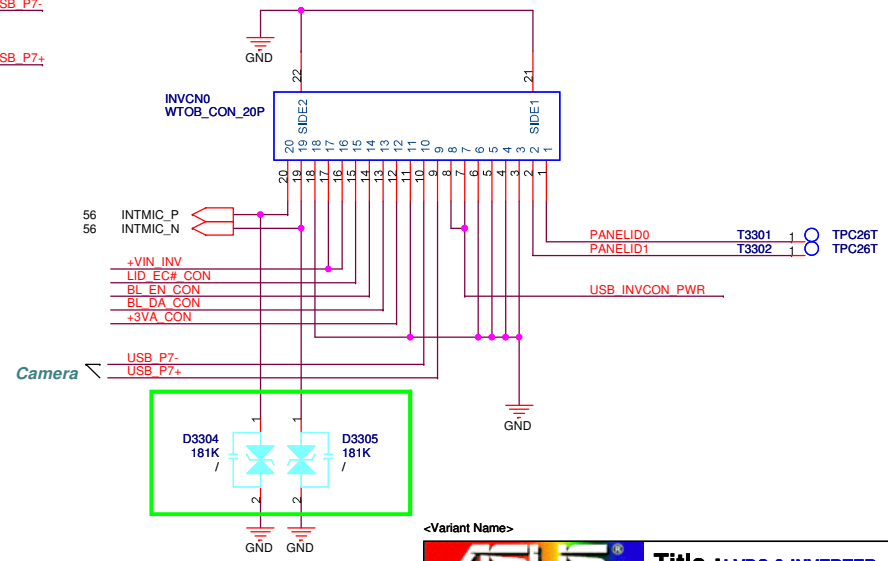
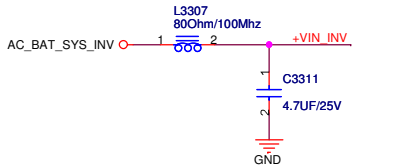
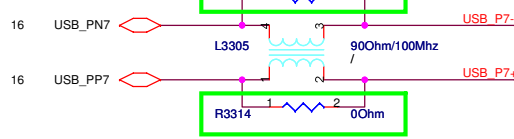
LCD LVDS Interface



INVERTER Interface/Speaker CONN.



<< Kennedy_Zhang >>

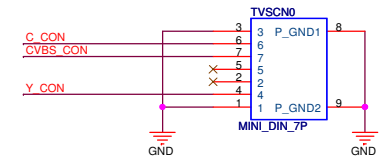
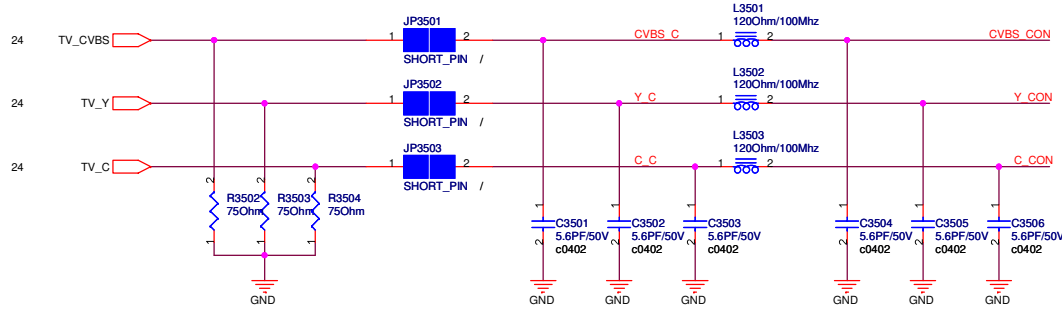
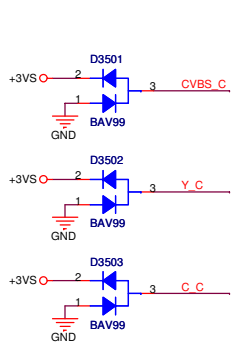


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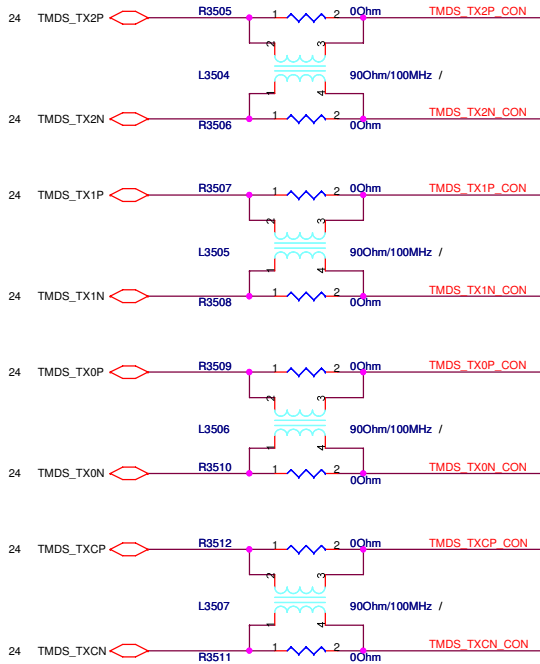
ASUS		Title :LVDS & INVERTER	
ASUSTeK COMPUTER INC		Engineer: Jerry Mou	
Size	Project Name	Rev	1.1
Custom	F7Sr	Date:	星期四, 五月 10, 2007
Date: 星期四, 五月 10, 2007		Sheet	33 of 95

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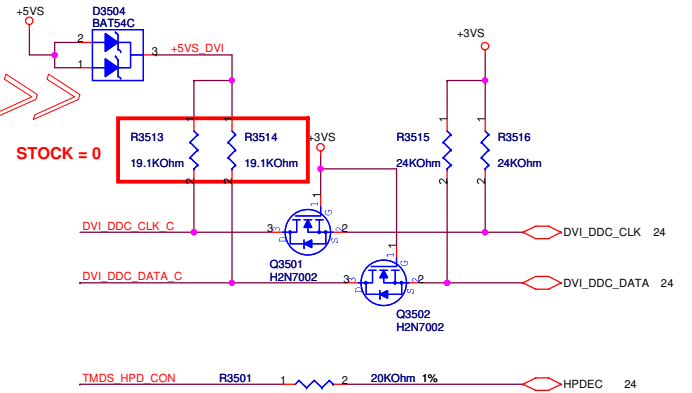
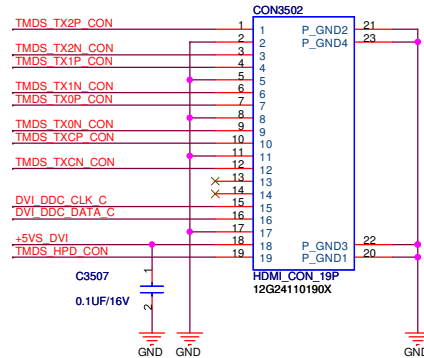
TV OUT



HDMI

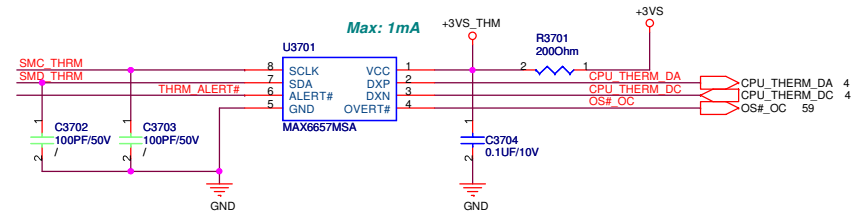
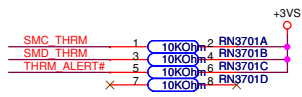
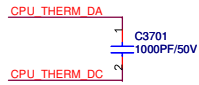
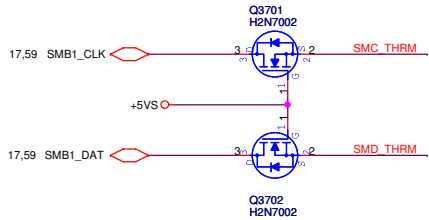


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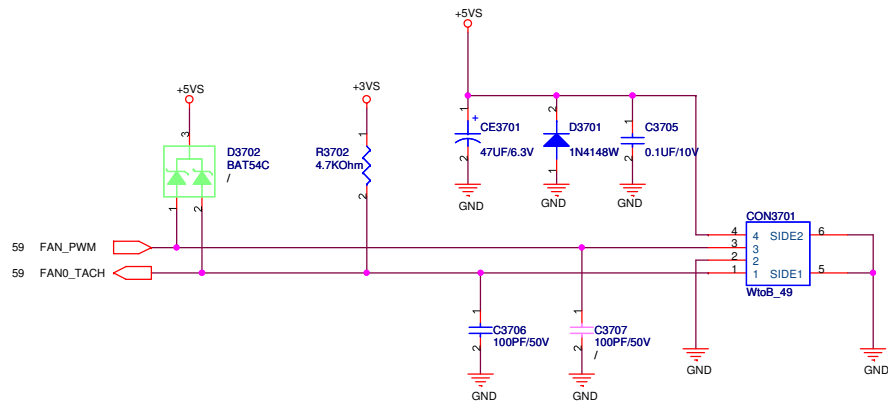
<< Kennedy_Zhang >>

Thermal Sensor

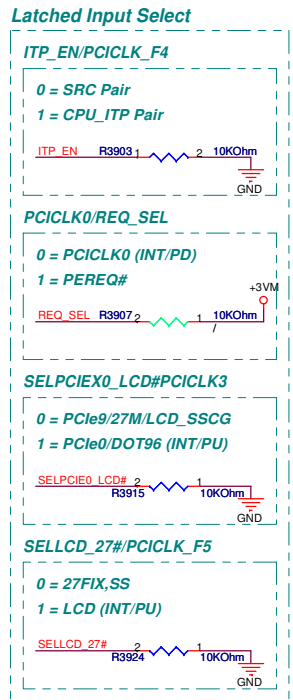
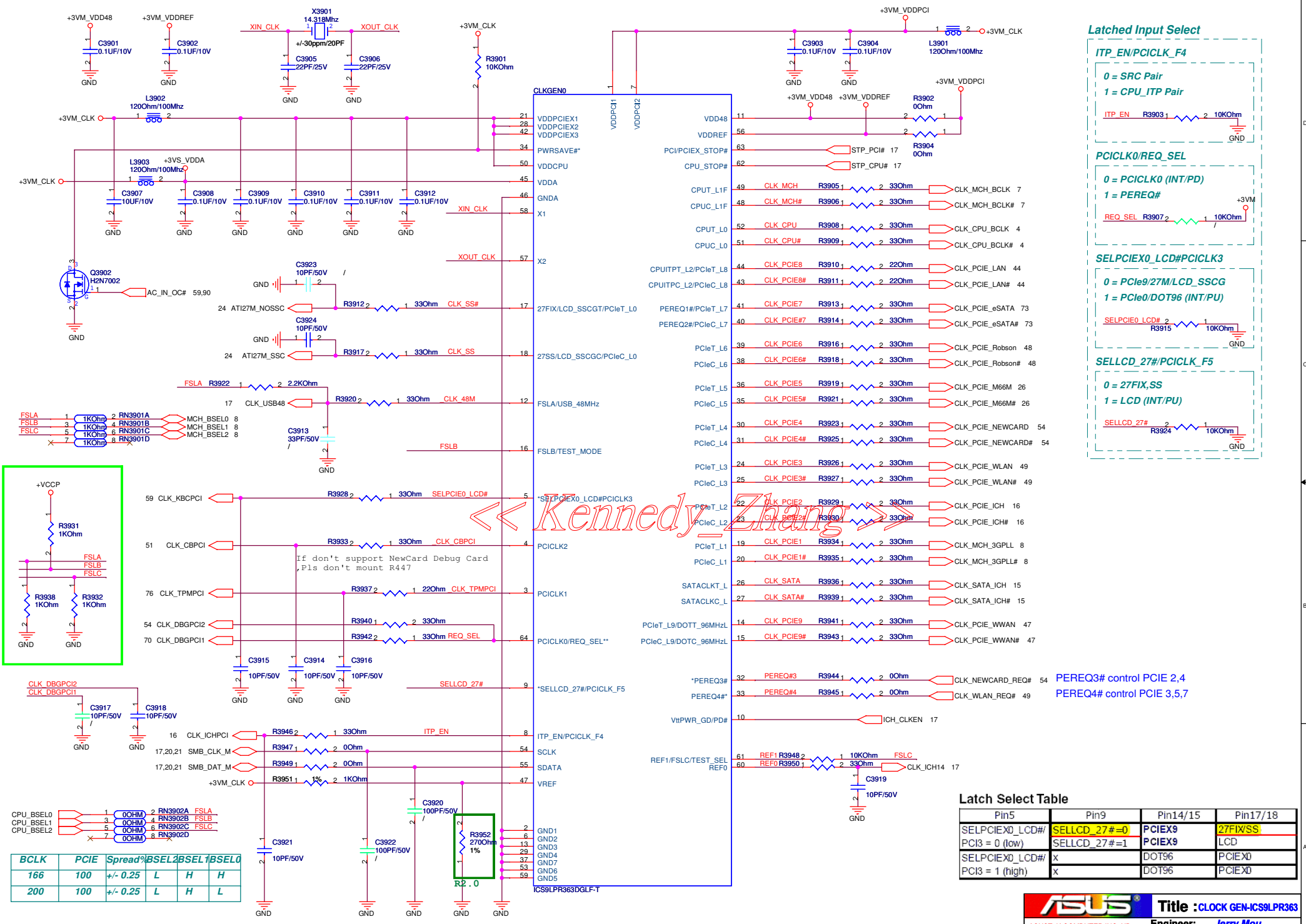


DC FAN Control

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



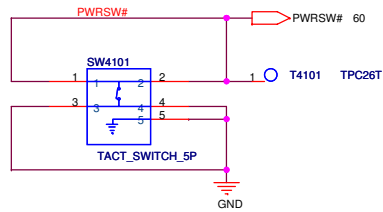
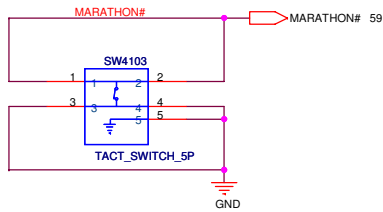
BCLK	PCIE	Spread%	%BSEL2	%BSEL1	%BSEL0
166	100	+/- 0.25	L	H	H
200	100	+/- 0.25	L	H	L

PEREQ3# control PCIE 2,4
PEREQ4# control PCIE 3,5,7

Latch Select Table

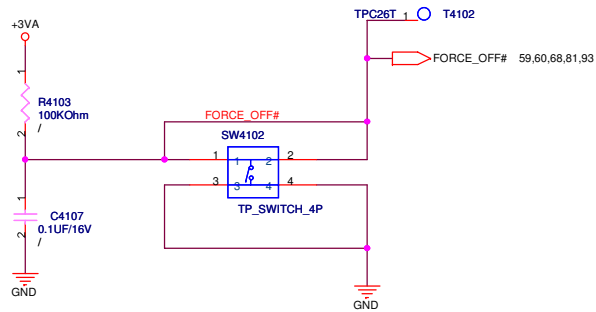
Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD#	SELLCD_27# = 0	PCIEX9	27FX/SS
PCIE3 = 0 (low)	SELLCD_27# = 1	PCIEX9	LCD
SELPCIEX0_LCD#	X	DOT96	PCIEX0
PCIE3 = 1 (high)	X	DOT96	PCIEX0

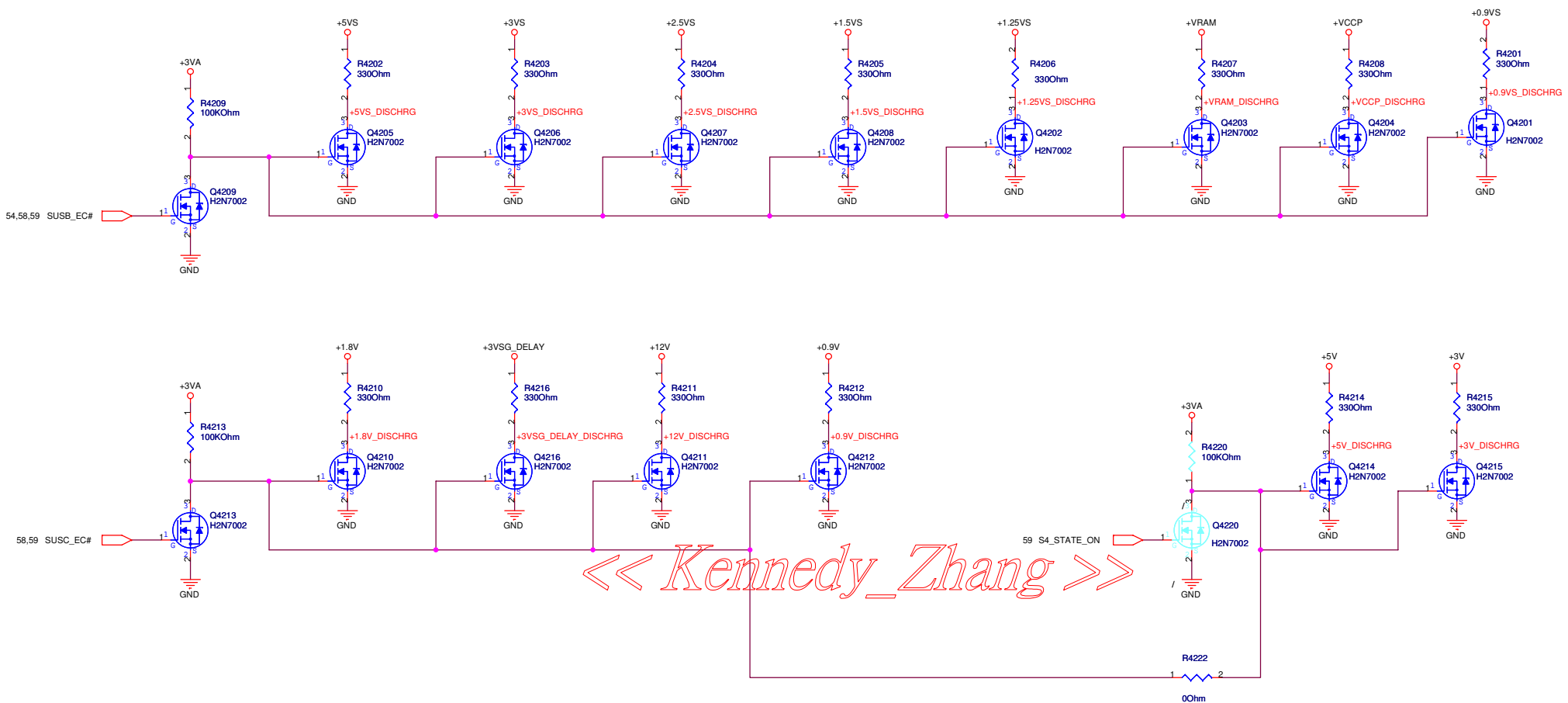
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

SHUT_DOWN#





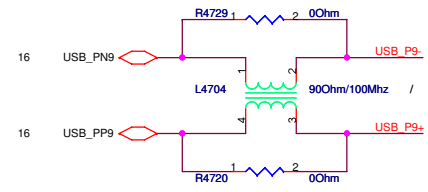
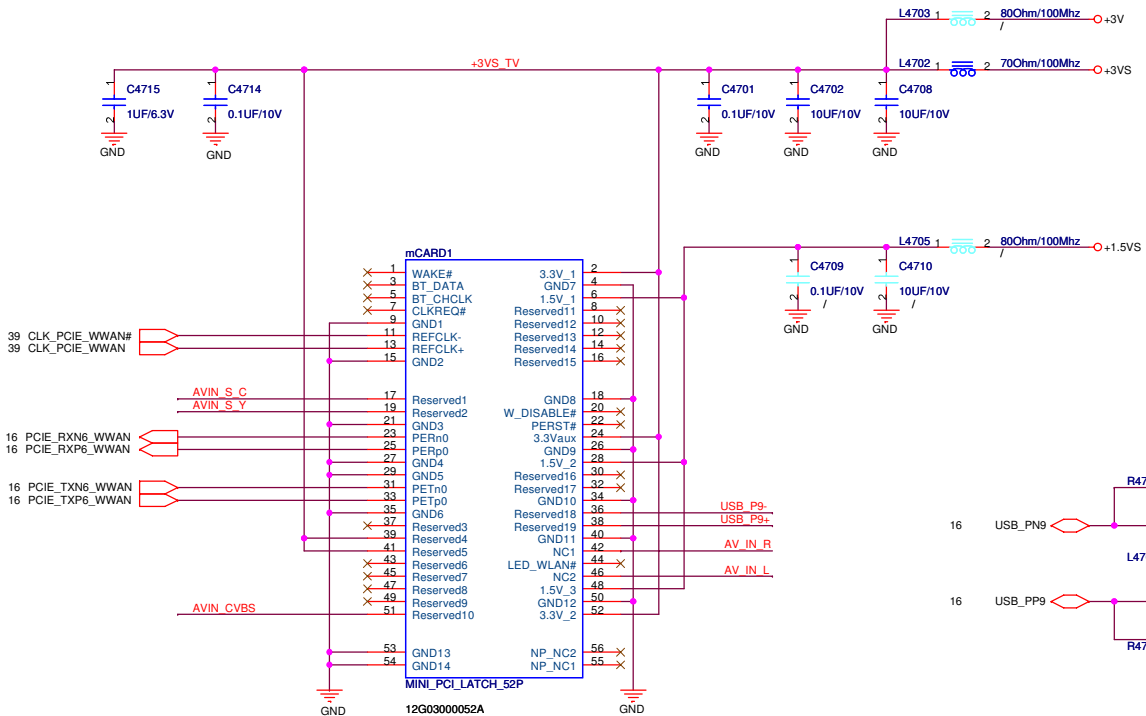
<< Kennedy_Zhang >>

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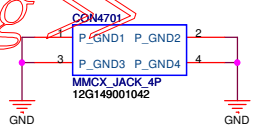
ASUS		Title : DISCHARGE & EMI CAP
ASUSTeK COMPUTER INC. NB1		Engineer: Jerry Mou
Size Custom	Project Name F7Sr	Rev 1.1
Date: 星期五, 五月 10, 2007	Sheet 42	of 95

<< Kennedy_Zhang >>

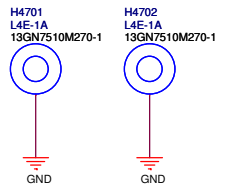
<< Kennedy_Zhang >>



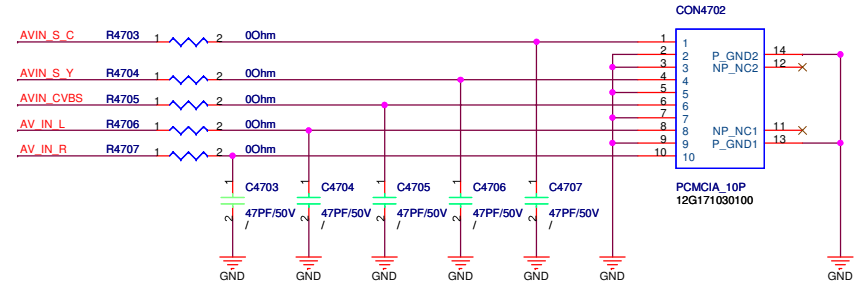
H = 5.2mm *<< Kennedy_Zhang >>* **TV Conn.**
FOR TV TUNER
(UWB OPTION)

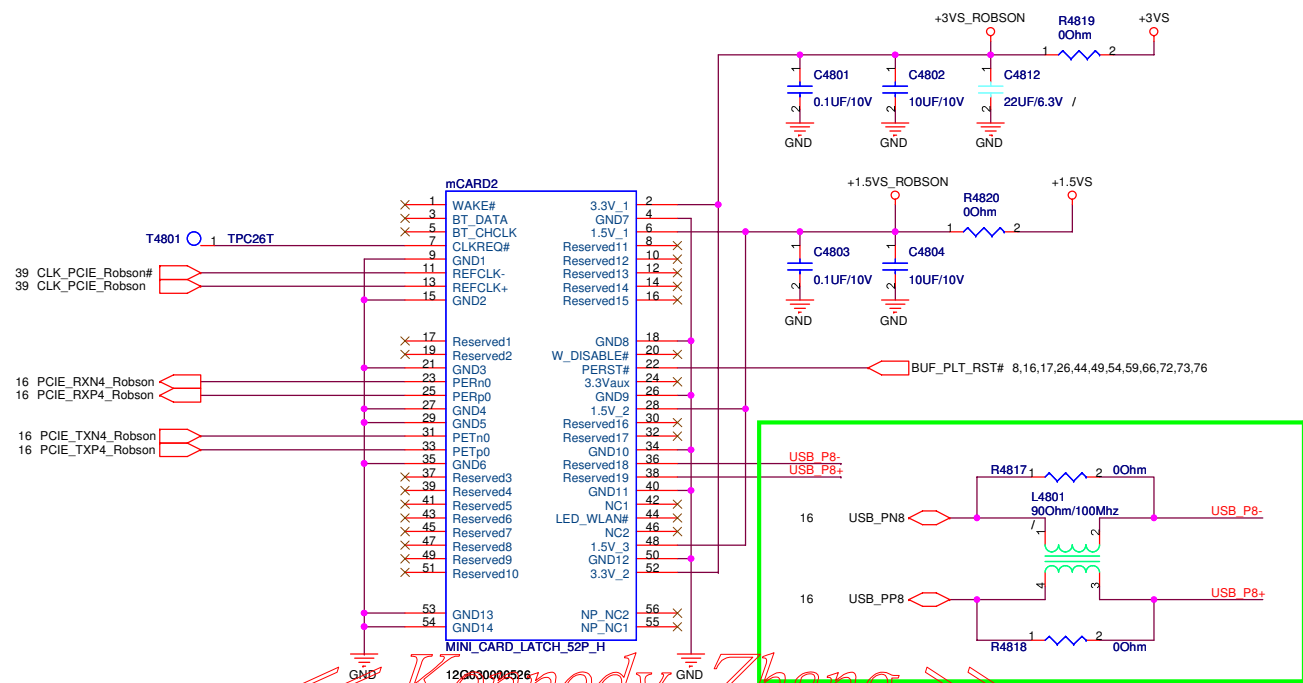


ME P/N : 14G152075000



H = 3.0mm

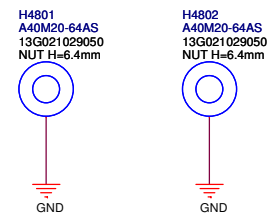


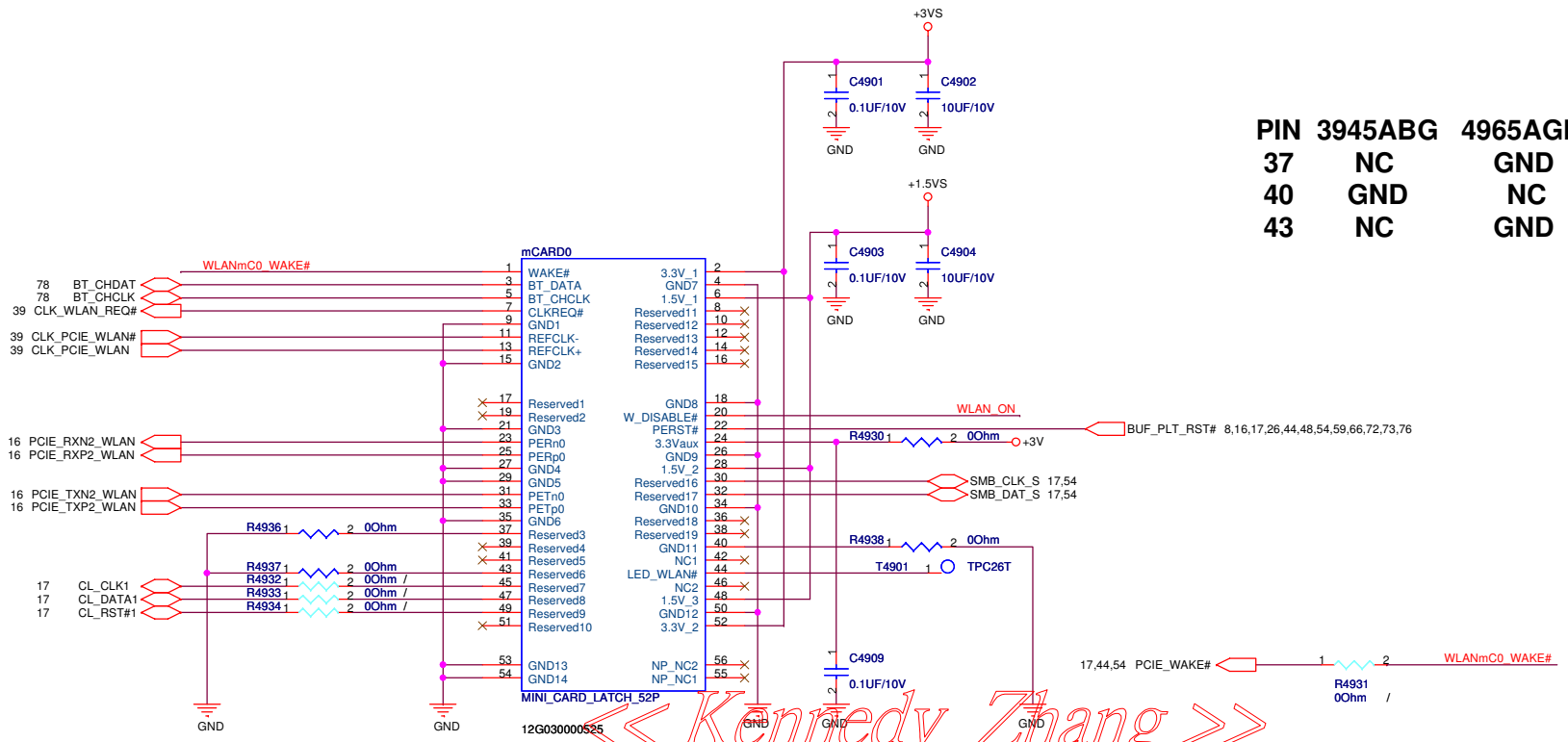


« Kennedy_Zhang »

RESERVED

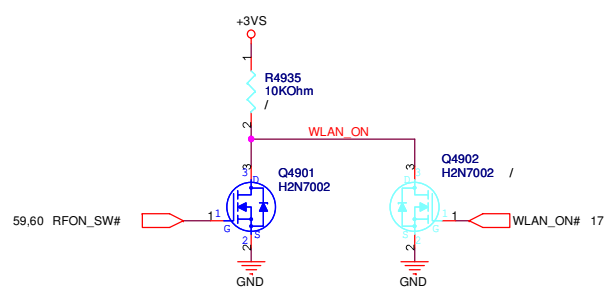
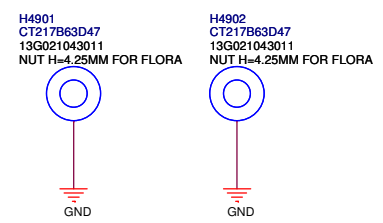
**FOR ROBSON
H=9.0mm**



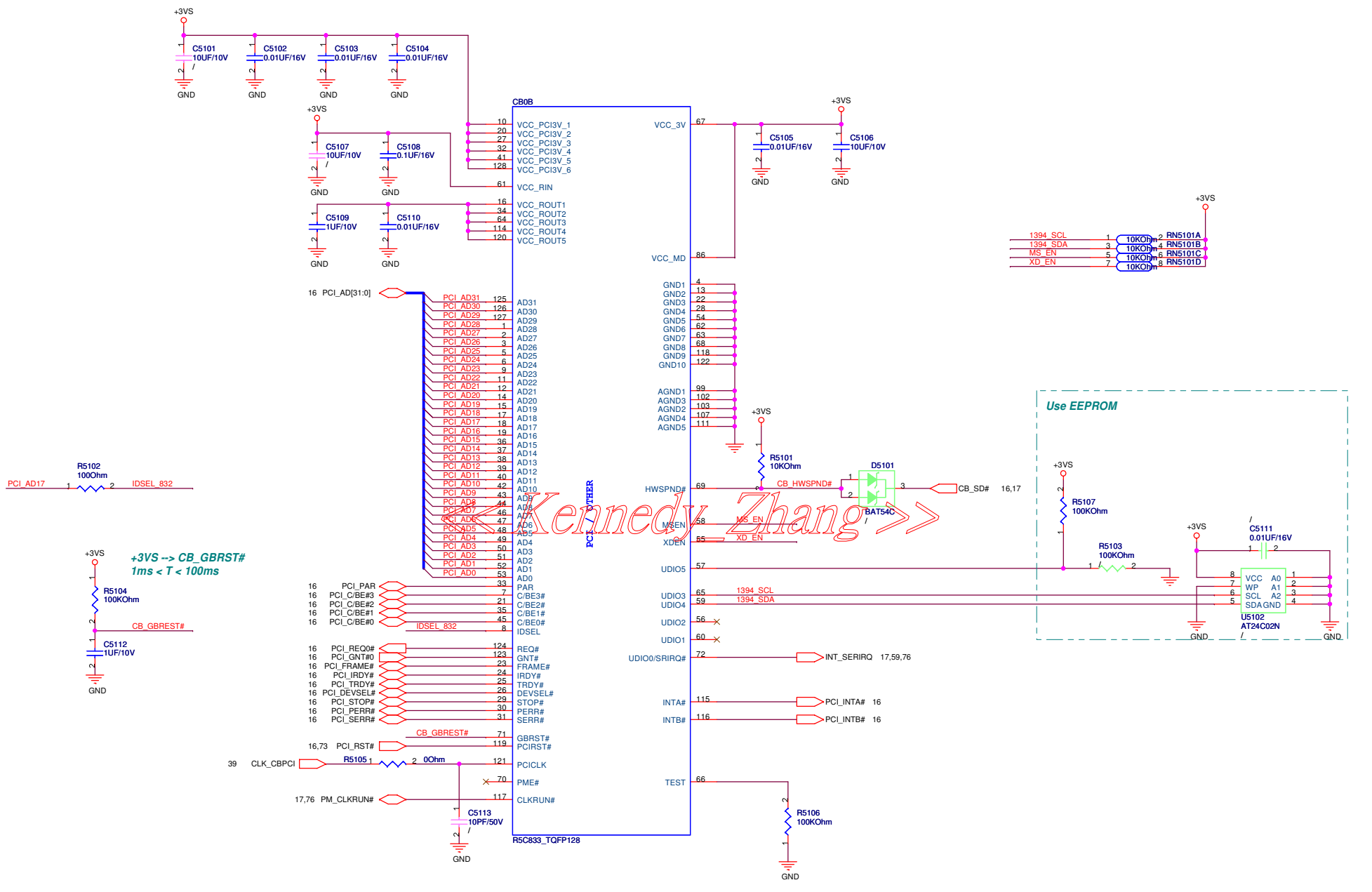


PIN	3945ABG	4965AGN
37	NC	GND
40	GND	NC
43	NC	GND

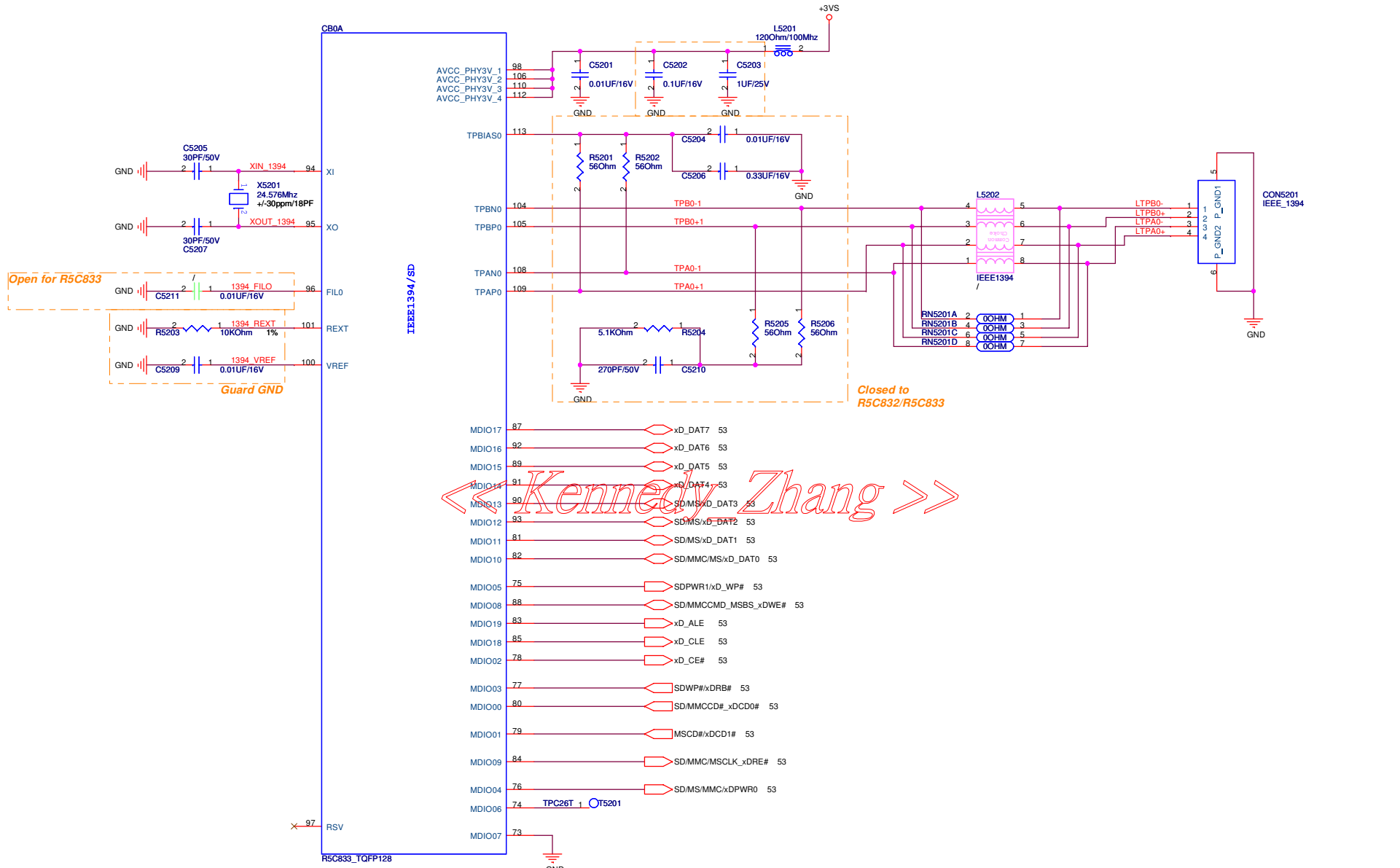
H = 6.75mm
FOR WLAN



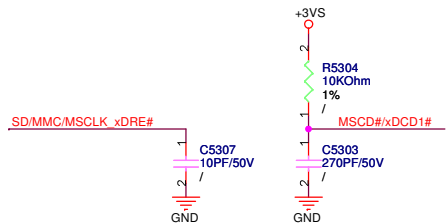
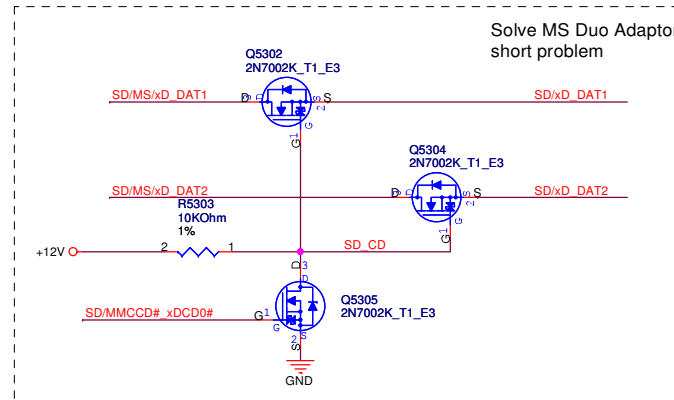
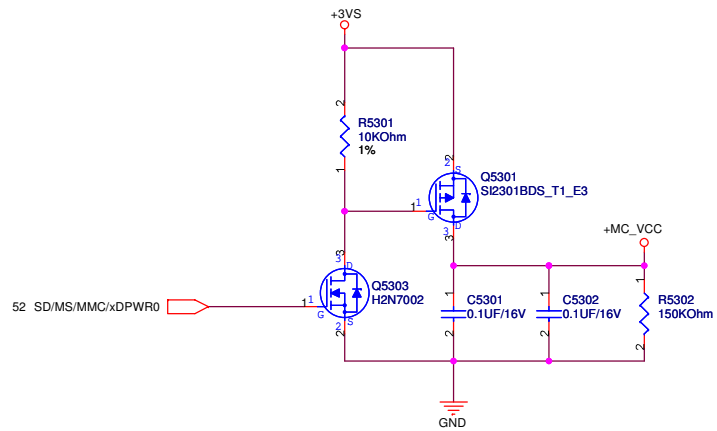
<< Kennedy_Zhang >>



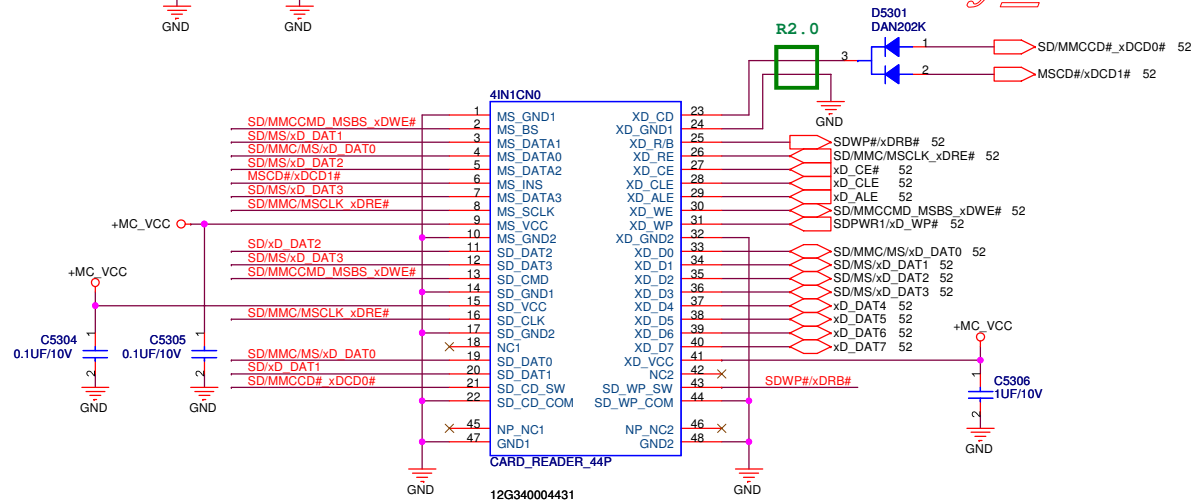
Kennedy Zhang

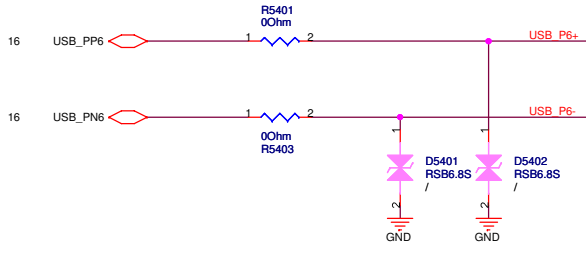
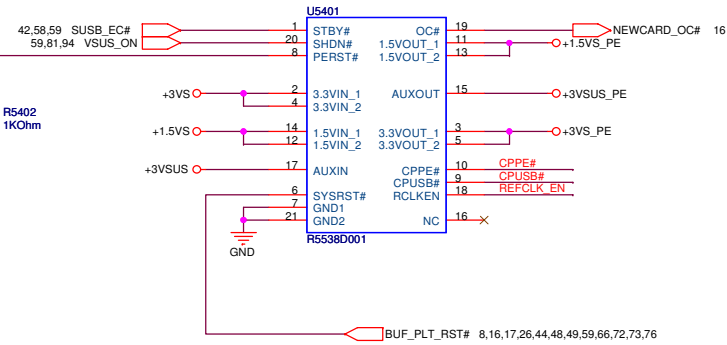


<< Kennedy Zhang >>



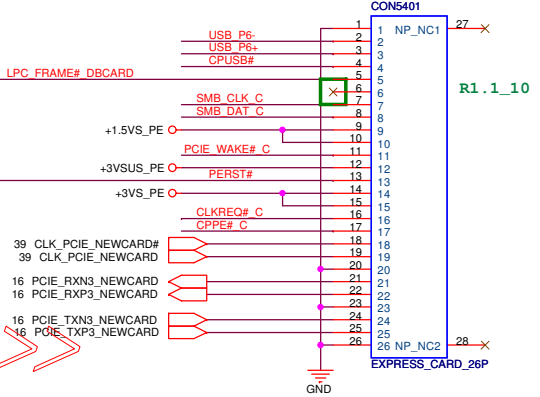
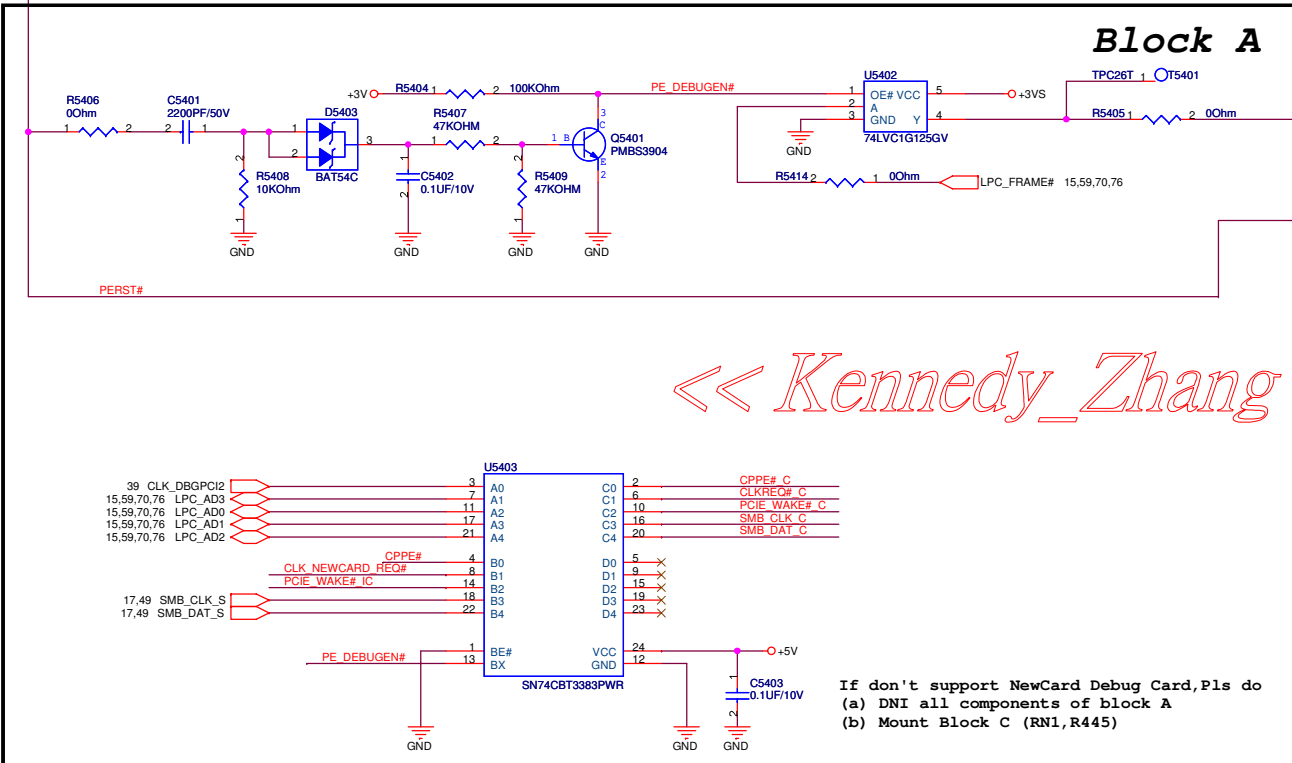
<< Kennedy_Zhang >>



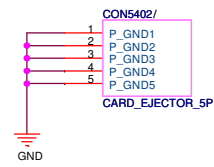


!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

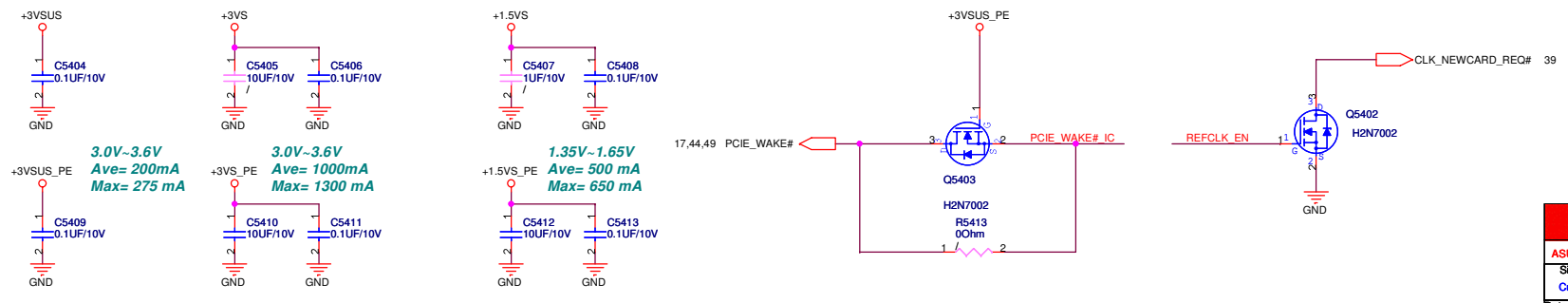
NewCard Header



NewCard Ejecter




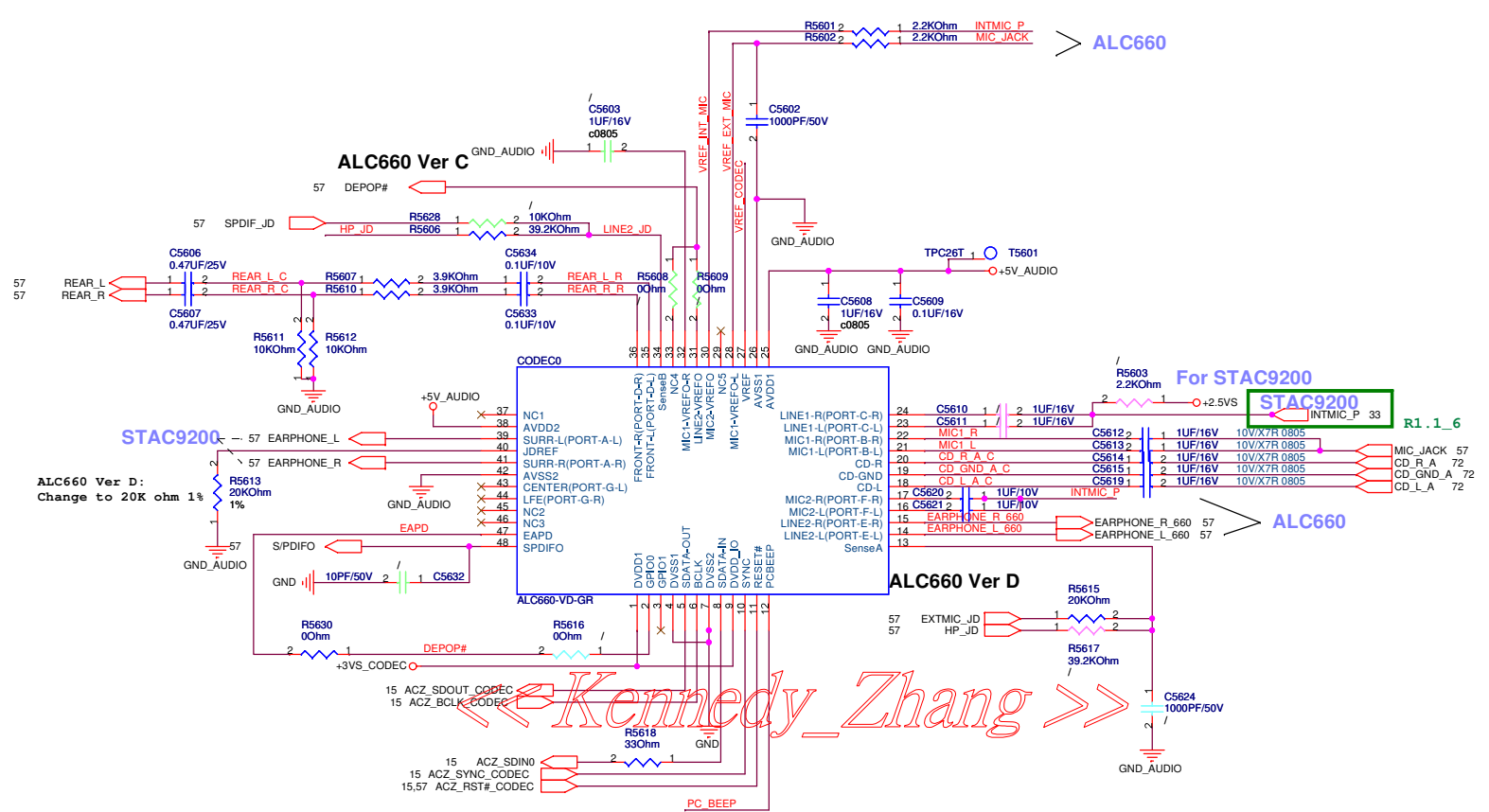
If don't support NewCard Debug Card, Pls do
 (a) DNI all components of block A
 (b) Mount Block C (RN1,R445)



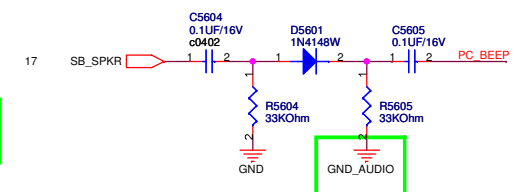
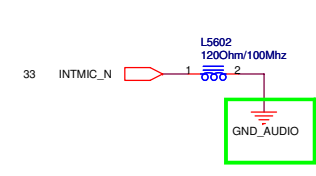
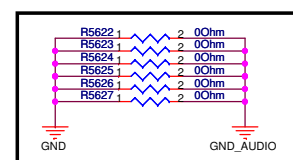
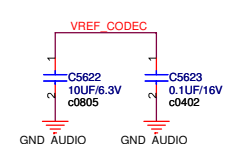
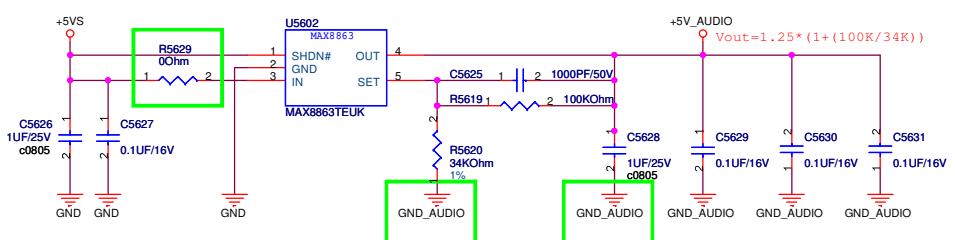
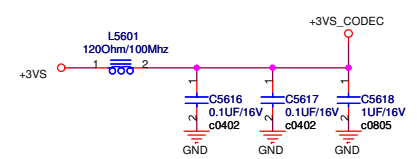
<< Kennedy_Zhang >>

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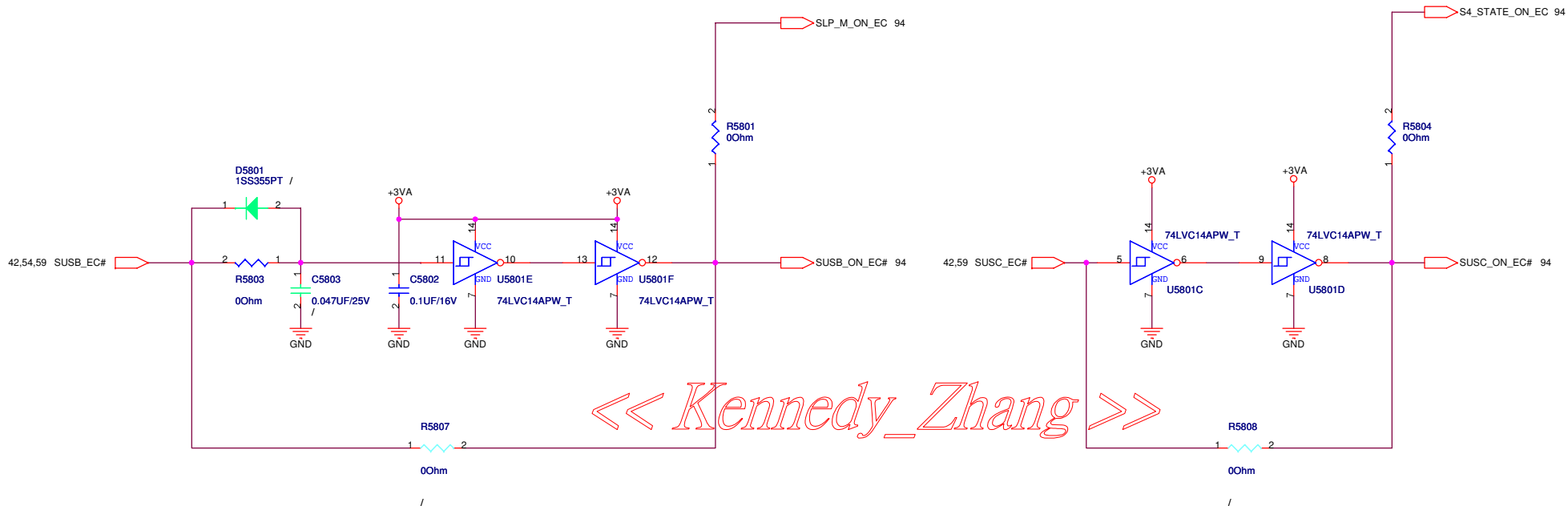
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ASUSTeK COMPUTER INC		Engineer: Jerry Mou	
Size	Project Name		Rev
Custom	F7Sr		1.1
Date:	星期三, 五月 10, 2007	Sheet	55 of 95



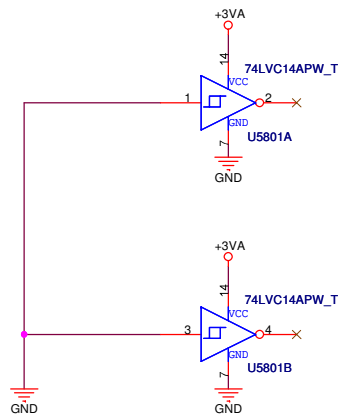
ALC660 Ver D:
Change to 20K ohm 1%

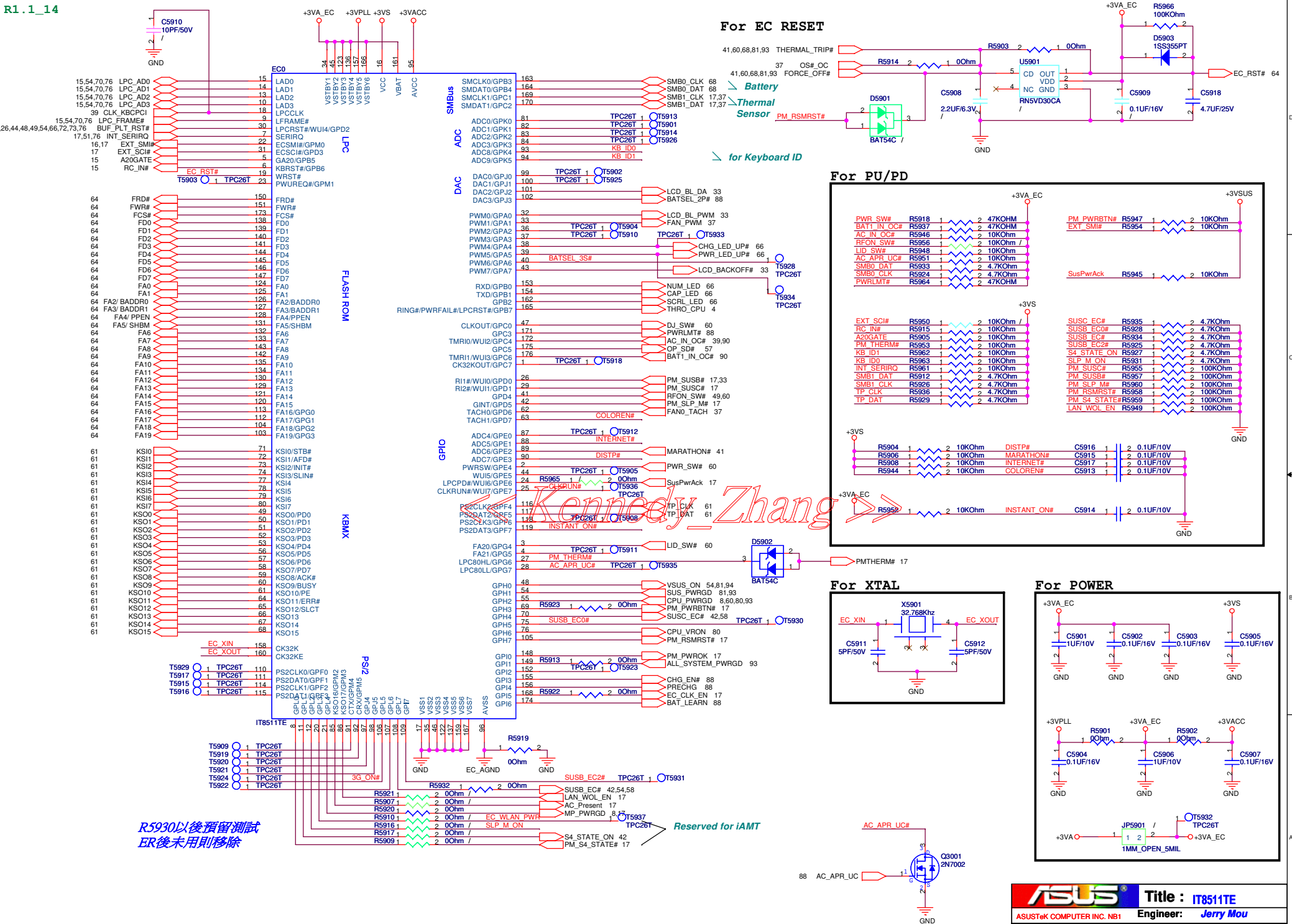


ASUS		Title : CODEC-ALC660	
ASUSTeK COMPUTER INC. N81		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	F7Sr	1.1	
Date: 2007.07.10	Sheet	56	of 95

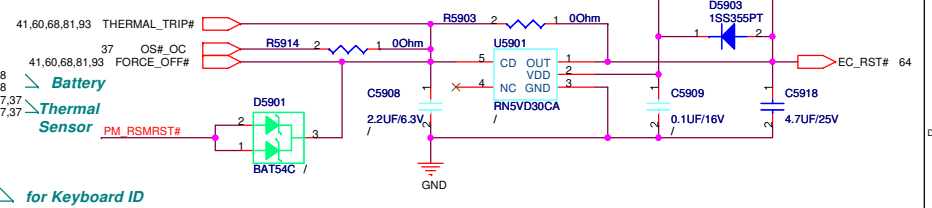


<< Kennedy_Zhang >>

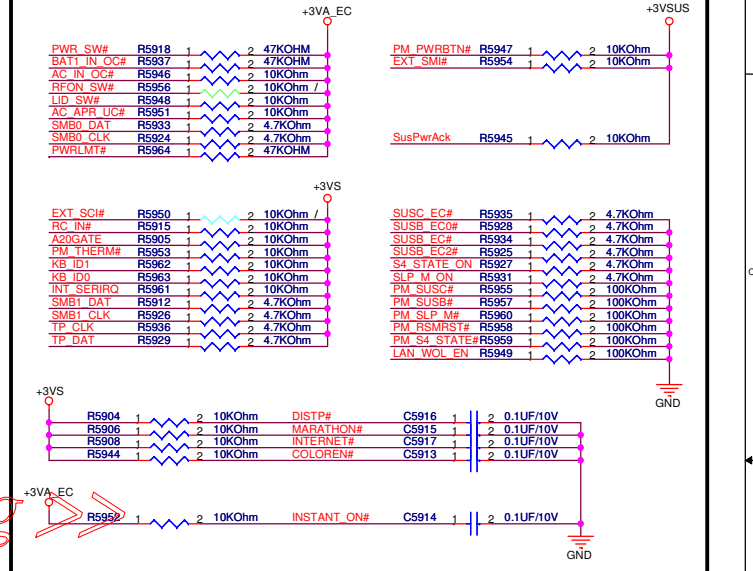




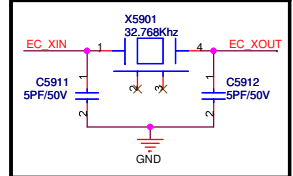
For EC RESET



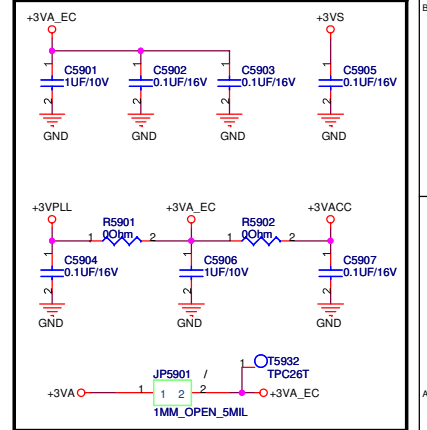
For PU/PD



For XTAL

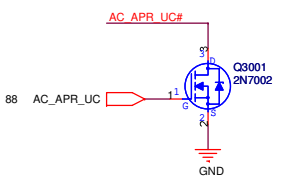


For POWER



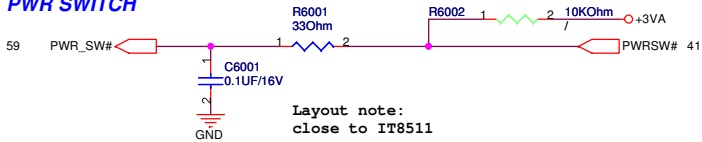
R5930以後預留測試 ER後未用則移除

Reserved for iAMT



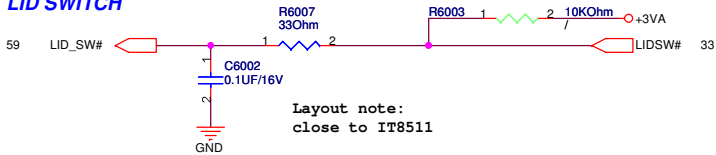
For Switch

PWR SWITCH



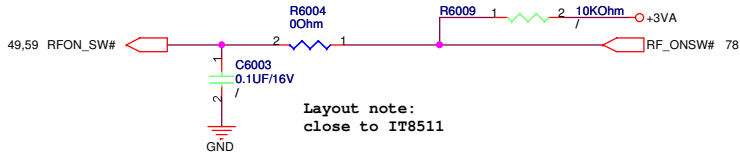
Layout note:
close to IT8511

LID SWITCH



Layout note:
close to IT8511

RF ON SWITCH



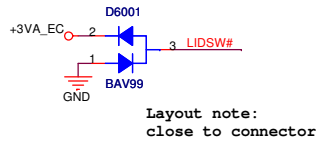
Layout note:
close to IT8511



If you don't use Audio DJ function, please use this schematics

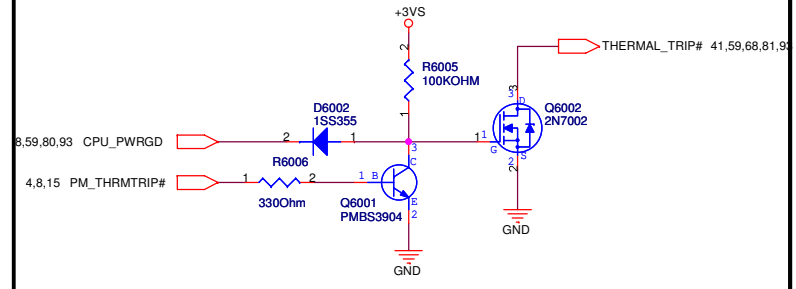
Note:

This LID_EC# is a signal from inverter board, it is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. It needed to add bidirectional diode to protect this pin.



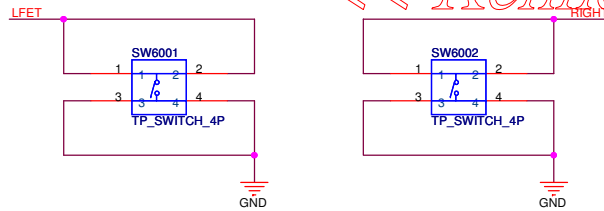
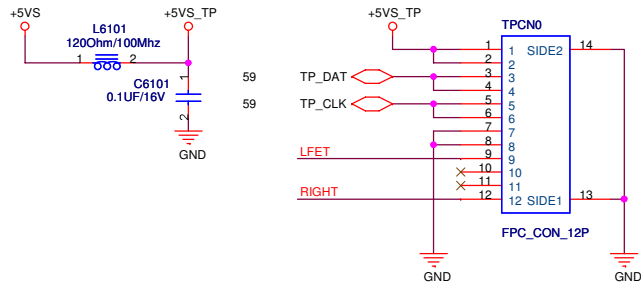
Layout note:
close to connector

For Thermal Control Method



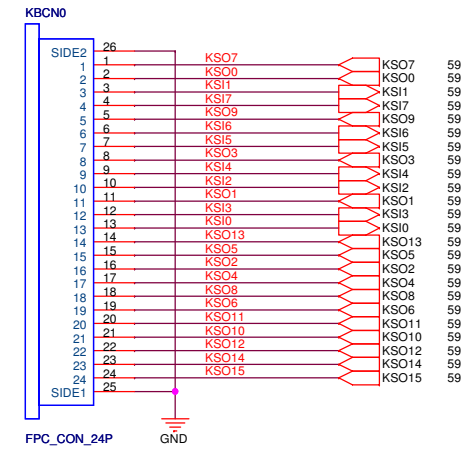
<< Kennedy_Zhang >>

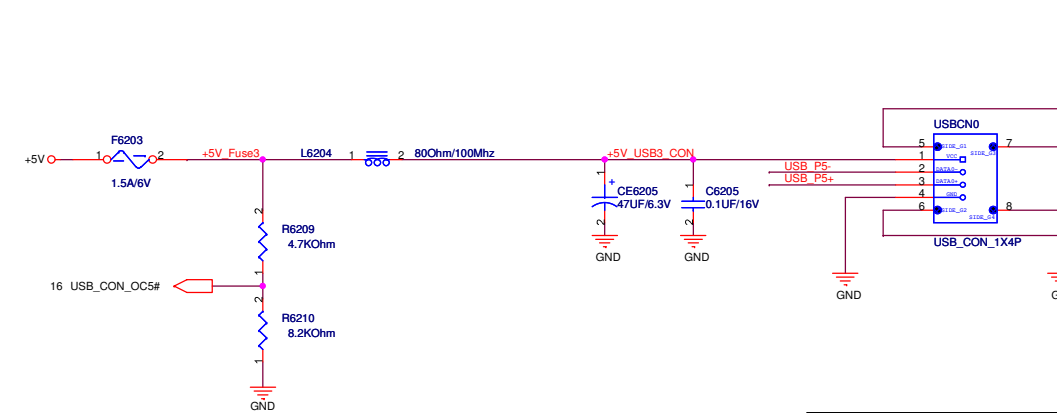
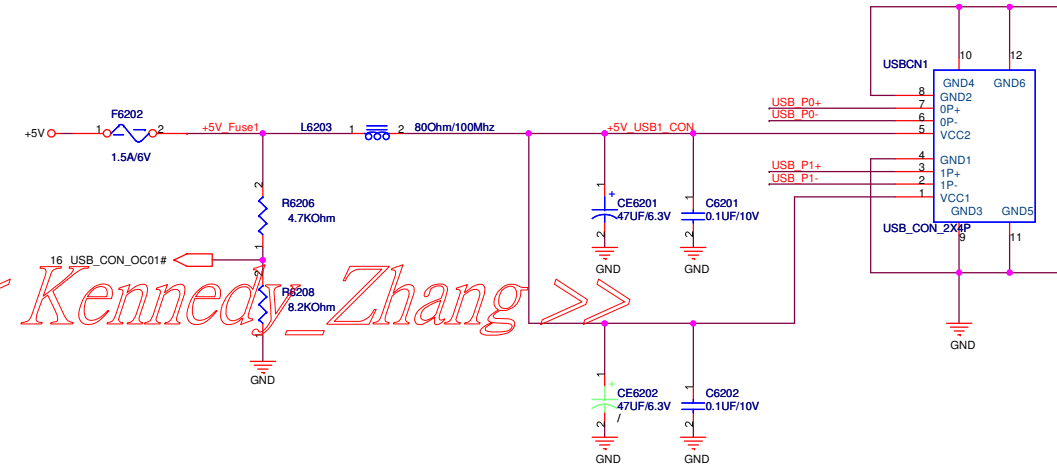
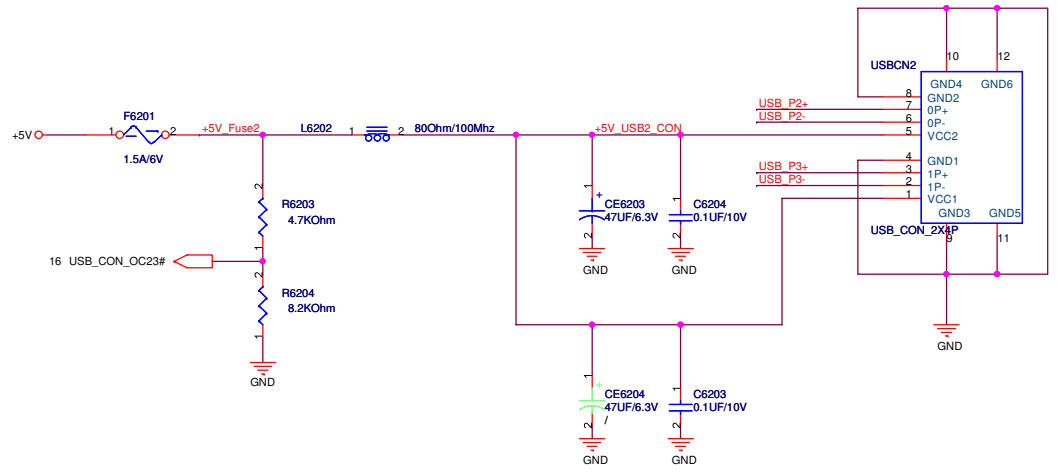
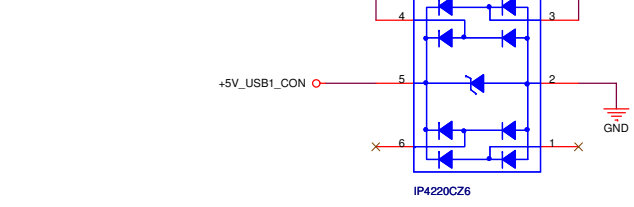
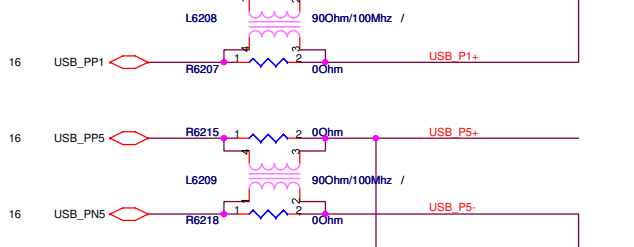
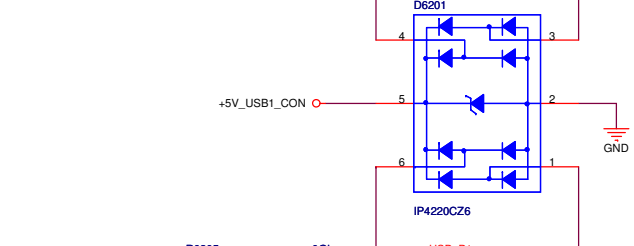
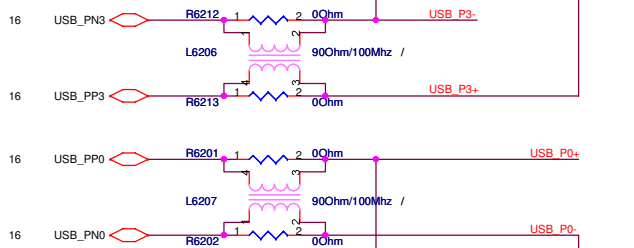
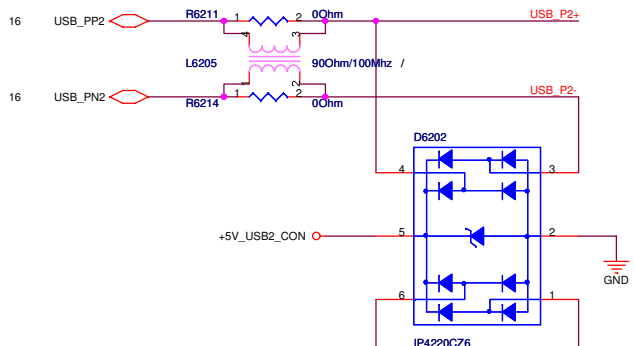
For Touch-Pad



<< Kennedy_Zhang >>

FOR A7 K/B , Matrix B





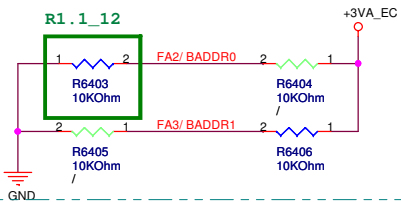
<< Kennedy_Zhang >>

<< Kennedy_Zhang >>

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

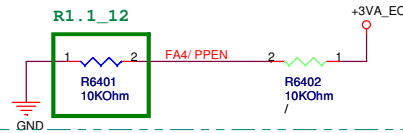
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

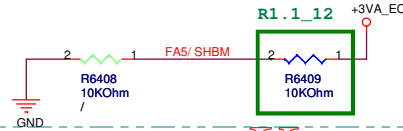
FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

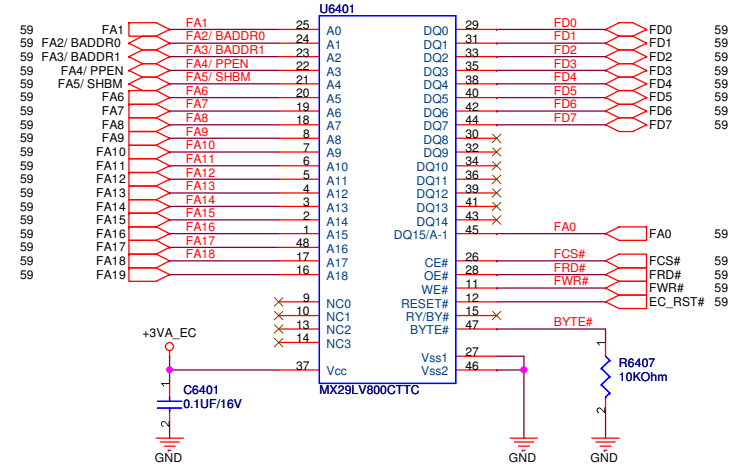


FA5/ SHBM

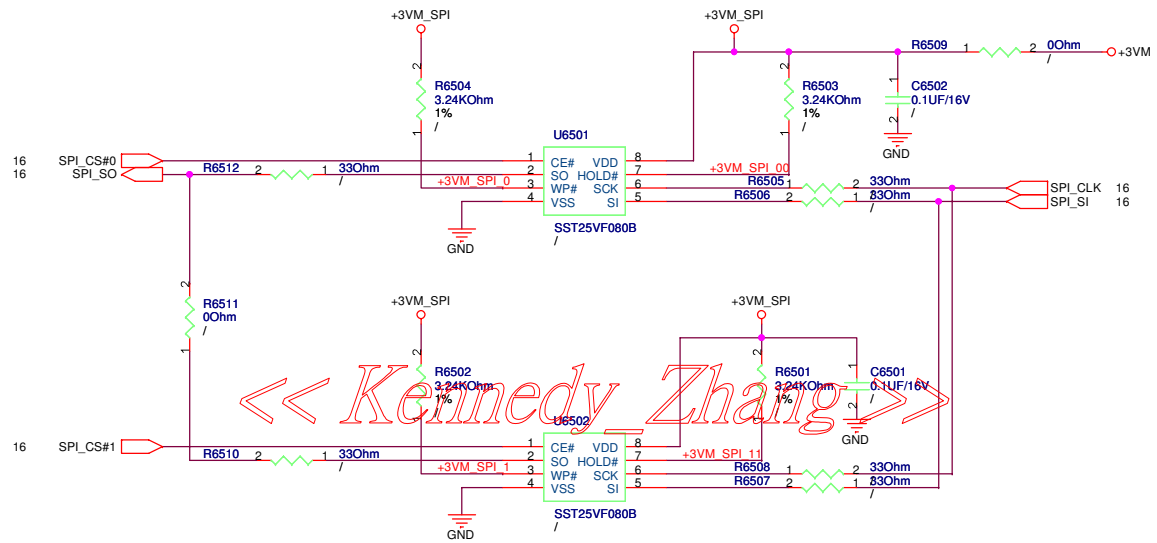
- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS



8M TSOP

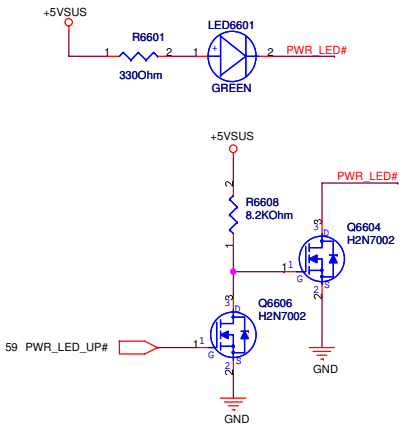


<< Kennedy_Zhang >>

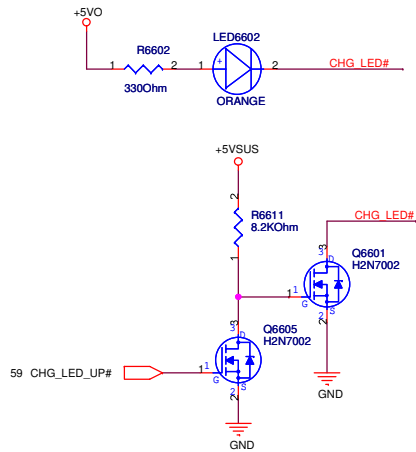


« Kennedy Zhang »

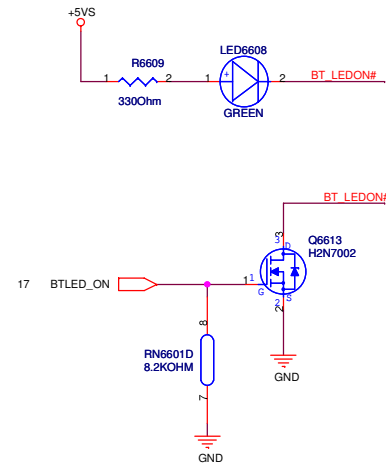
For Power LED



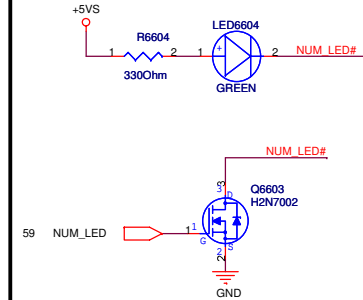
For Battery LED



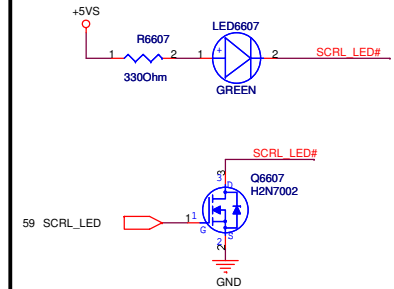
For BT LED



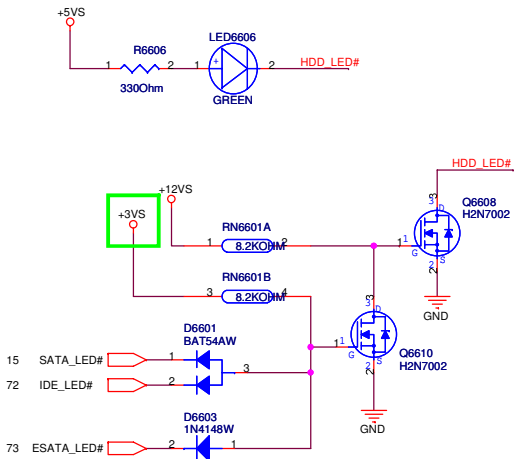
For Number Lock



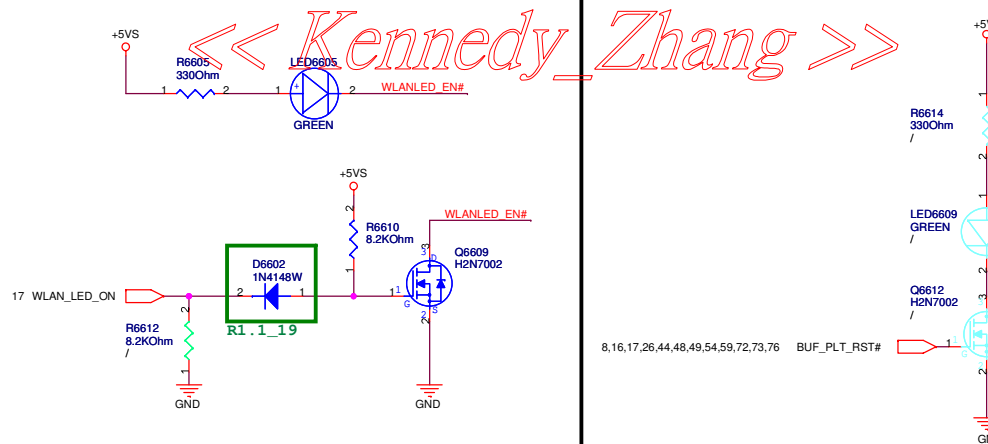
For Scroll Lock



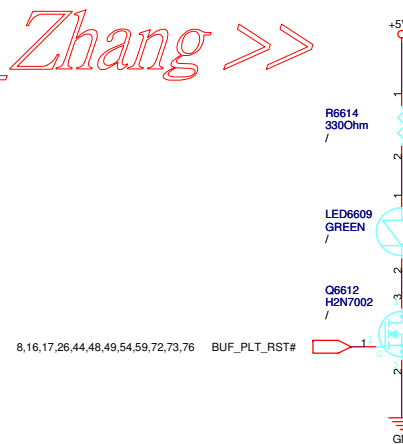
For SATA/IDE LED



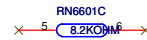
For WireLess LED



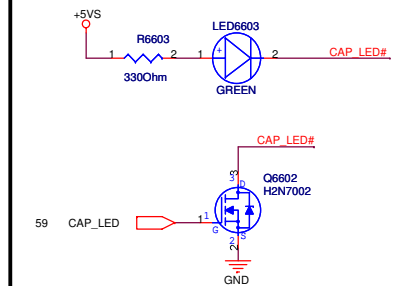
Reserved LED



<< Kennedy Zhang >>

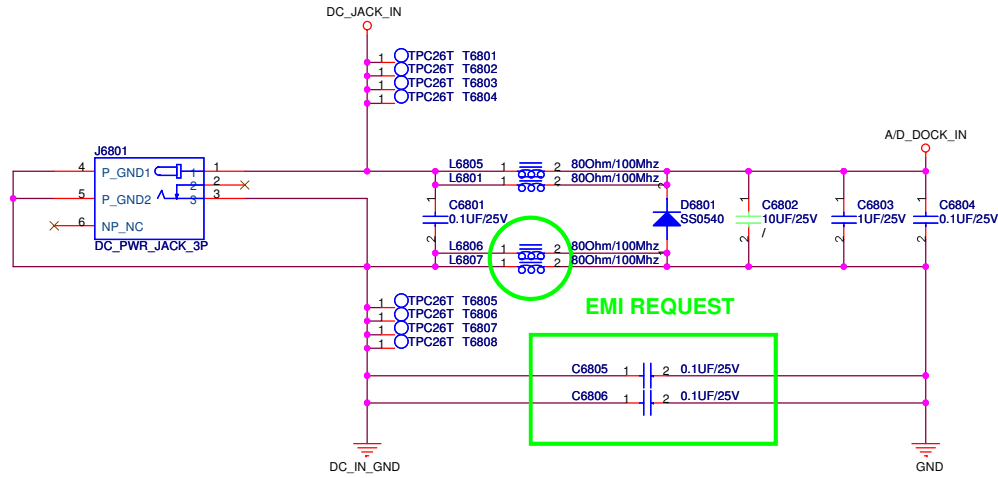


For Caps. Lock

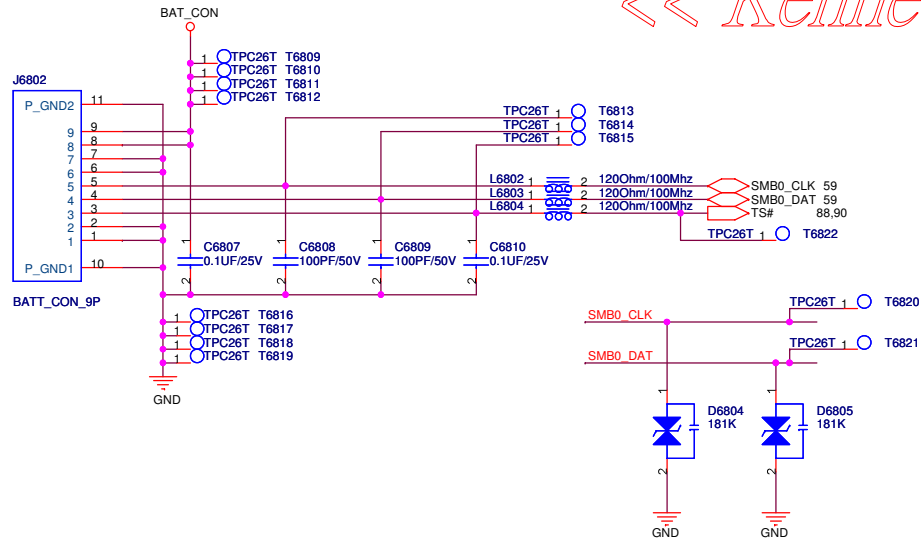


<< Kennedy_Zhang >>

DC IN

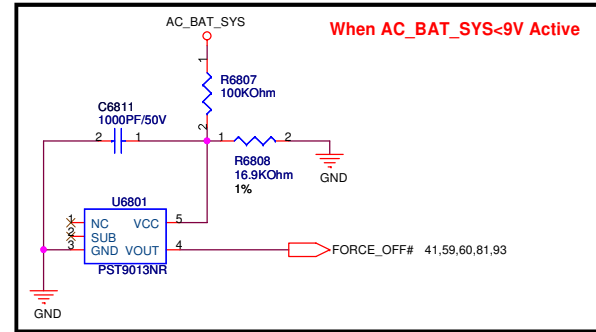


BAT IN



<< Kennedy_Zhang >>

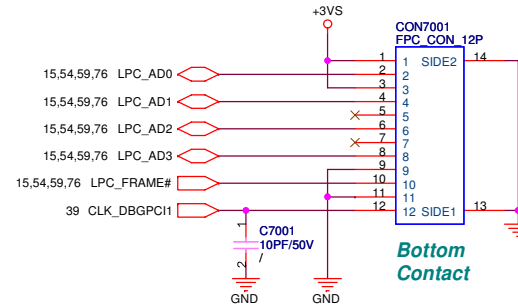
Without Battery & Pull out Adapter



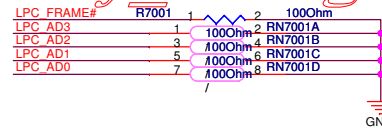
<< Kennedy_Zhang >>

For Debug

**If support NewCard Debug Card,
Pls don't mount all components.**

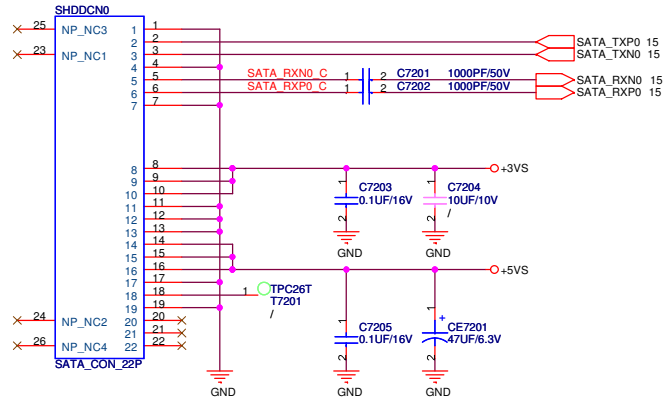


<< Kennedy Zhang >>

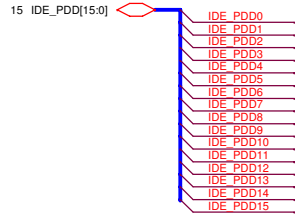


<< Kennedy_Zhang >>

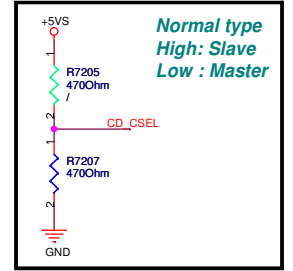
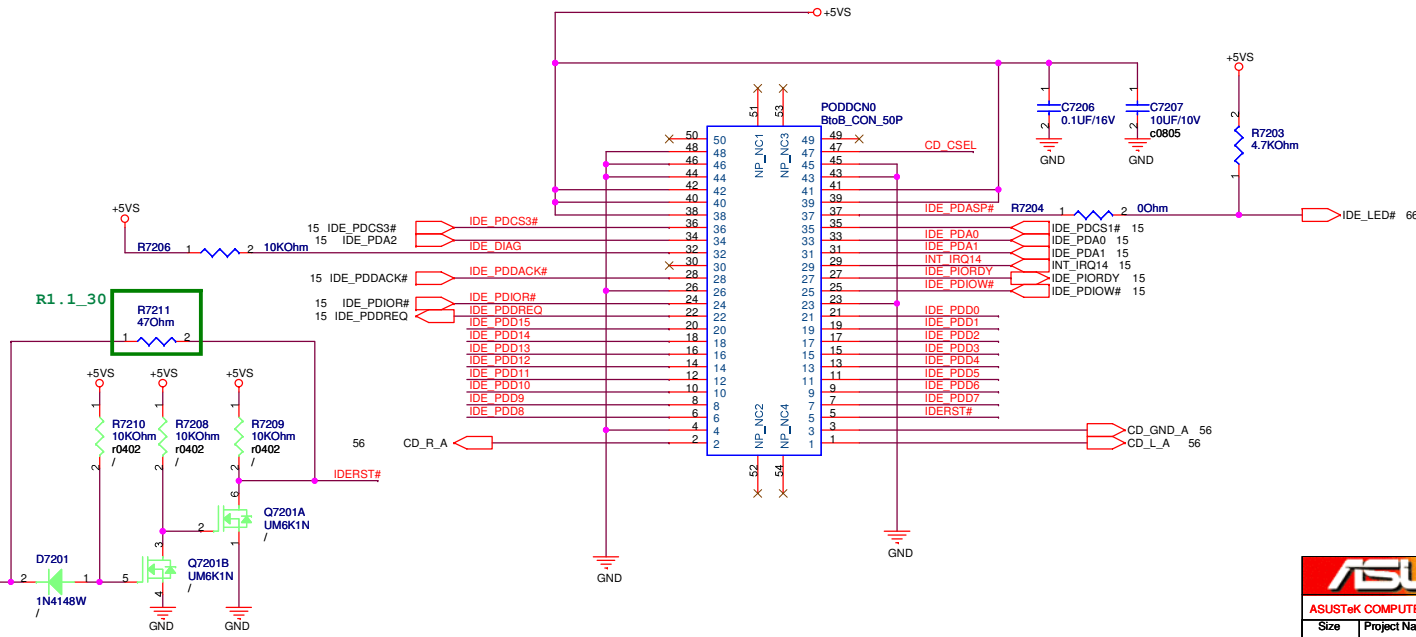
SATA HDD

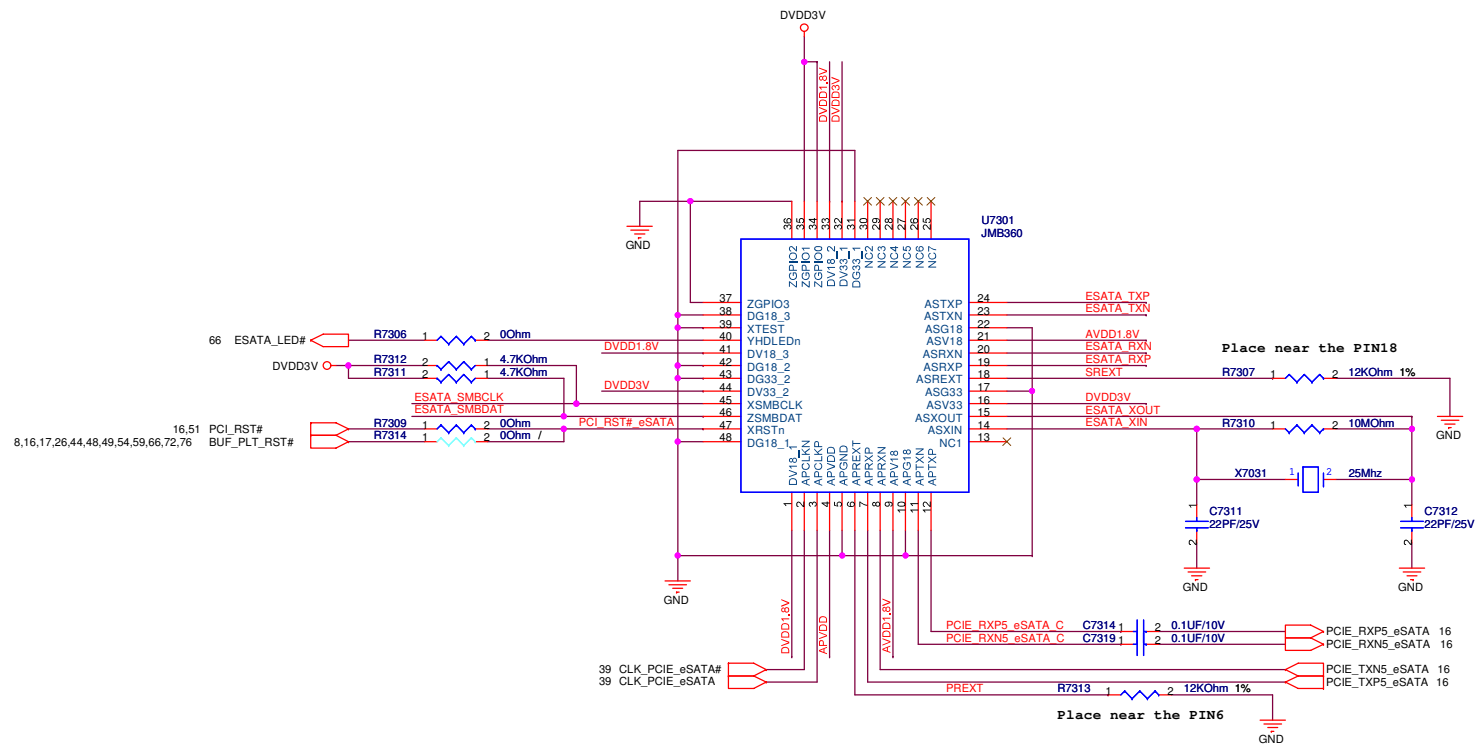


ODD



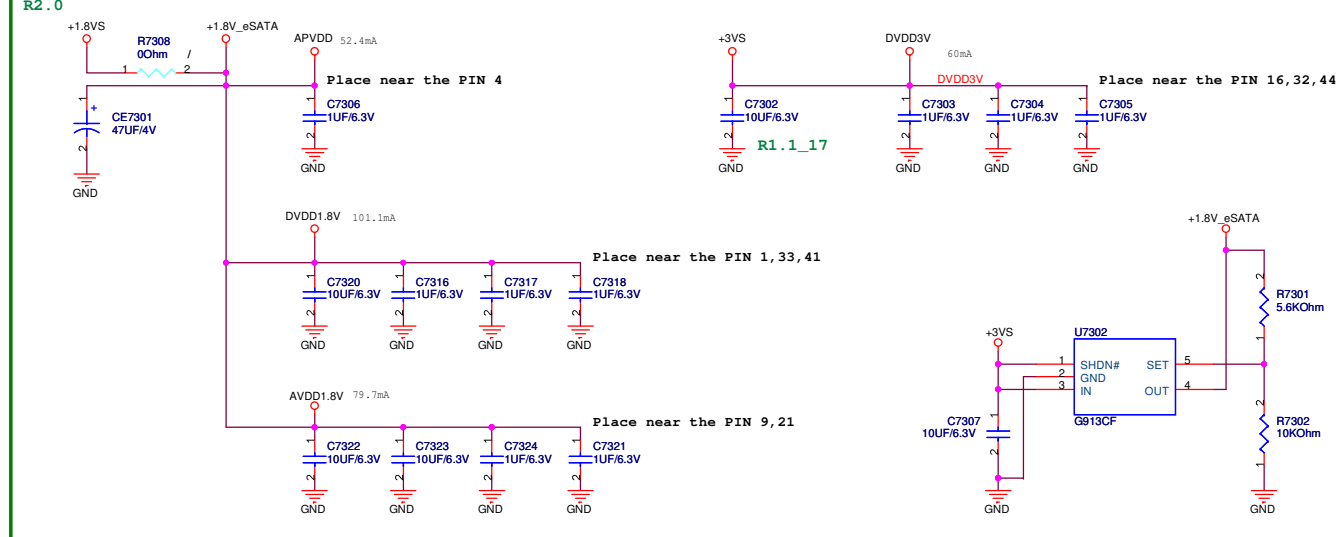
<< Kennedy_Zhang >>



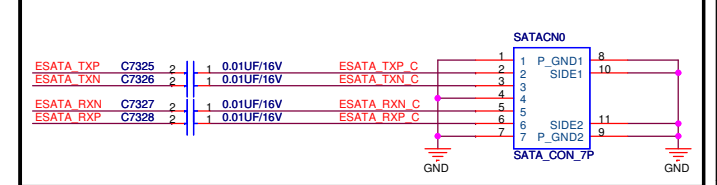


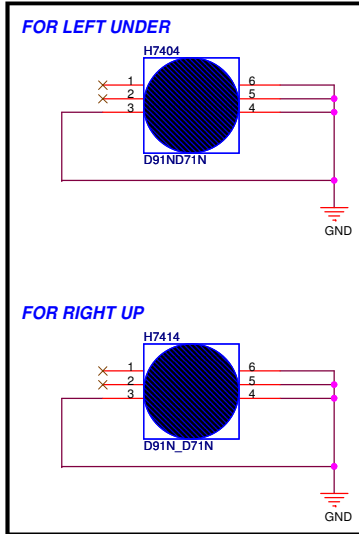
<< Kennedy_Zhang >>

eSATA Power

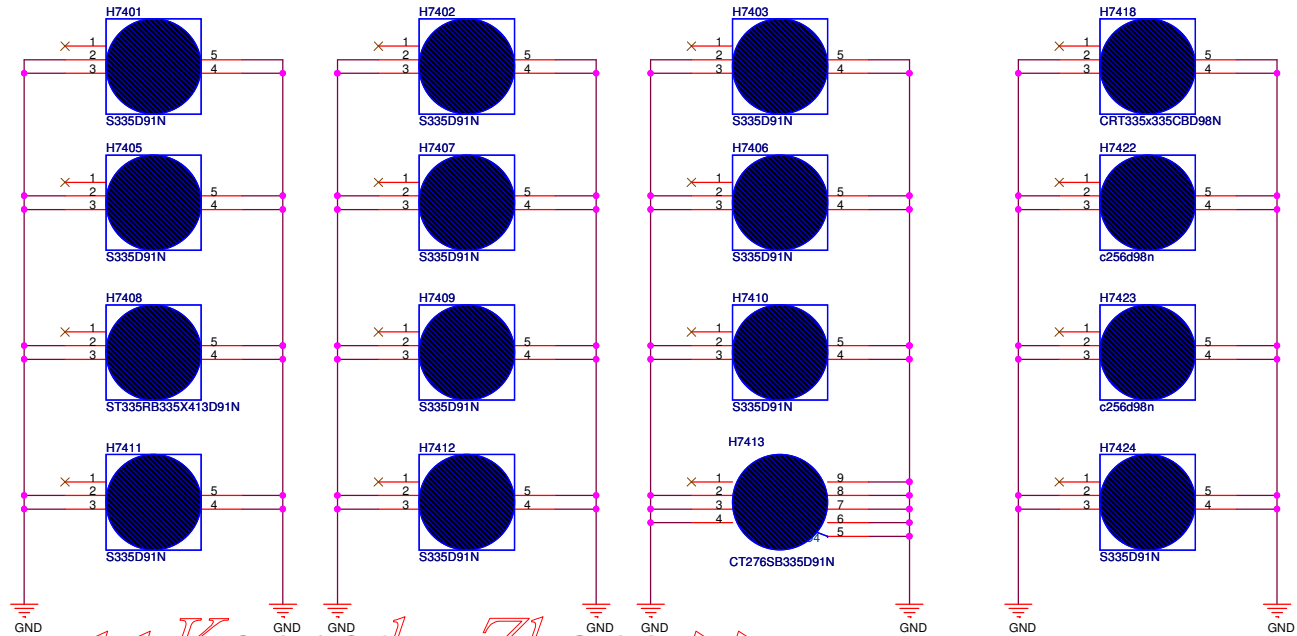


eSATA Connector



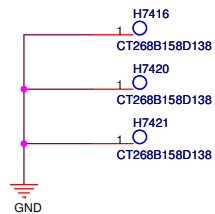


FOR SCREW HOLE

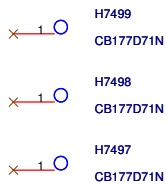
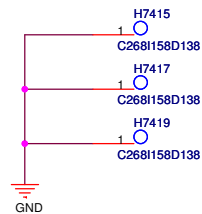


<< Kennedy_Zhang >>

FOR CPU

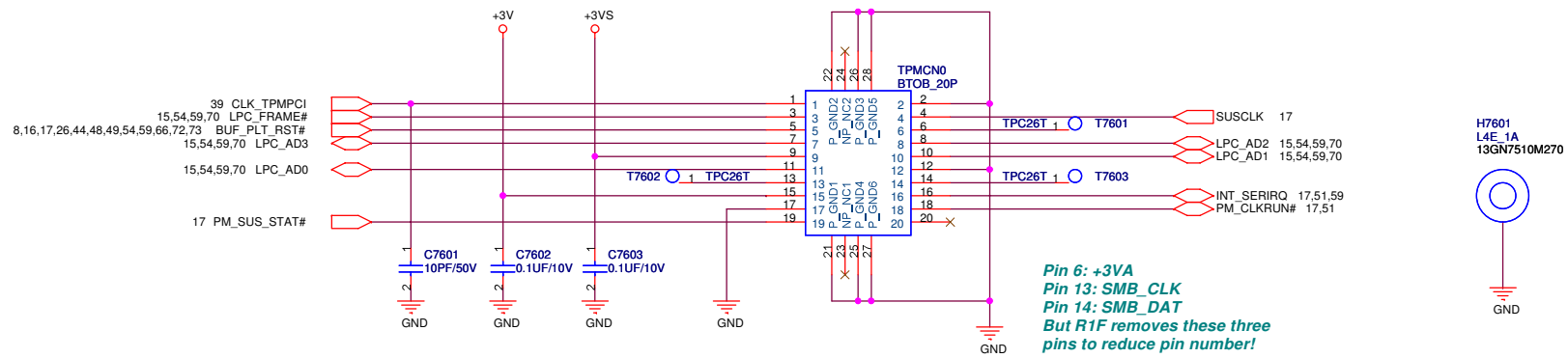


FOR VGA




<< Kennedy_Zhang >>

For TPM module

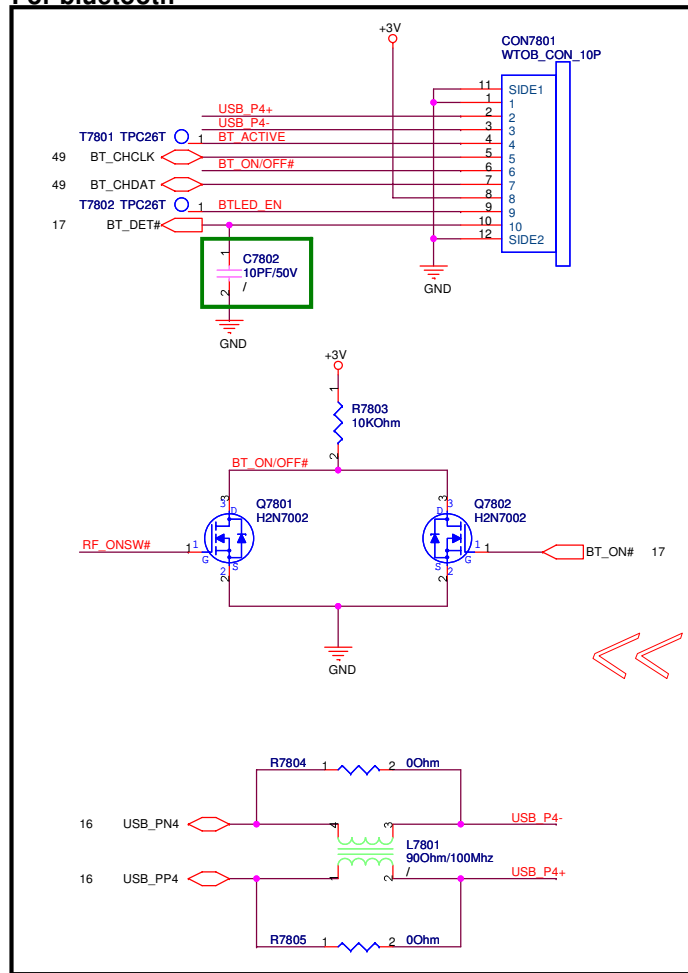


<< Kennedy_Zhang >>

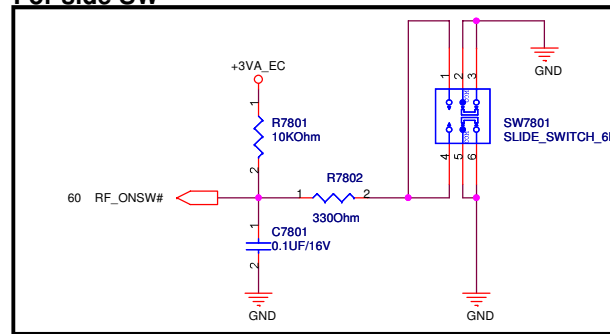
<< Kennedy_Zhang >>

		Title : SPRING
ASUSTeK COMPUTER INC		Engineer: Jerry Mou
Size Custom	Project Name F7Sr	Rev 1.1
Date: 星期四, 五月 10, 2007		Sheet 77 of 95

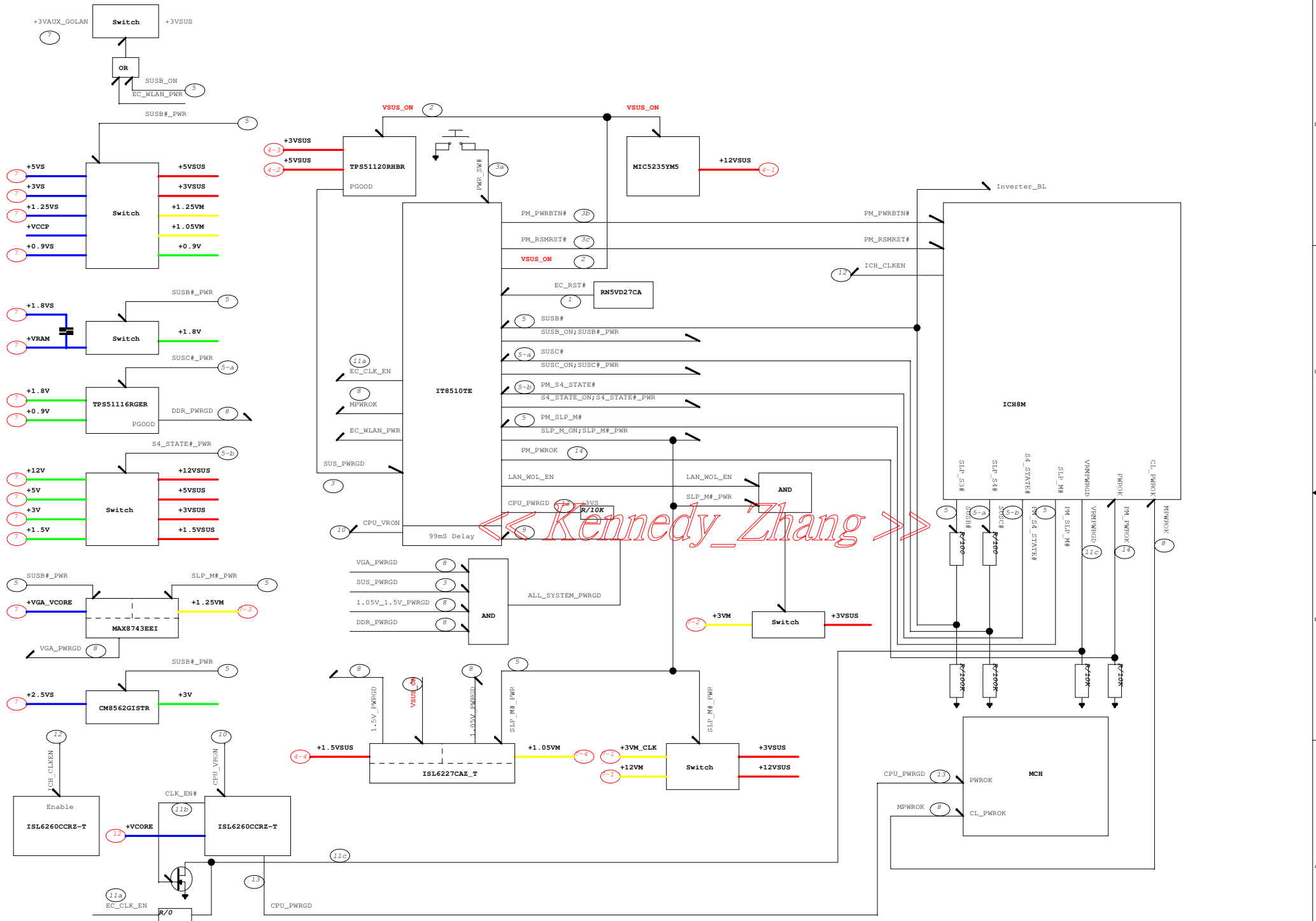
For bluetooth

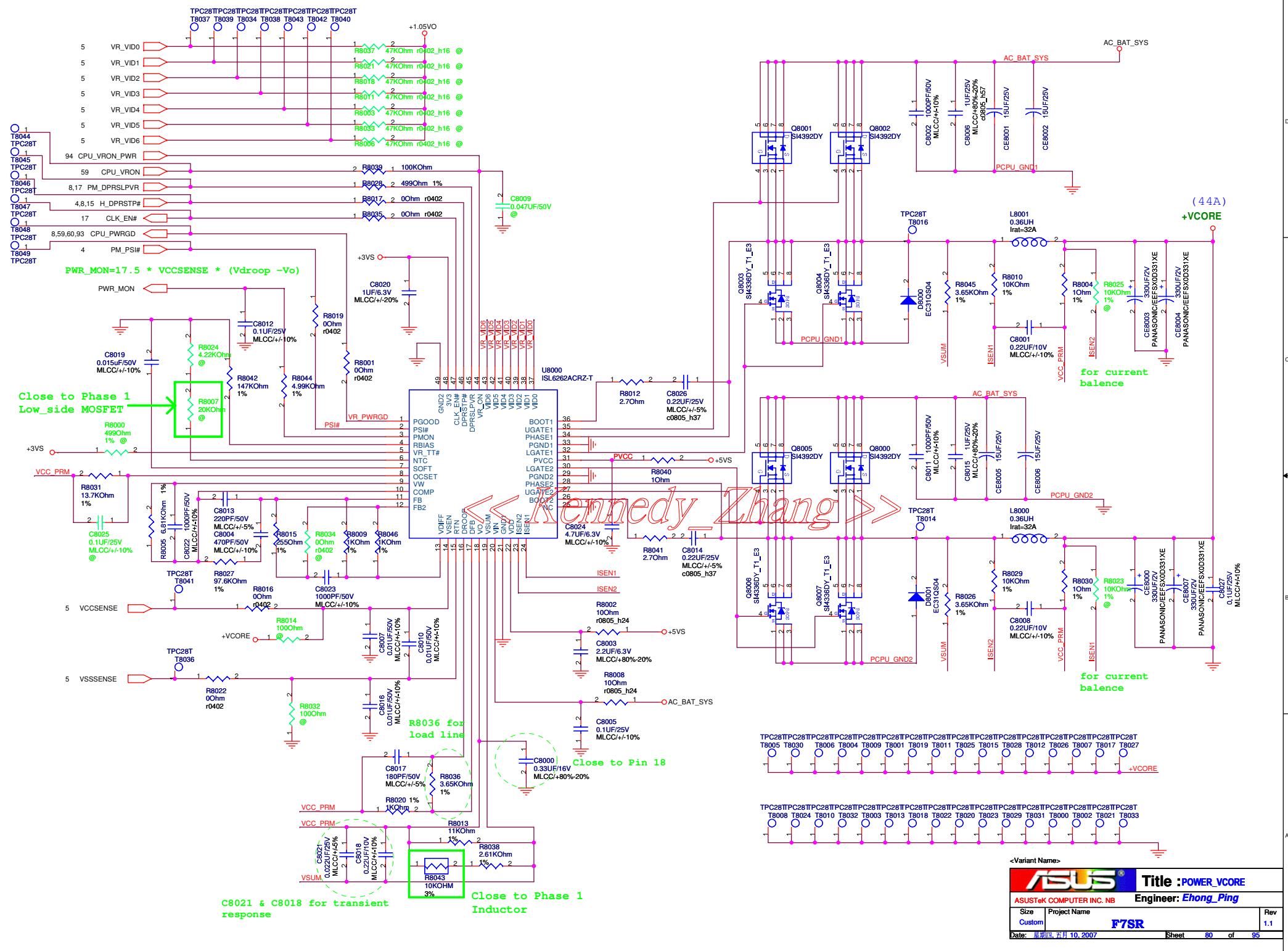


For side SW



<< Kennedy_Zhang >>

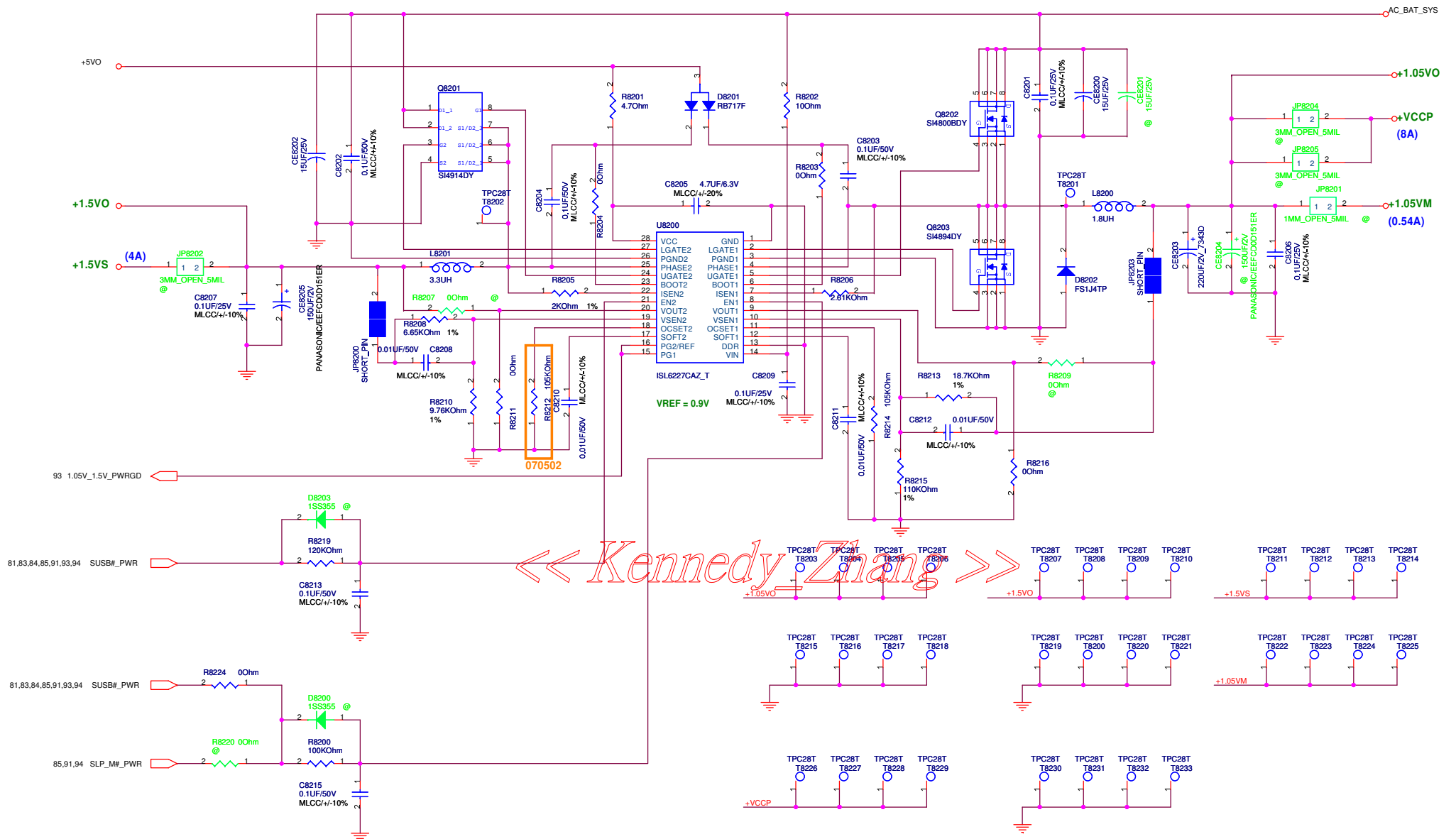




C8021 & C8018 for transient response

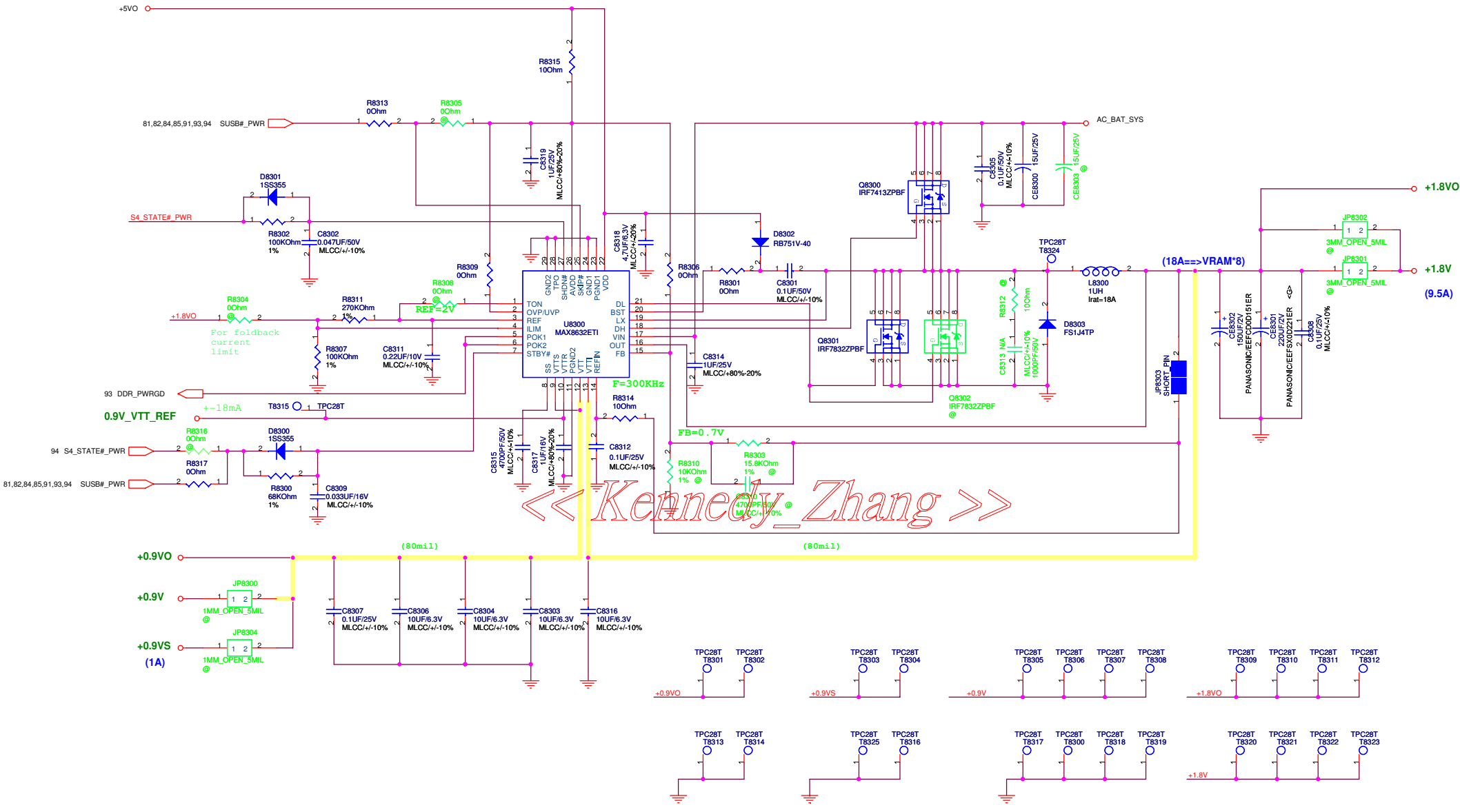
Close to Phase 1 Inductor

<Variant Name>		ASUS Title :POWER_VCORE	
ASUSTek COMPUTER INC. NB		Engineer: Hong_Ping	
Size	Project Name	Rev	
Custom	F7SR	1.1	
Date: 星期四, 五月 10, 2007	Sheet	80	of 95



<Variant Name>

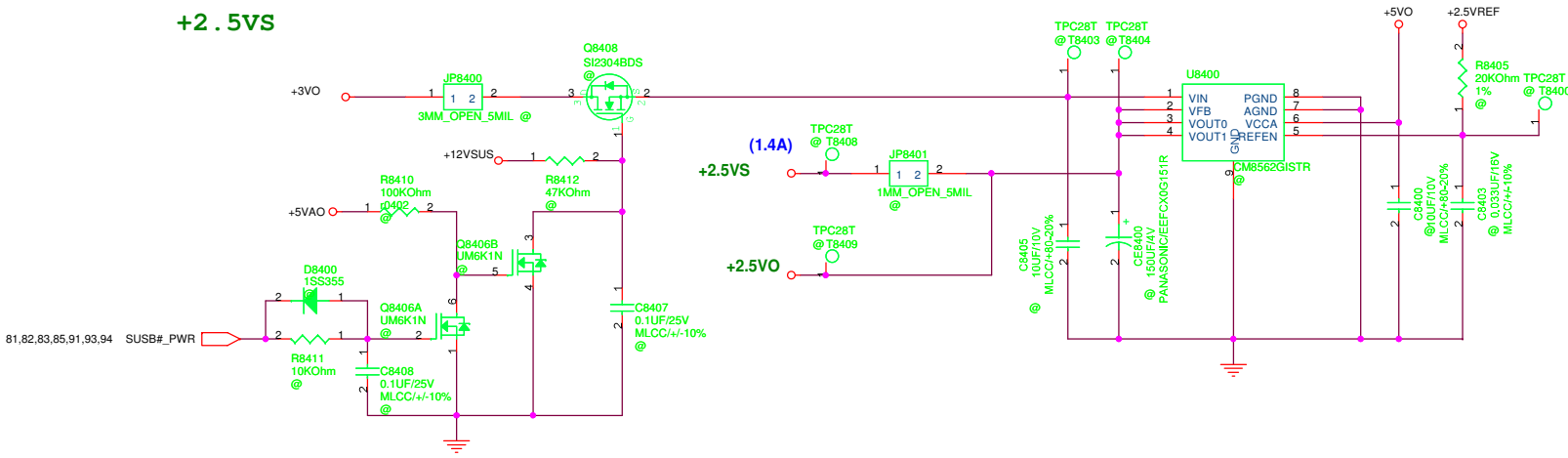
ASUS		Title : POWER_IO_1.5VS & 1.05VS
<OrgName>		Engineer:
Size	Project Name	Rev
Custom	F7SR	1.1
Date: 星期四, 五月 10, 2007	Sheet	82 of 95



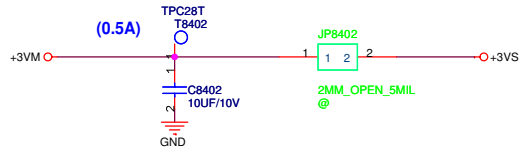
<Variant Name>

ASUS		Title : POWER_I/O_DDR & VTT	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size	Project Name	Rev	
Custom	F7SR	1.1	
Date: 华硕, 五月 10, 2007	Sheet 83	of 95	

+2.5VS

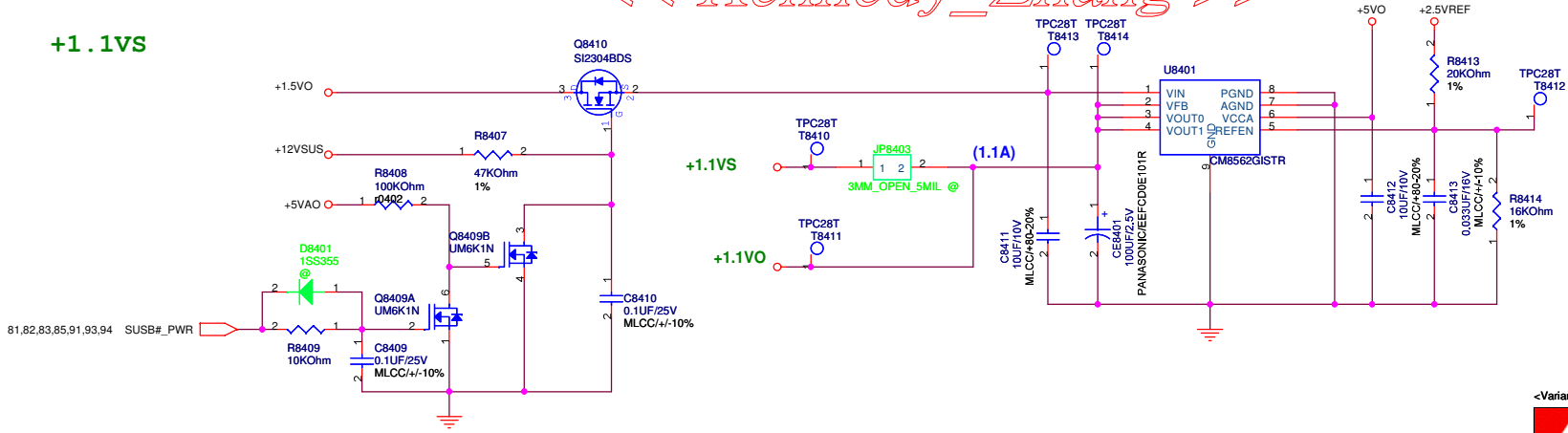


+3VM



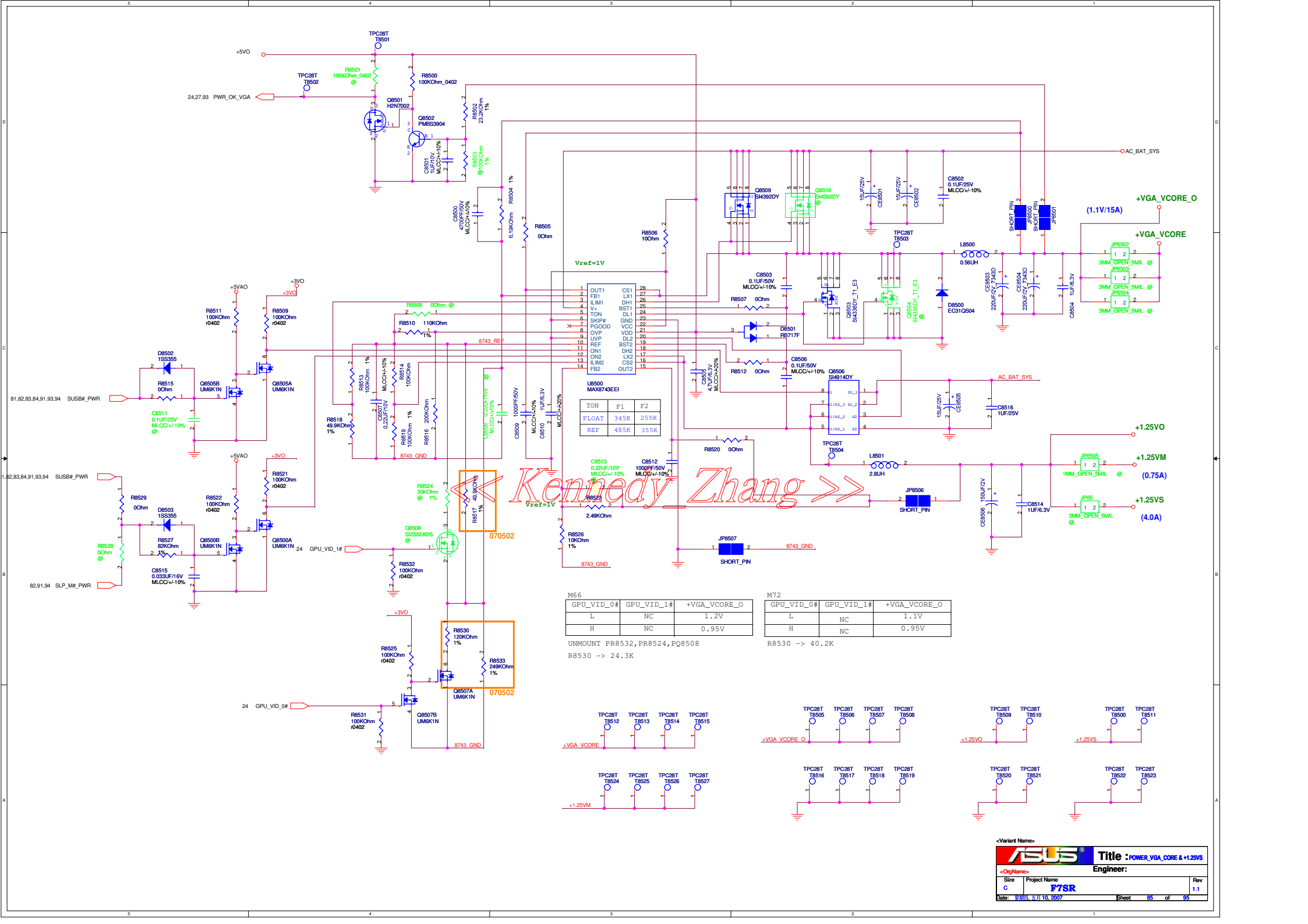
<< Kennedy_Zhang >>

+1.1VS



<Variant Name>

ASUS		Title POWER_I/O_+3VM & +2.5VS
Engineer:		
Size	Project Name	Rev
Custom	F7SR	1.1
Date: 星期四, 五月 10, 2007	Sheet 84	of 95



Vref=1V

OUT1	CS1	27
FB1	LK1	28
ILM1	DH1	28
V+	BST1	28
TON	DL1	28
SKIP#	GND	33
PGOOD	VCC	21
OV	VDD	21
UVP	DL2	22
REF	BST2	18
ON1	DH2	18
ON2	LX2	17
ILM2	CS2	15
FB2	OUT2	15

U8500 MAX8743EEI

TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

M66

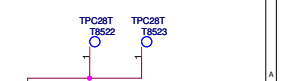
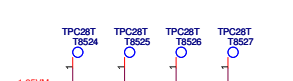
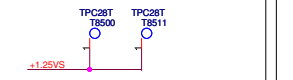
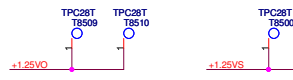
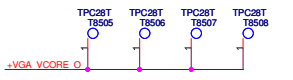
GPU_VID_0#	GPU_VID_1#	+VGA_VCORE_O
L	NC	1.2V
H	NC	0.95V

M72

GPU_VID_0#	GPU_VID_1#	+VGA_VCORE_O
L	NC	1.1V
H	NC	0.95V

UNMOUNT PR8532, PR8524, PQ8508
R8530 -> 24.3K


R8530 -> 40.2K




Kennedy Zhang

<< Kennedy_Zhang >>

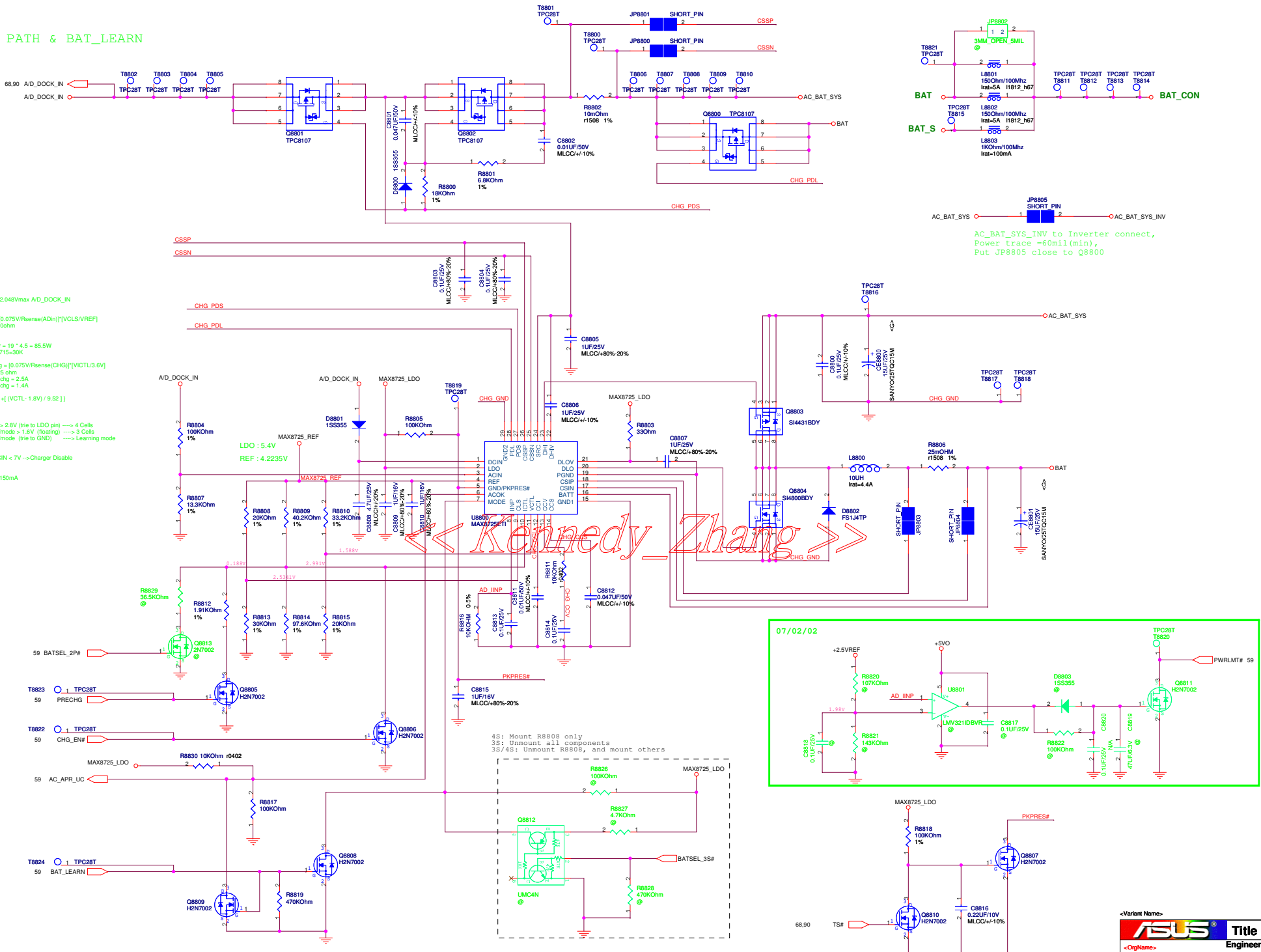
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		Title : N/A
<OrgName>		Engineer:
Size	Project Name	Rev
A	F7SR	1.1
Date: 星期四, 五月 10, 2007		Sheet 86 of 95

<< Kennedy_Zhang >>

<Variant Name>		Title : N/A	
		Engineer:	
<OrgName>	Project Name	Rev	1.1
C	F7SR	Date:	2007.5.10
Date: 2007.5.10		Sheet	87 of 95

POWER PATH & BAT_LEARN



● AC_IN Threshold 2.045Vmax A/D_DOCK_IN > 17.44V active

Adapter lin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
 Rsense(ADin) = 0.010ohm
 VCLS = 2.5341V
 => lin(max) = 4.5A
 => Constant Power = 19 * 4.5 = 85.5W
 => R5710 = 20K, R5715 = 30K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
 Rsense(CHG) = 0.025ohm
 VICTL = 3V => Ichg = 2.5A
 VICTL = 1.88V => Ichg = 1.4A

Vbatt = Cell * [Vref + (VCTL - 1.8V) / 9.52]
 VCTL = 1.588V
 => Vbatt = 4.2V

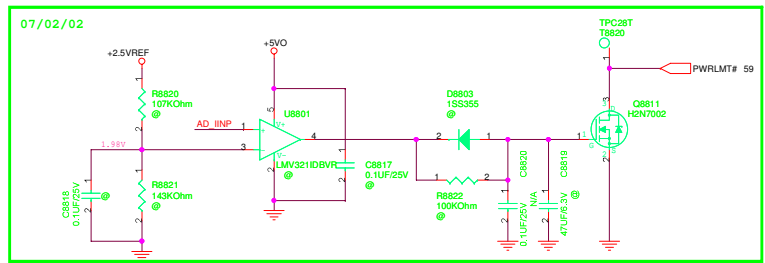
Mode pin : Vmode > 2.6V (tie to LDO pin) => 4 Cells
 2.0 > Vmode > 1.6V (floating) => 3 Cells
 0.8 > Vmode (tie to GND) => Learning mode

VICTL = 0.8V or DCIN < 7V => Charger Disable

Preccharge current = 150mA


AC_BAT_SYS_INV to Inverter connect,
 Power trace = 60mil(min),
 Put JP8805 close to Q8800

« Kennedy Zhang »

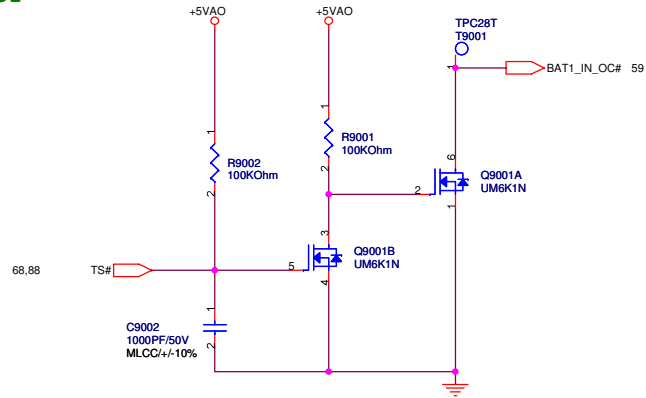


4S: Mount R8808 only
 3S: Unmount all components
 3S/4S: Unmount R8808, and mount others

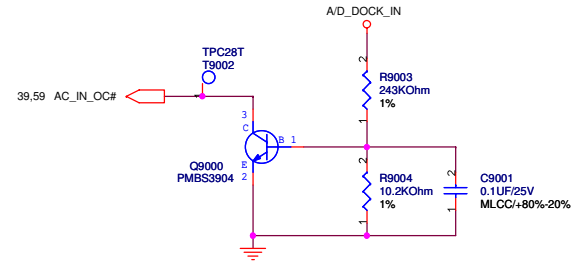
<< Kennedy_Zhang >>

<Variant Name>		
		Title : N/A
<OrgName>		Engineer:
Size Custom	Project Name F7SR	Rev 1.1
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BATTERY IN DETECT

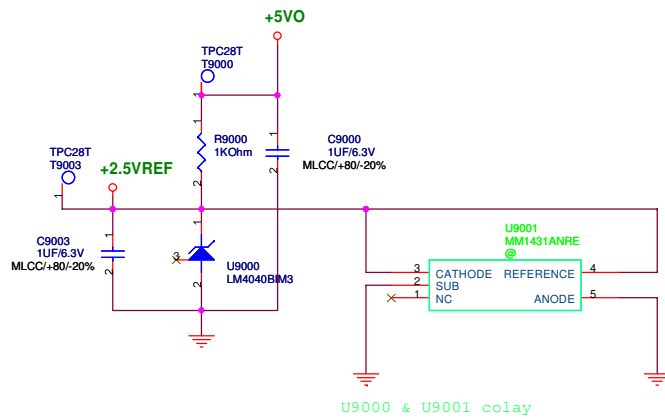


ADAPTER IN DETECT



<< Kennedy_Zhang >>

+2.5VREF

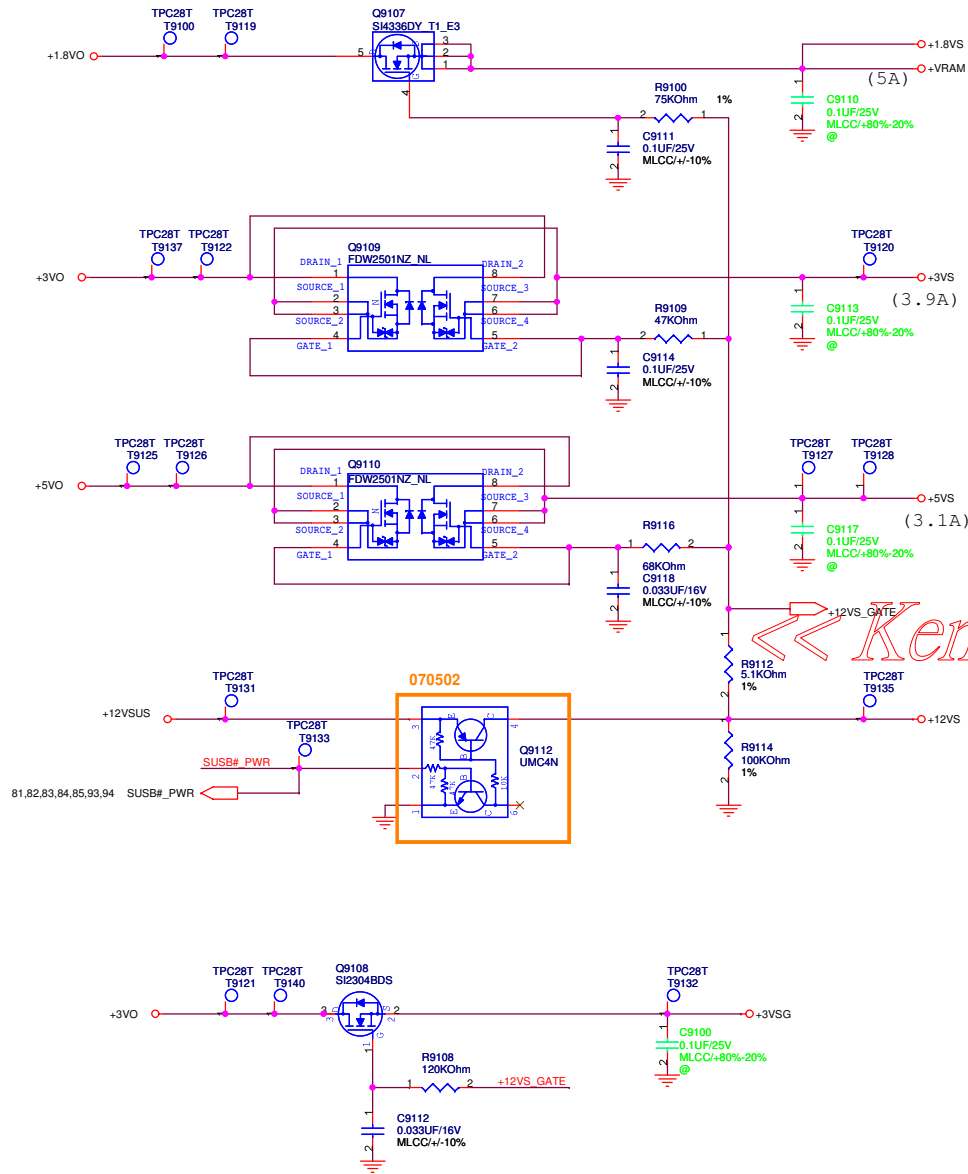


U9000 & U9001 colay

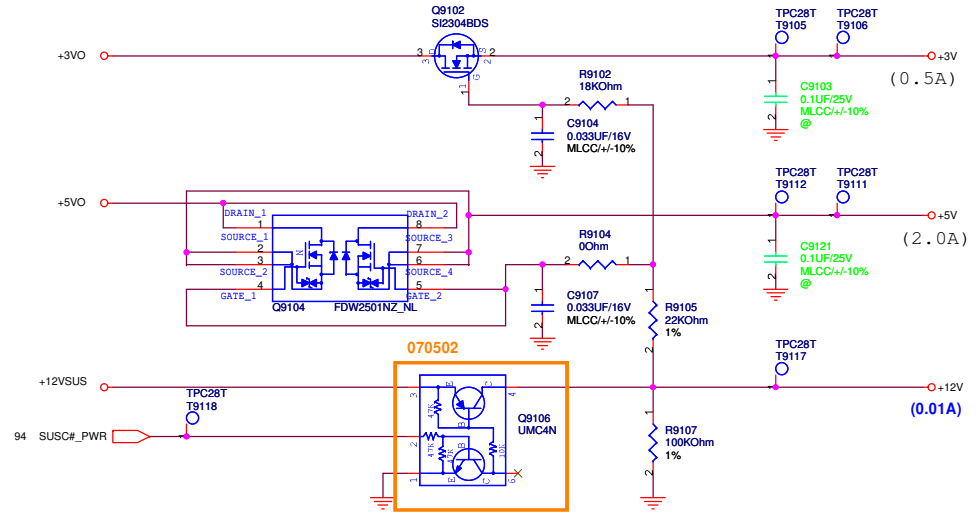
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		Title : POWER_DETECT	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	F7SR	1.1	
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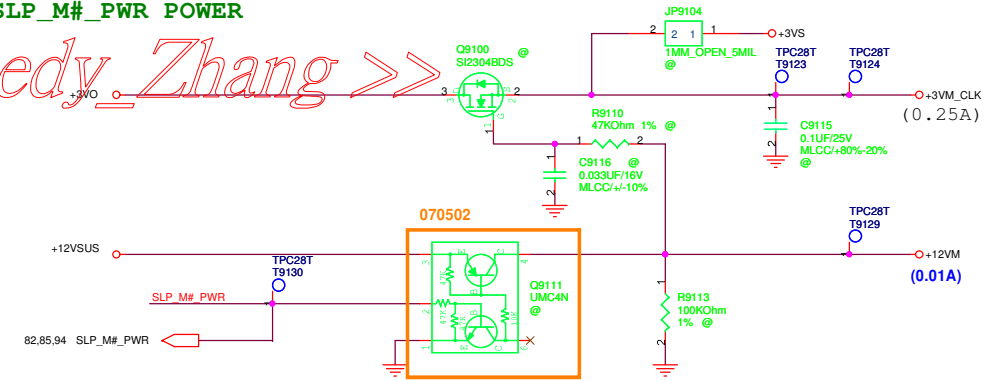
SUSB#_PWR POWER



SUSC#_PWR POWER



SLP_M#_PWR POWER



<< Kennedy_Zhang >>

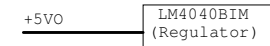
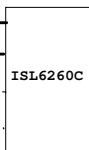
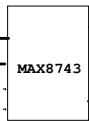
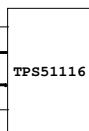
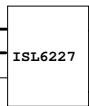
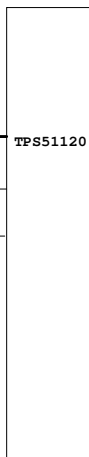
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ASUS		Title : POWER_LOAD SWITCH	
<OrgName>		Engineer :	
Size	Project Name		Rev
Custom	F7SR		1.1
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A/D_DOCK_IN

AC_BAT_SYS

VSUS_ON



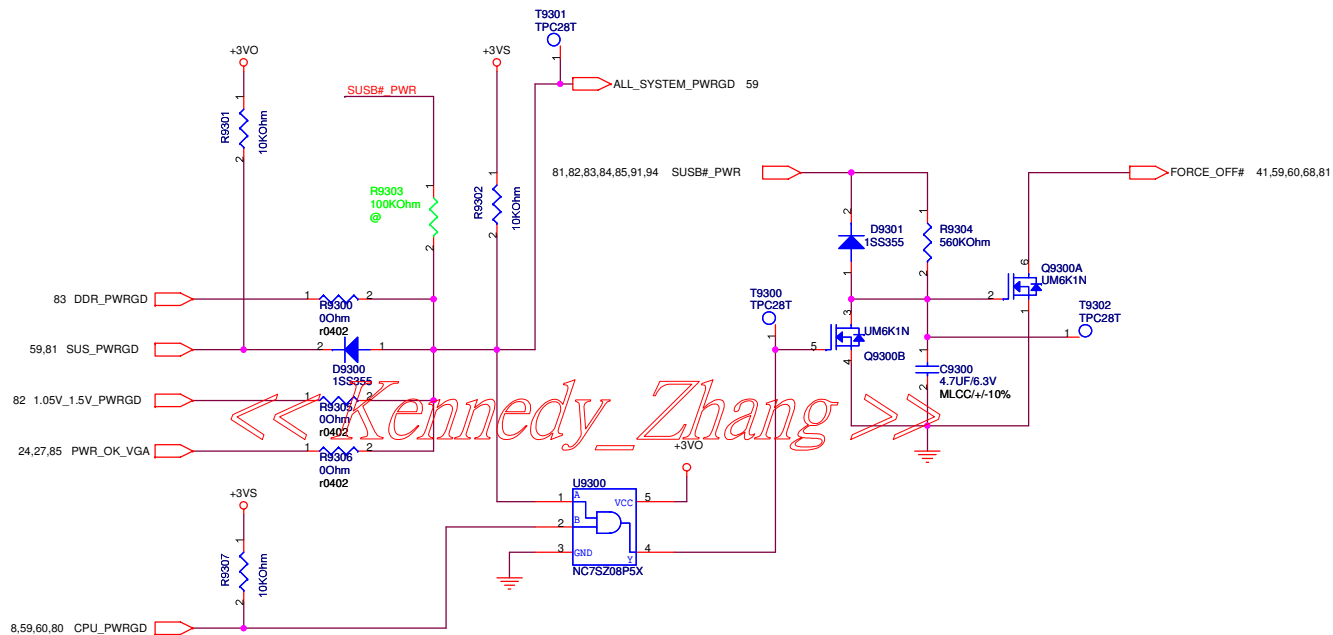
<< Kennedy_Zhang >>

VR_VID0-VR_VID6, H_DPRSTP#, MCH_OK, PM_DPRSLEPVR, PM_PSI#, VCCSENSE, VSSSENSE, STP_CPU#

<Variant Name>

ASUS		Title : POWER_VCORE
<OrigName>		Engineer:
Site	Project Name	Rev
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POWER GOOD DETECTOR



<Variant Name>



Title : POWER_PROTECT

<OrgName>

Engineer:

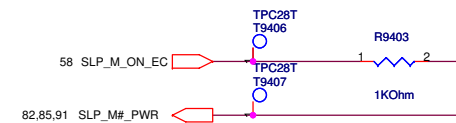
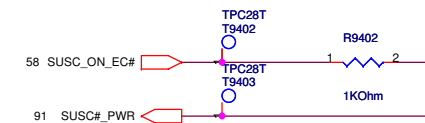
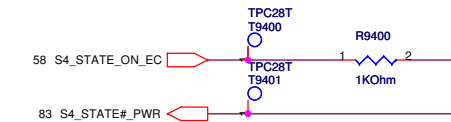
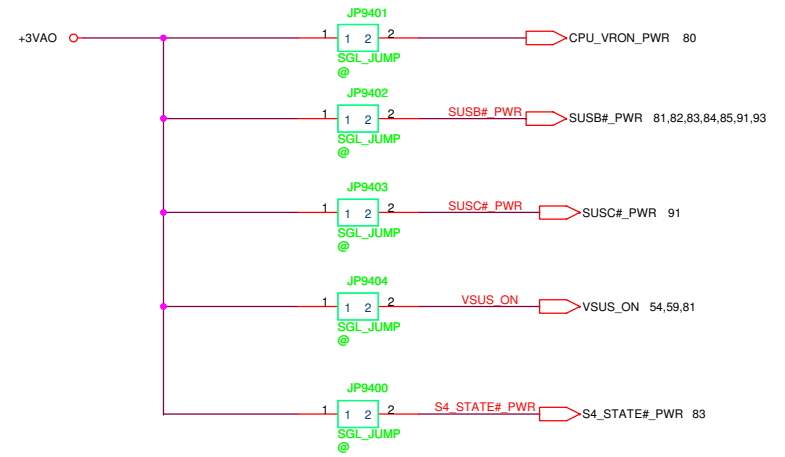
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Custom	F7SR	1.1

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FOR POWER TEST

AC_BAT_SYS	AC_BAT_SYS	68,80,81,82,83,85,88
+3VA	+3VA	15,33,41,42,58,59,60,81
+1.5VSUS	+1.5VSUS	
+5VO	+5VO	66,81,82,83,84,85,88,90,91
+3VO	+3VO	81,84,85,91,93
+3VSUS	+3VSUS	16,17,18,44,45,54,59,81
+5VSUS	+5VSUS	18,66,81
+3V	+3V	33,42,45,47,49,54,57,76,78,91
+3VS	+3VS	4,8,12,15,16,17,18,32,33,35,37,42,44,47,48,49,51,52,53,54,56,57,59,60,66,70,72,73,76,80,84,91,93
+3VM	+3VM	17,18,20,21,39,65,84
+3VAUX_GOLAN	+3VAUX_GOLAN	
+3VM_CLK	+3VM_CLK	39,91
+12VSUS	+12VSUS	81,84,91
+12V	+12V	42,53,57,91
+12VS	+12VS	27,32,33,57,66,91
+5V	+5V	33,42,54,62,91
+5VS	+5VS	17,18,32,35,37,42,44,56,57,61,66,72,80,91
+2.5VO	+2.5VO	84
+2.5VS	+2.5VS	23,27,42,56,84
+1.8VO	+1.8VO	83,91
+1.8V	+1.8V	8,11,12,20,21,42,83
+VCCP	+VCCP	4,5,7,9,11,12,15,18,23,27,39,42,82
+1.05VM	+1.05VM	11,82
+0.9VO	+0.9VO	83
+0.9V	+0.9V	22,42,83
+0.9VS	+0.9VS	28,29,42,83
BAT	BAT	88
+2.5VREF	+2.5VREF	84,88,90
+VCORE	+VCORE	5,80
+VGA_VCORE	+VGA_VCORE	23,27,85
+VRAM	+VRAM	23,24,25,27,28,29,42,73,91
+1.25VS	+1.25VS	12,18,23,27,42,85
+1.25VM	+1.25VM	8,12,85
BAT_CON	BAT_CON	68,88
+1.1VS	+1.1VS	23,27,84

<< Kennedy_Zhang >>



<Variant Name>


ASUS		Title : POWER_SIGNAL	
<OrgName>		Engineer:	
Size Custom	Project Name F7SR		Rev 1.1
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Rev	Date	Description
1.0	2006/07/	1. Initial release.
1.1	2006/09/29	1.Enable INTVRMEN and LAN100_SLP (Remove R1506, R1511).[15] 2.Change R0803 R0804 to 20ohm.[8] 3.Set PCIE graphic lane to normal mode.(Unmount R0809).[8] 4.Pull high 10Kohm at 3GSIM_DATA.[33] 5.Change INVCN0 to 20 pin.[33] 6.Change net name "INT_MIC_P" to "INTMIC_P".[56] 7.Change R5706 and R5707 to 75ohm.[56] 8.Change CE5701 and CE5702 to 100UF.[57] 9.Add +1.5V discharg circuit.[42] 10.Remove R5415.[54] 11.Change power "+12V" to "+12VS".[54] 12.Change R6401,R6403,R6409 to10KOhm.[64] 13.Change C2940 to0.1uF.[28] 14.Change EC_GPIO pin define for design IP.[59] 15.Add debounce and thermal circuit for EC design IP.[60] 16.Change C1612,C1613 to 0.1uF.[16] 17.Change C7302,C7308 to 10uF and remove C7315, C7307,C7321,C7301,C7309,C7313,C7310,C7320, C7321.[73] 18.Remove Q4401,Q5404 and change R1604 to 1Kohm.[16,44,54] 19.Revers D6602.[66] 20.Remove C4401,C4404.[44] 21.Colay M66/M76M.[23~30] 22.Connect ICH8M_LAN_RST# to GND.[17] 23.Add JACK detect circuit at DOS mode.[15] 24.Connect M_VREF_MCH to" 0.9V_VTT_REF".[8] 25.Change R0402 to 1Kohm.[4] 26.Change R3952 to 270Ohm.[39] 27.Swap "xD_GND1" and "xD_CD".[53] 28.Add R and C to avoid pop.[56] 29.Add 3G Led circuit.[66] 30.Connect "BUF_PLT_RST#" and "IDERST#" by 47Ohm.[72]

Rev	Date	Description

<< Kennedy_Zhang >>

<Variant Name>

		Title : History	
ASUSTek COMPUTER INC		Engineer: <i>Jack Chen</i>	
Size	Project Name	Rev	
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