SUCHITAV KHADANGA

Analog RF IC CONSULTANT

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Good experience in analog and wireless chip, circuit, layout and testing with different foundries and different technologies since 1997.

NEW COMPLETED PROJECT: APR 2021 CIRCUIT DESIGN AND LAYOUT OF LDO, POWER MANAGEMENT IC –XFAB

NEW PAPER Design of low-power CMOS transceiver front end for 2.4-GHz WPAN applications

https://www.ias.ac.in/describe/article/sadh/045/0131

Have experience in complete rf asic : asic testing- assembly- bond pad- esd protection- full chip layout- circuit design- eda tools .

Suchitav Khadanga (Bangalore, India) is an electronics design engineer having more than 20 years of solid experience in wireless and semiconductor products. Throughout his professional career, he has designed and managed designs from concept to mass production on wireless and broadband RFICs and wireless consumer products, successfully worldwide in million units. He graduated with first class distinction from BU, India, where he studied microelectronics, analog and digital electronics, electromagnetic theory and microwave. After completing research on microelectronics and microwave in CEERI (Central Electronics engineering research institute), Pilani, India he is working in analog and wireless development companies since 1997. In his role he had worked in international locations with companies Intel, NXP, WIPRO. He had successfully completed projects in wireless communication, cellular communication, UWB, WLAN. His main area of work is analog and wireless communication, RFIC, high speed analog, CMOS process. He is now in RFIC technologies, Bangalore, India and working on design, development of next generation wireless products.

SKILLS

VLSI, CMOS, CMOSRF, TRANSCEIVER, PLL, LNA, PA, SWITCH, OPAMP, VGA

EXPEREINCE OVERVIEW

Companies

INTEL, bangalore

NXP, Germany

WIPRO, bangalore

Athena Semiconductor, Greece

CEERI, Pilani, India

System design, development and production

Multiband Cellular chip

Wireless communication

UWB Transmitter

Power management

Frequency Synthesizer

Transceiver

Circuit Design

LNA VGAVCO,LDO, OPAMP, PFD Frequency Divider

Layout

Full chip WLAN, GPRS

CMOS Inductor

PAD ring VCO LNA

Process and Technology

Cadence, spice, mentor design tool

Semiconductor Device Modeling

tower, tsmc umc xfab

Additional

Managing chip from system till market

Managing design team

Program Management

Some of the analog-RFIC products/designs

- **RFIC-8432**

RF front end chip in tower jazz 180nm cmos SOI process. This is high performance chip of power amplifier, low noise amplifier and switch in a single chip having packaged in 3 X 3 mm 16 pin QFN package.

- **RFIC-8241**

This is a RF front end chip in SIP for 900 MHZ NAN applications. It have cmos SOI switch and LNA with high performance SiGe (31 dBm) power amplifier in one package 4 X 4 mm QFN 24 pin package.

- **RFIC-8242**

This is 10 pole switch targeted for multiband transreceiver having 2 Tx and 8 RX input/outputs with one antenna pin. power handling capability is above 30 dBM and very low insertion loss less than 0.5dB for wide frequency range till 4000 MHz.

- **Frequency Synthesizer design**

Client : NXP, Nuremberg Germany

Product: Aero 4223 TSMC 130nm

This is the frequency synthesizer for the quad band transceiver and designed with TSMC 130nm cmos process technology. The frequency range is 6.5 to 8.5 GHZ. The tank of the vco is combination of fixed capacitor, switched capacitor, varactor and inductors.

- **RFCMOS mixer**

Client : NXP, Nuremberg Germany

This is the mixer for the quad band transceiver and designed with TSMC 65nm cmos process technology. This mixer is in the receiver section of the transceiver chip.

- **Mixer Design**

Client : Athena Semiconductor (acquired by broadcom), Athens, Greece

Product: ATS 5001

This is mixer in receiver path of quad band receiver. The cmos mixer is double balanced passive mixer initially designed in 0.13 um technology. The design started with analysis of different mixer architectures and after comparison passive mixer had chosen for low power application.

VARIABLE GAIN AMPLIFIER

Client : Athena Semiconductor (acquired by broadcom), Athens, Greece

Product: ATS 2001

This is in base band section of GPRS chip and designed for low noise and low power. This is a two stage amplifier, the first one is fixed low gain and low noise, the second one is an opamp used for changing gain. The frequency is 200Hz to 200 KHz with gain varies from -4 to 26 dB (step size 6dB). The integrated noise is 4nV/sqHz when gain is maximum. The VGA is designed as an independent module and finally integrated in GPRS chip.The VGA design is completed using UMC 0.18um 1.8V process.

- **UWB Transmitter design**

Client : Intel Bangalore, Bangalore, India

Product: Cayman Intel 90nm process

The design and development of UWB transmitter is completed. This is transmitter section of UWB transceiver test chip. The power consumption is 50mW. The transmitted signal varies from 160mV to 800mV with 50ohm load. The frequency range is 3 to 5 GHz with 500 MHz band

- **PLL (mixed signal design project)**

Company: WIPRO Technology, Bangalore, India

Product: IP Development

Technology Used: TSMC 0.18 um CMOS technology and Specter RF from Cadence Tool.

This is a low power dual modulus pre scaler PLL having step size 1MHz. except the loop filter all the circuit components are on chip.

Contribution: Design of 2.4GHz VCO, pre scaler, programmable divider, phase detector using tsmc 0.18um technology and integration of PLL building blocks.

- **Low Noise Amplifier Design**

Company: WIPRO Technology, Bangalore, India

Product: IP Development

LNA is designed using tsmc 0.18um technology. This is inductively degenerated common source amplifier. . The gain of LNA is 15 dB, noise figure 2.1dB at 2.4GHz frequency having bandwidth 100 MHz, total power consumption is 23mW.

- **CMOS Operational Amplifier Design (analog design project)**

Company: WIPRO Technology, Bangalore, India

Product: IP Development

Technology Used: TSMC 0.25 um CMOS technology and Specter RF from Cadence Tool.

Two stages CMOS Operational amplifier is designed using 0.25um cmos technology .The opamp is designed successfully. Gain of opamp is 30K with unity gain 10MHz and power dissipation is 1.9mW.

EDUCATIONAL QUALIFICATION

M. Sc. in Electronics from Berhampur University, orissa, India in 1997

Microelectronics from CEERI, Pilani, India

PERSONNEL DETAILS

Address	: 401, green castle, St john's road, Ulsoor, Bangalore, India-560042
Professional	: Analog and RFIC
Date of birth	: 15th June 1973
Nationality	: Indian